Digital Calibration for Current-Steering DAC Linearity Enhancement

Faculty of Science and Technology,
Division of Electronics & Informatics
Gunma University
Shaiful Nizam Mohyar, Haruo Kobayashi

Outline

- Introduction
- Problem Statement
- Proposed Techniques
  - Half-Unary Current-Steering DAC
  - Outlier Elimination
  - Current Source Sorting
  - Circuit
  - Layout
- Simulation Result
- Conclusion

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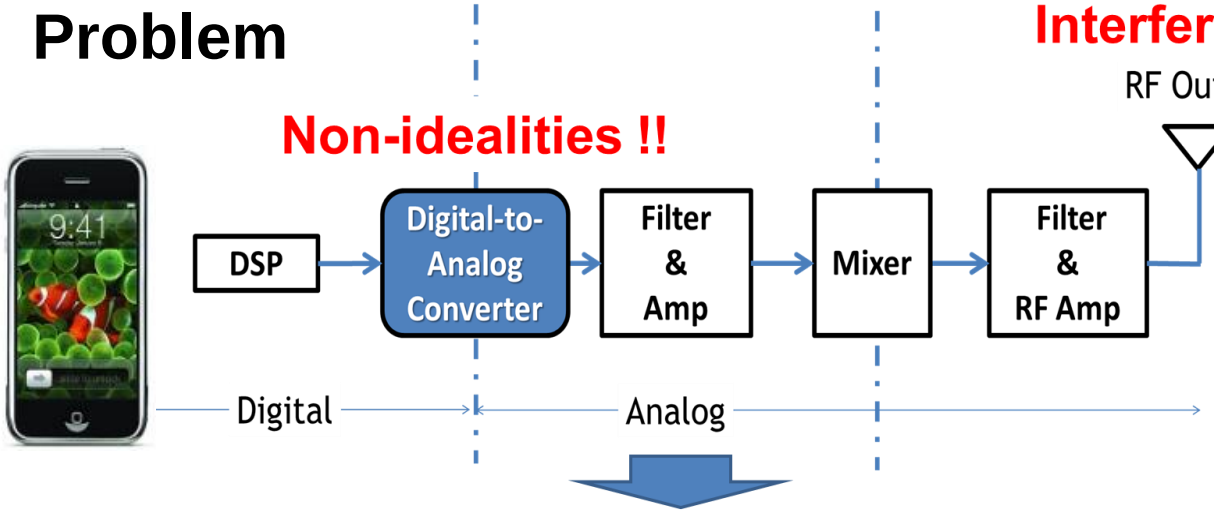
Introduction

- **Background**
  - Telecommunication devices
    - Mobile phones, wireless modems & avionics
    - **High-speed, high-accuracy**

      Digital-to-Analog Converter (DAC)

- **Problem**



Objective & Investigated Method

- **Objective**
  - High SFDR current-steering DAC for communication application

    SFDR: Spurious Free Dynamic Range

    DAC: Digital-to-Analog Converter
- **Proposed method**
  - Current source mismatch effect reduction
    - ① Half-unary DAC architecture
    - ② Current source outlier elimination
    - ③ Current source sorting

    ⇒ Static linearity improvement
  - Layout strategy
    - ① Clock-tree-like layout of current sources & switches

    ⇒ Dynamic linearity improvement

SFDR – Spurious Free Dynamic Range

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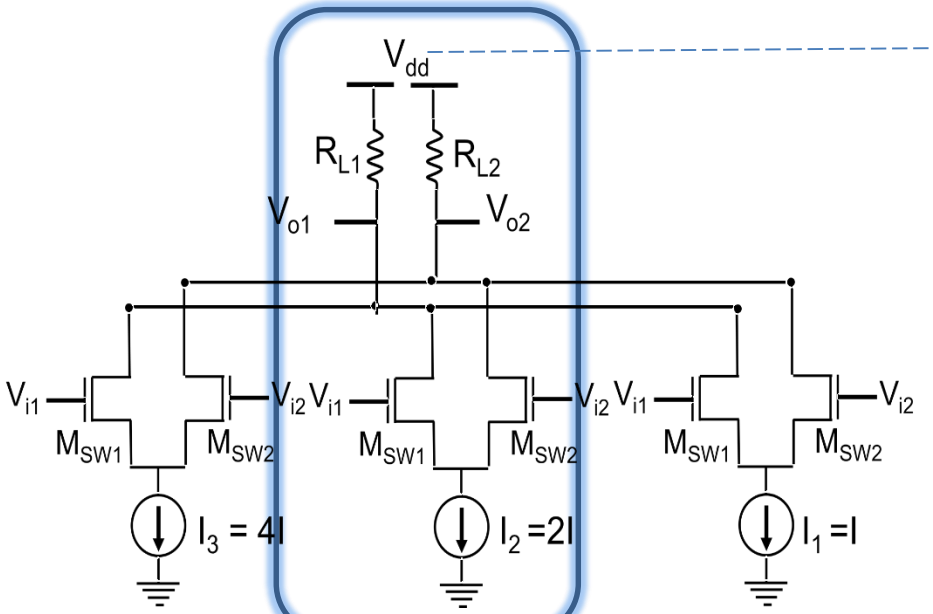
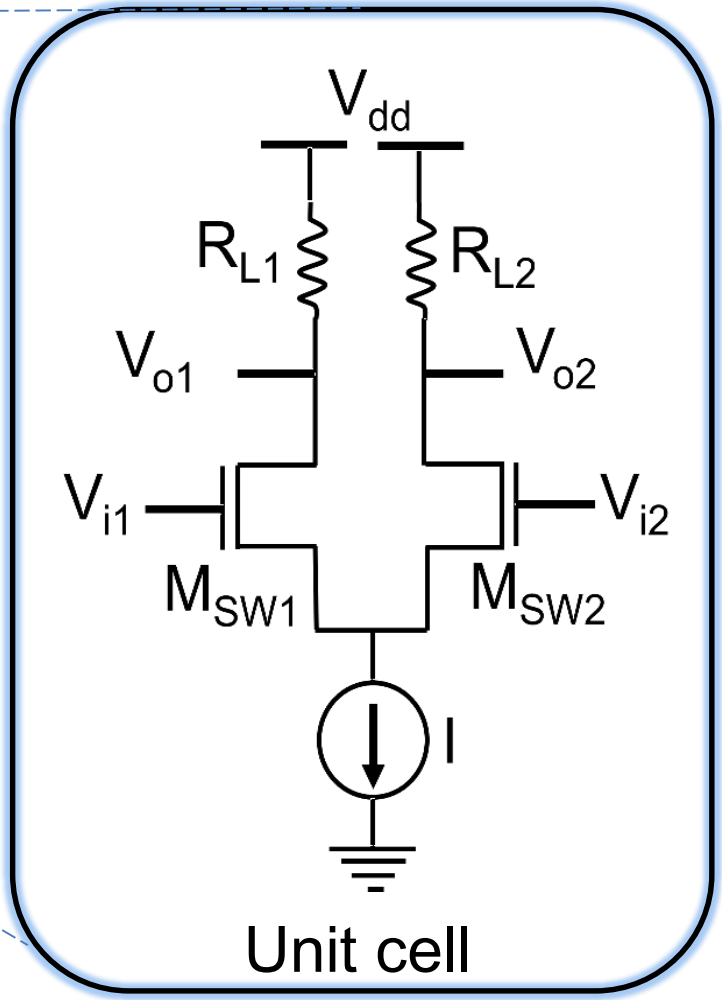
Current-Steering DAC





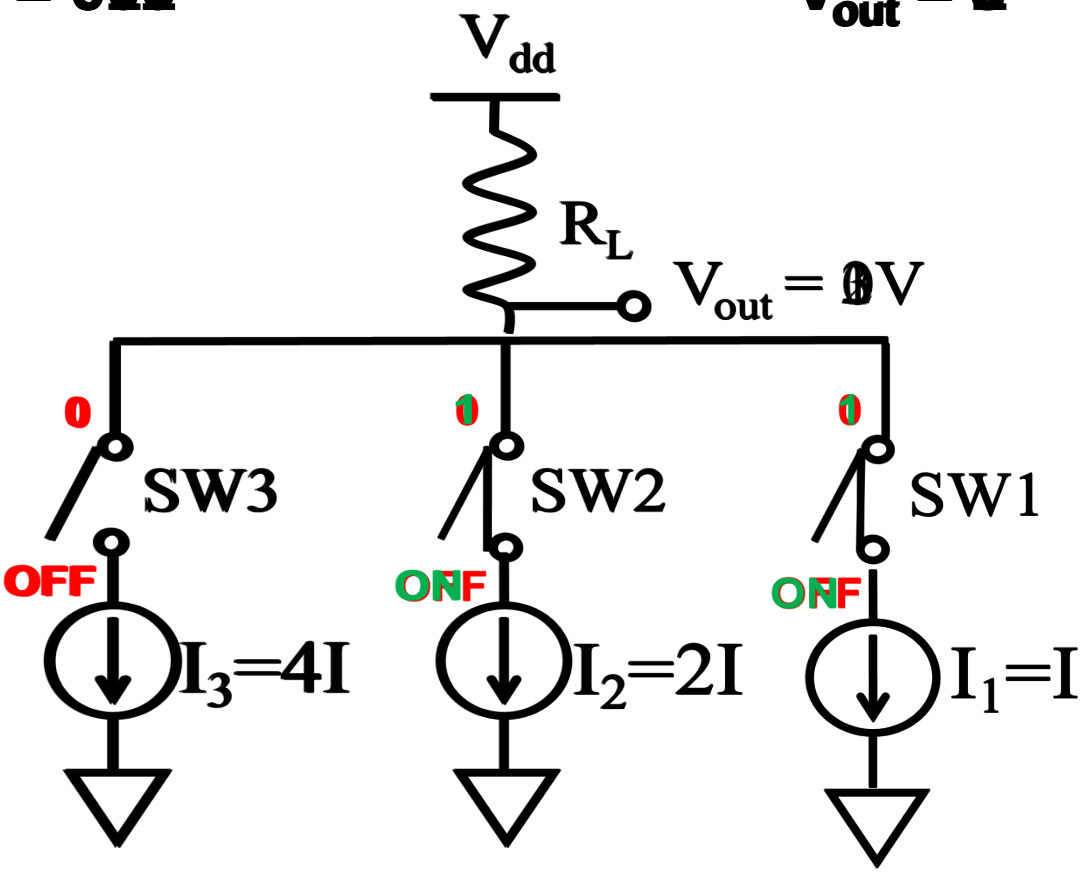
- High speed
- High resolution
- Small chip area

3b binary weighted DAC

Critical condition:

D_{in} = 001

V_{out} = 1/8



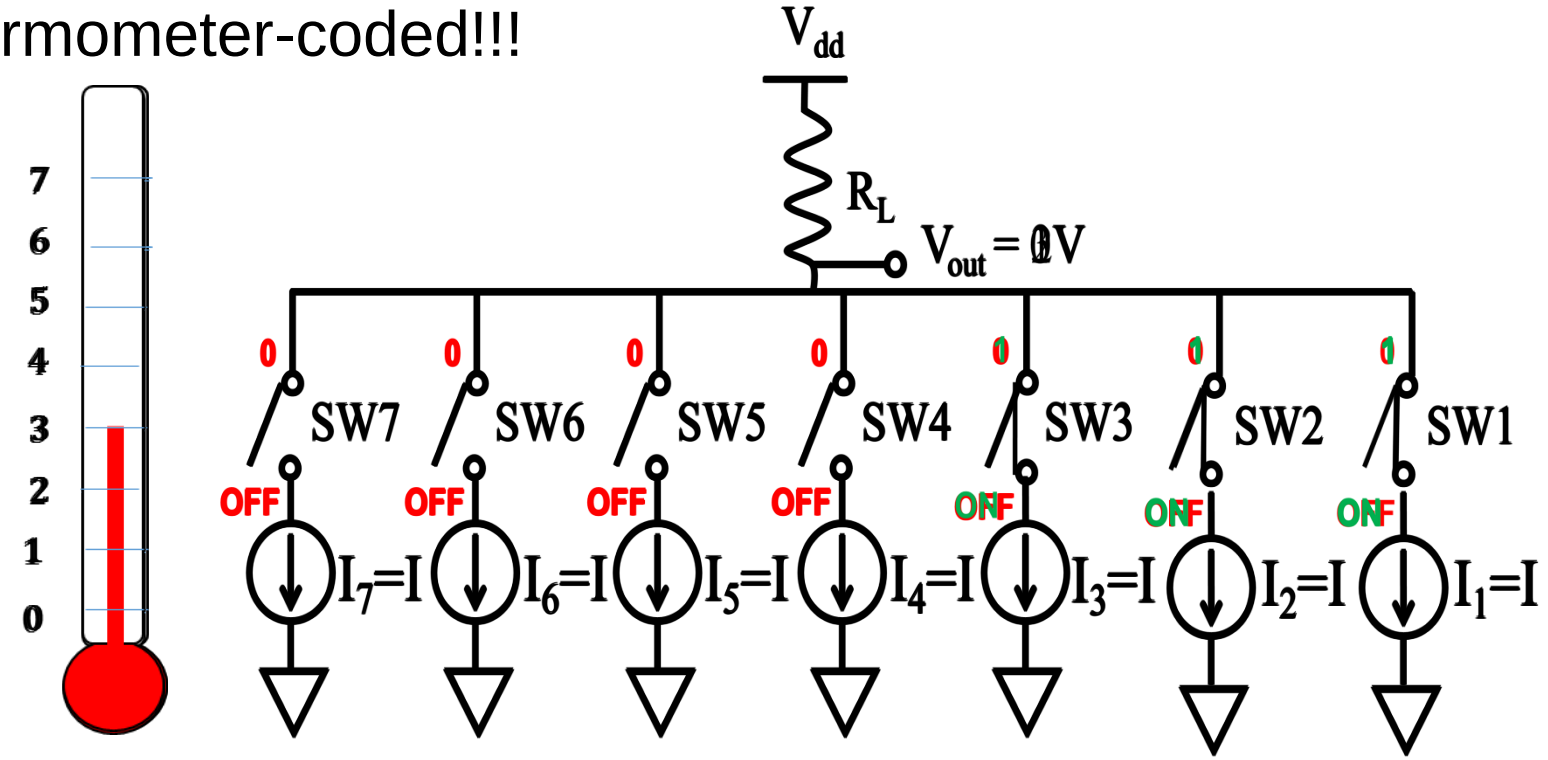
3b Unary weighted DAC

Critical condition:

D_{in} = 0000001 → 0000010

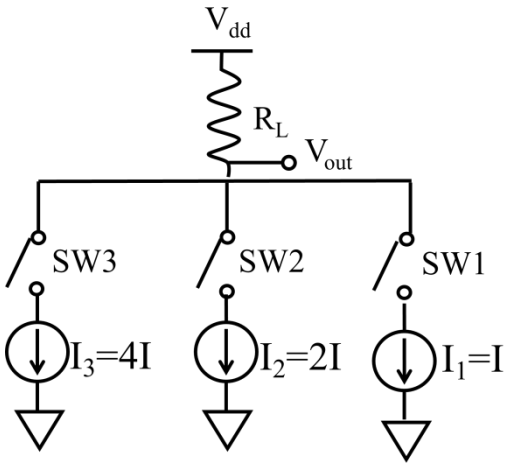
V_{out} = 1/8 → 2/8

Thermometer-coded!!!

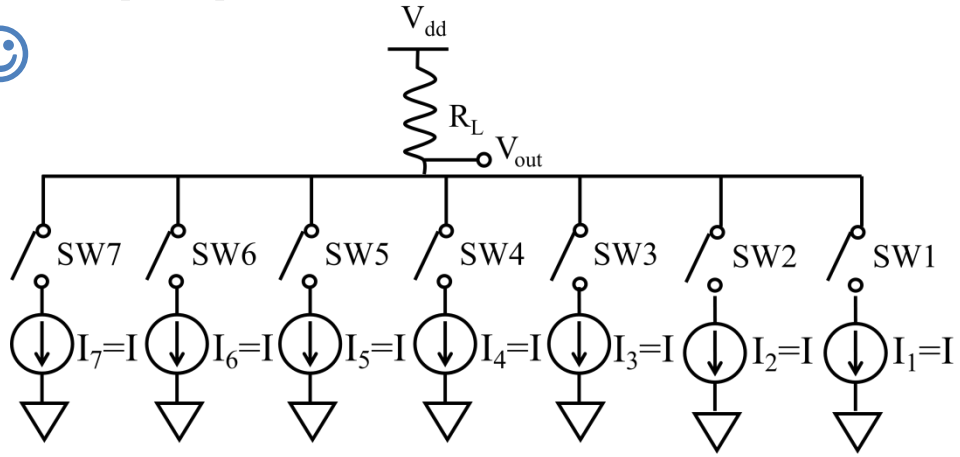


Binary versus Unary CS DAC

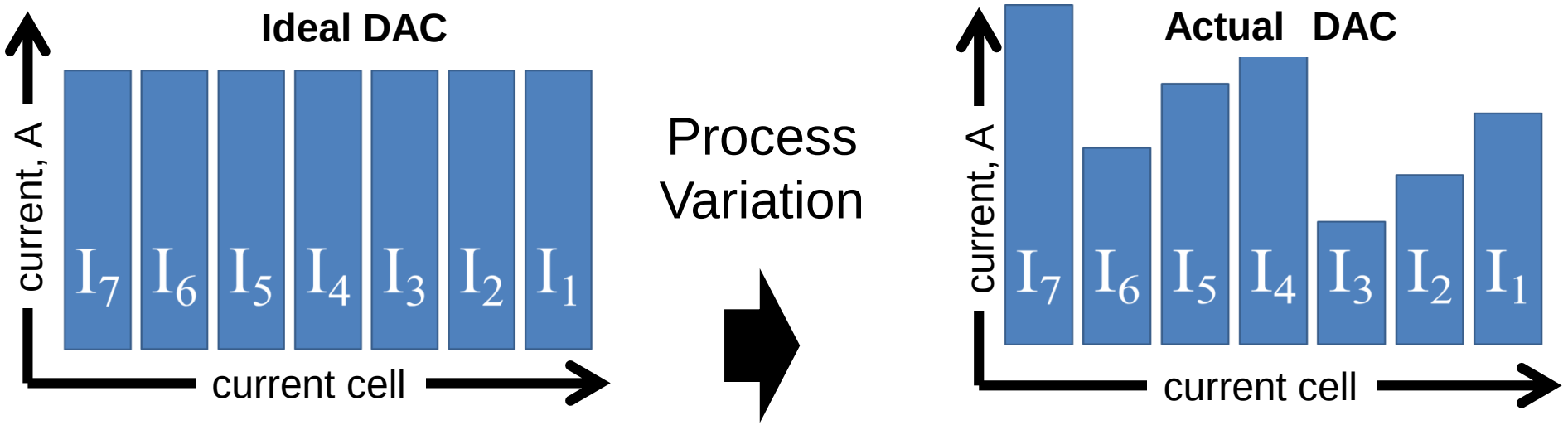
- **Binary**
  - Small silicon area ☺
  - High speed ☺
  - Large glitch energy ☹



- **Unary / Thermometer-coded (TC)**
  - Small glitch energy ☺
  - Redundancy ☺
  - Low speed ☹
  - Large silicon area ☹



Current Source Mismatch



$$I_1 = I_2 = I_3 = I_4 = I_5 = I_6 = I_7 = I$$

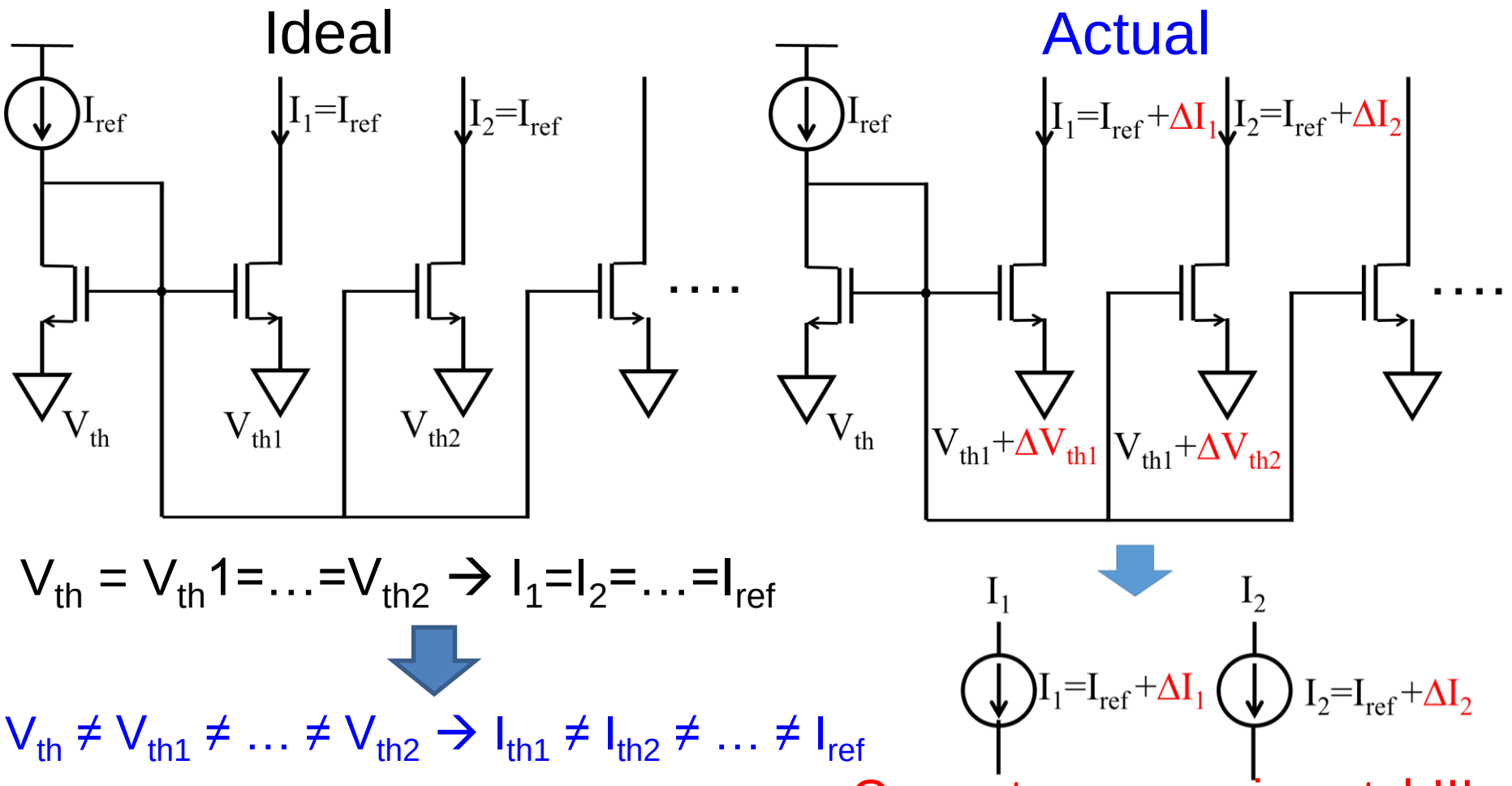
$$I_{ave} = (I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7)/7$$

$$I_k = I_{ave} + dI_k \qquad (k = 1, 2, .. , 7)$$

Current Source Mismatch

➔ DAC nonlinearity ☹!!!

Current Source Mismatch



$V_{th} = V_{th}1=\ldots=V_{th2} \rightarrow I_1=I_2=\ldots=I_{ref}$

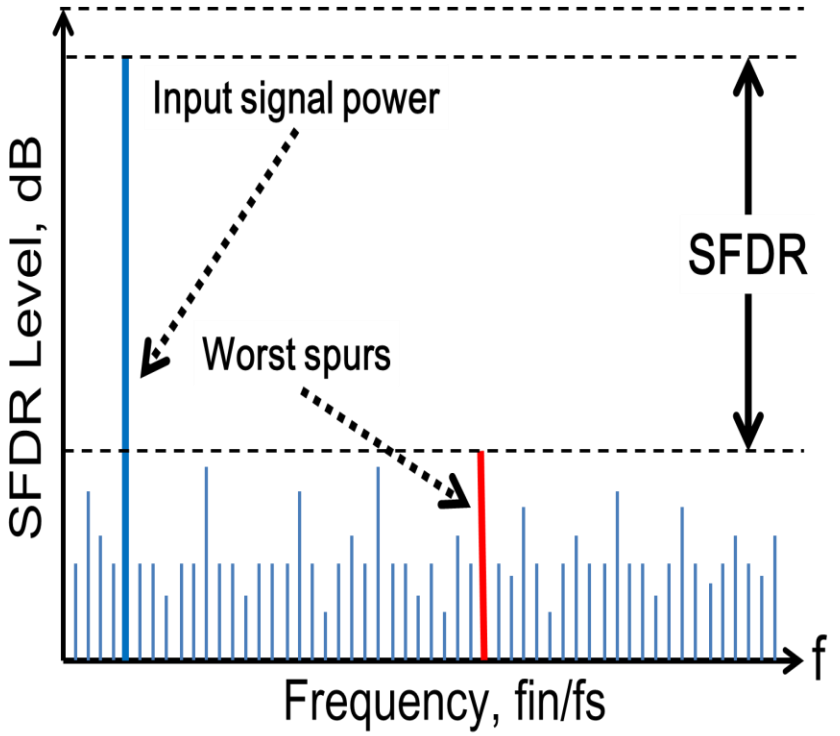
$V_{th} \neq V_{th1} \neq \ldots \neq V_{th2} \rightarrow I_{th1} \neq I_{th2} \neq \ldots \neq I_{ref}$

Current source mismatch!!!

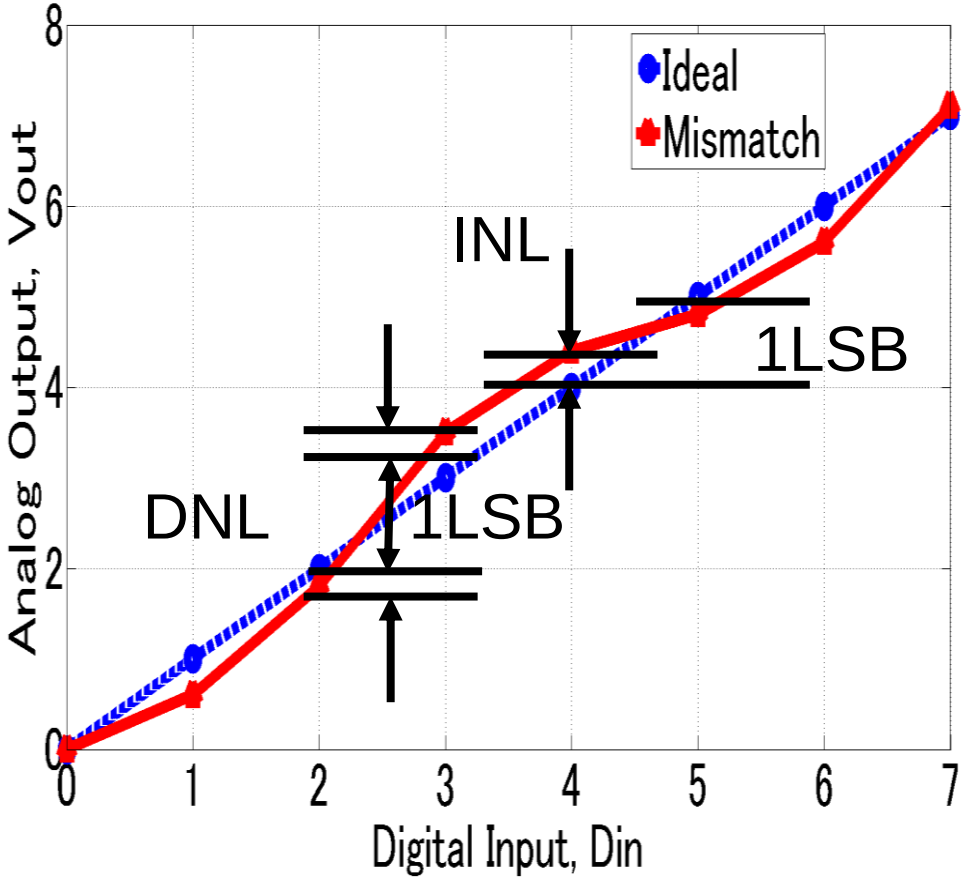
Spurious Free Dynamic Range (SFDR)

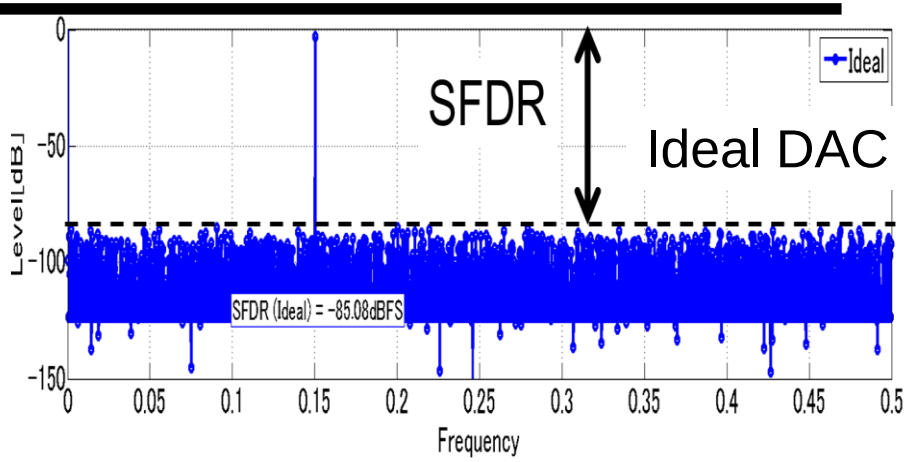
SFDR Degradation Sources

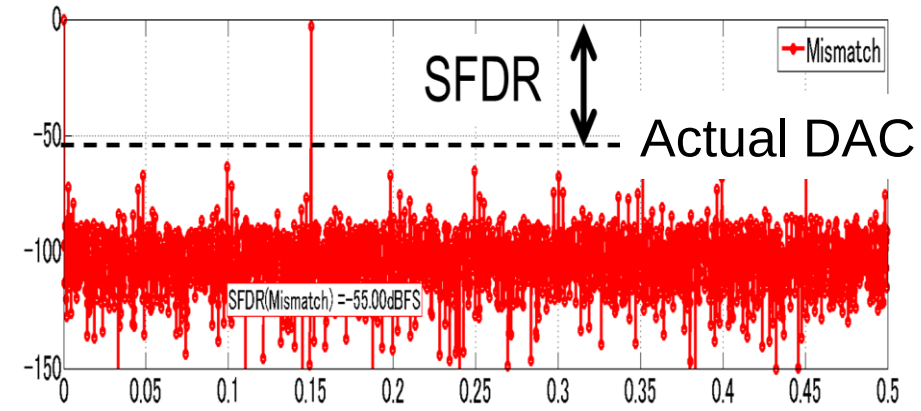
- Unit current source mismatches
  - ➔ Static nonlinearity
- Data-dependent output load variations
  - ➔ Dynamic nonlinearity



Nonlinearity & SFDR degradation





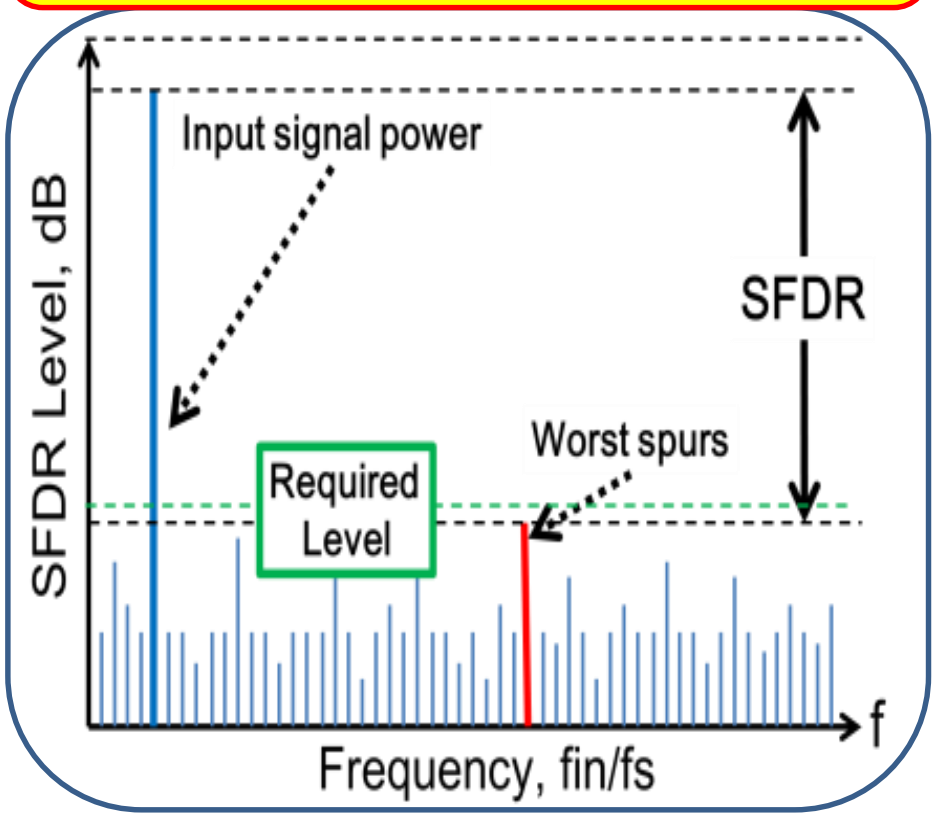


Current source mismatch
➔ DAC nonlinearity ☹

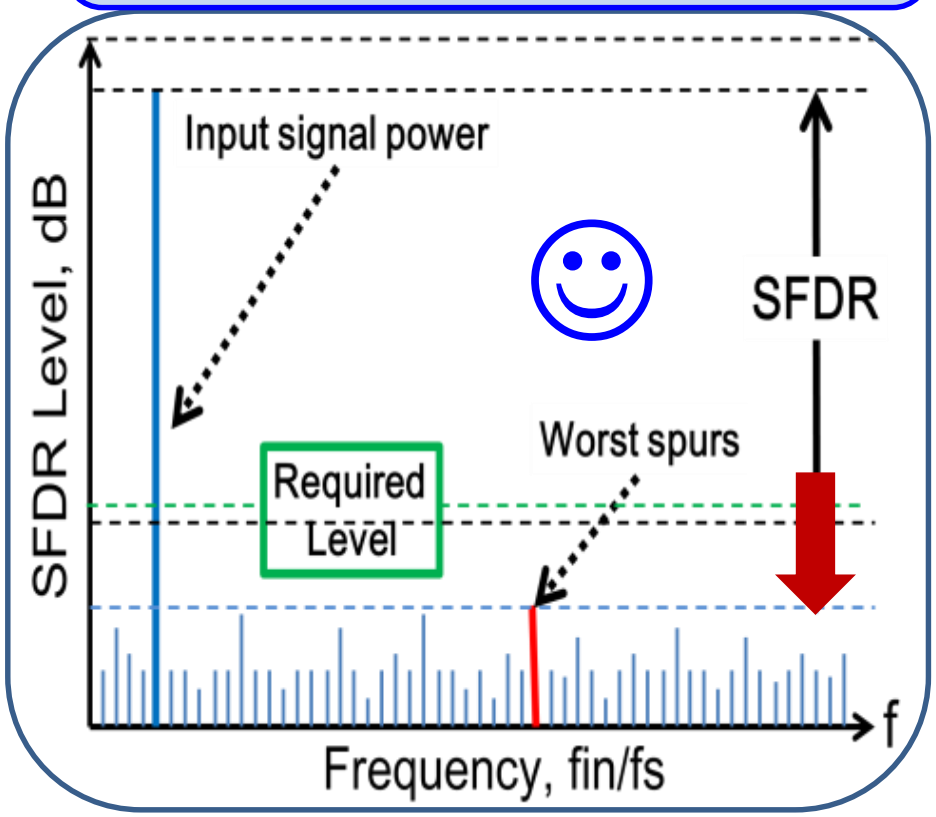
➔ SFDR degradation ☹

SFDR Improvement With Calibration

Without calibration



With calibration



Current-steering DAC Limitation

- Transistor mismatch
  - Current source mismatch
  - Timing errors

DAC static & dynamic non-linearity

- Better transistor matching
  - large size ➔ Power loss ☹
  - Laid out close to each other ➔ Complicated ☹

Design Approach

- **Analog**
  - Complex hardware
  - Not programmable
  - Costly

- **Digital**
  - Simple
  - Programmable
  - Low-cost

➔ **Digital rich approach**
for fine CMOS implementation

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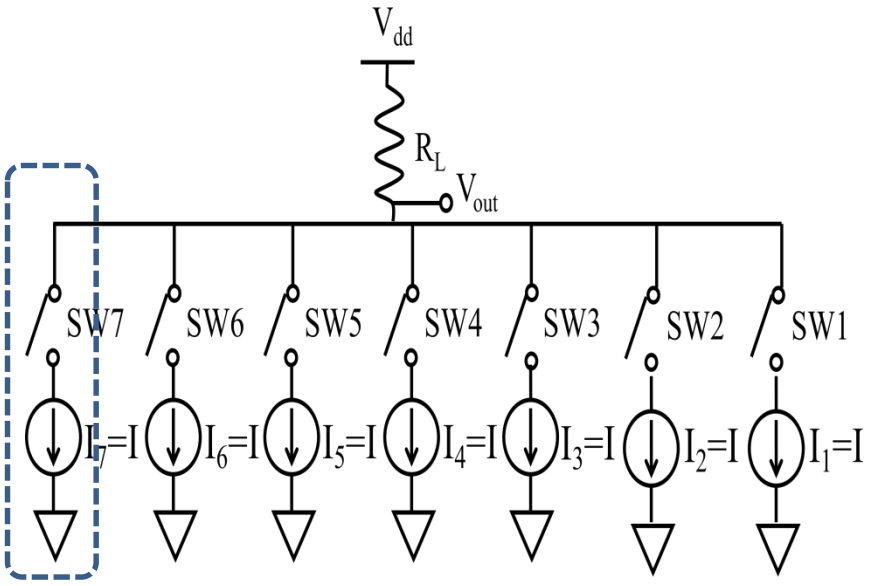
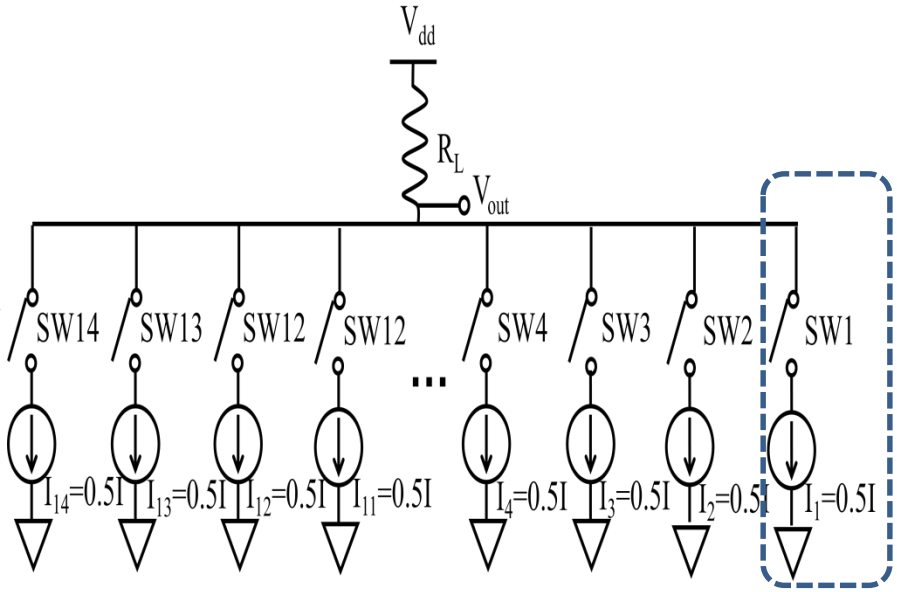
What is half-unary?

Unary



Half-unary

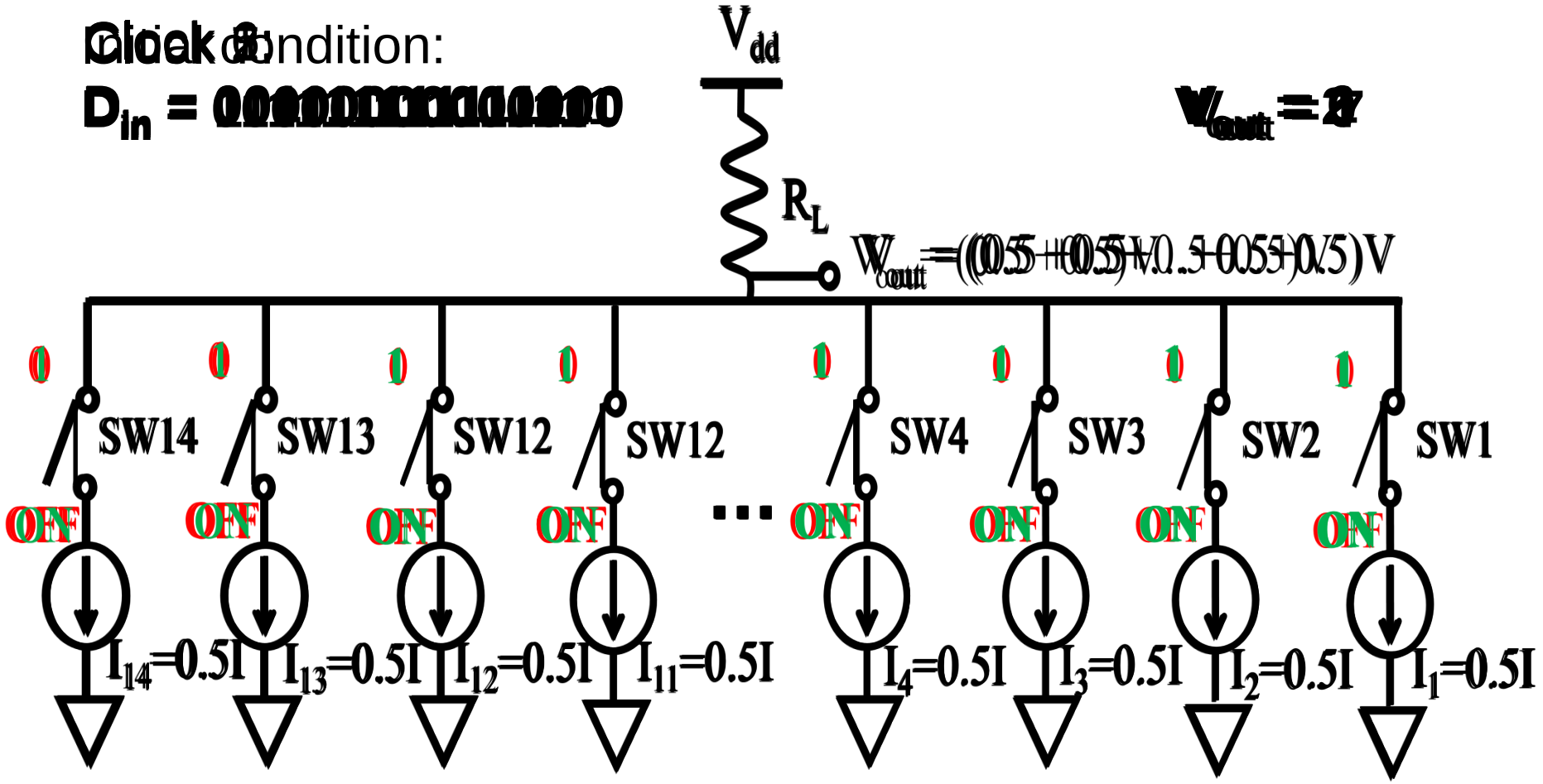


- Each current source cell = I

Each current source cell = 0.5I

- Pair of 0.5I & 0.5I for output of I

Half-unary current steering DAC



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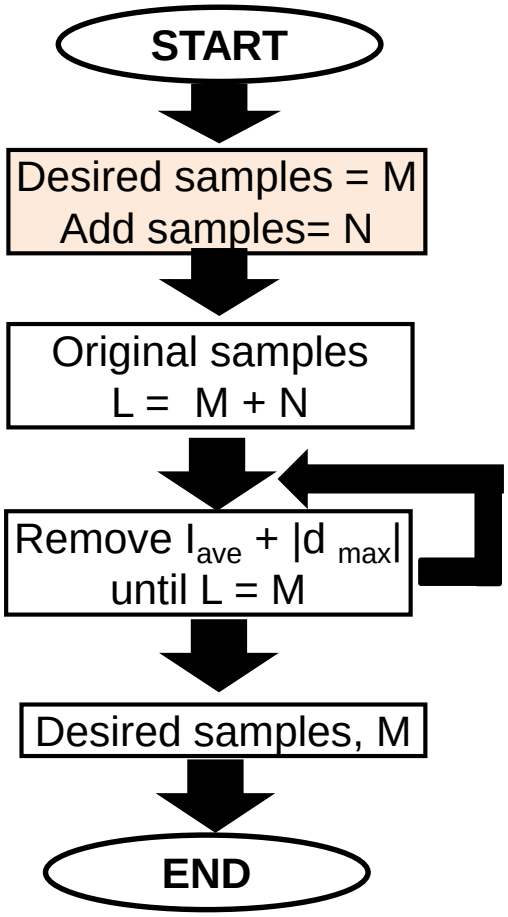
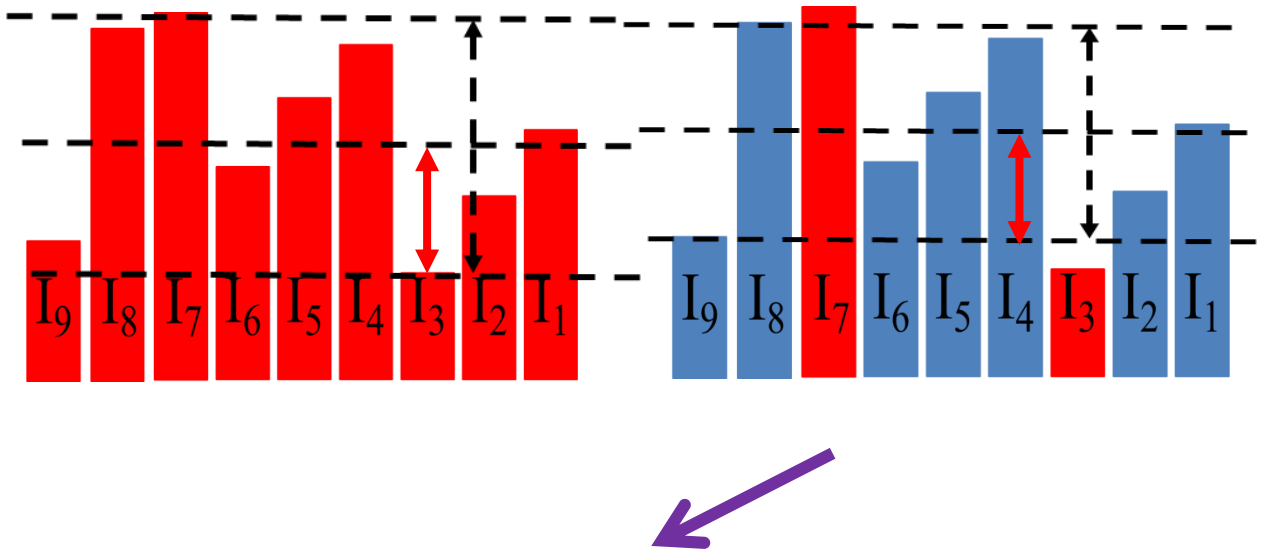
Current Source Outlier Elimination



Before outlier elimination

After outlier elimination



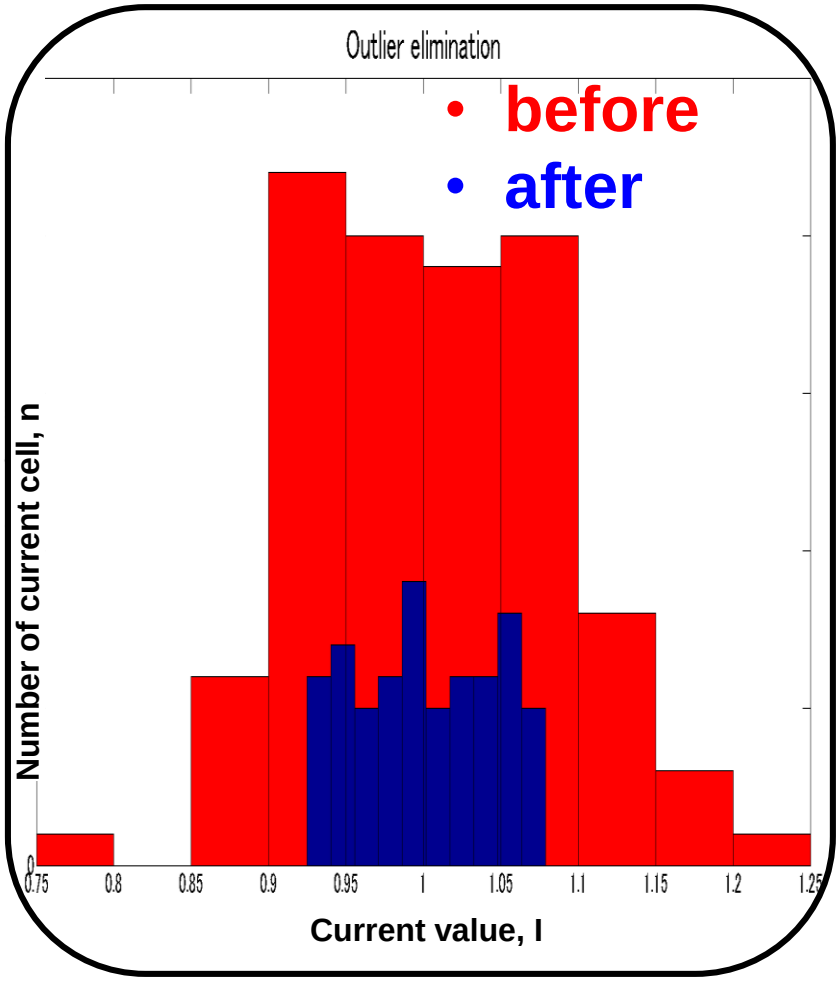
Current source deviation reduction

➔ **Better DAC linearity☺!!!**

Current Source Outlier Elimination Example

6b half-unary
Original number, L =196
Desired number, M = 126
Additional number = 196 – 126 = 70
(56% elimination)

New sample = desired number (126)
New standard deviation
= half of original value



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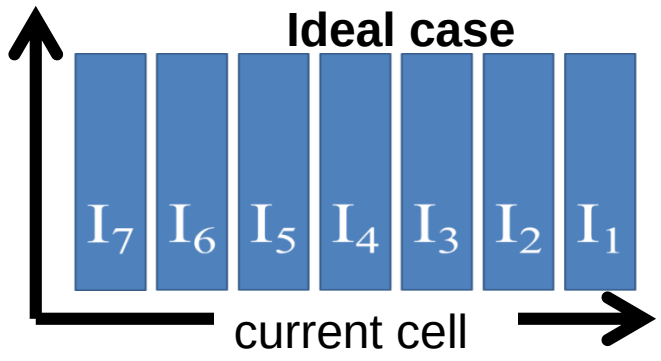
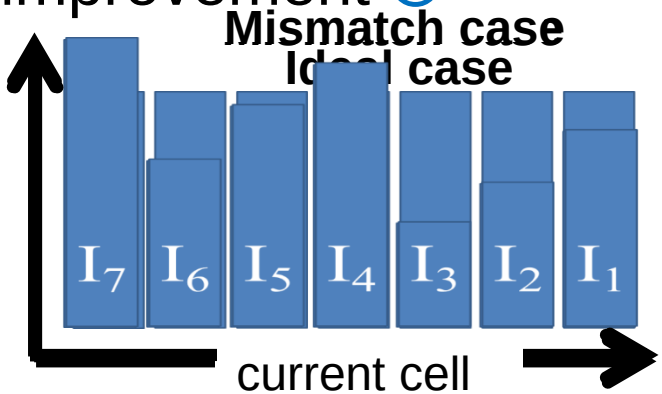
Unit Current Cell Switching Sequence



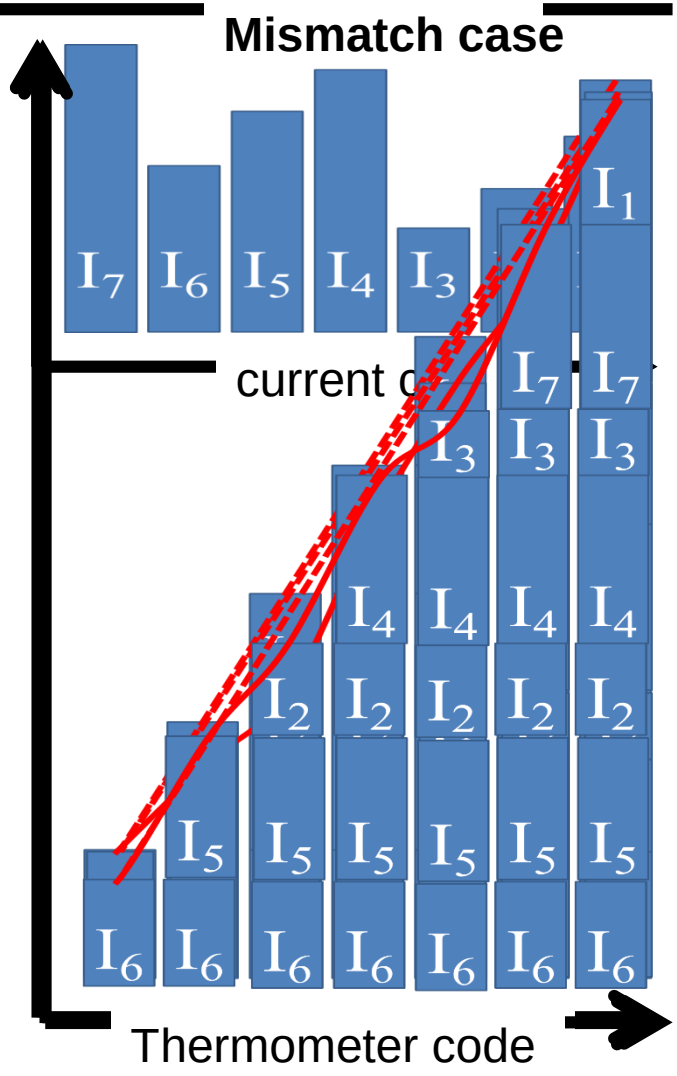
Process Variation

Switching sequence

➔ Integral nonlinearity improvement ☺

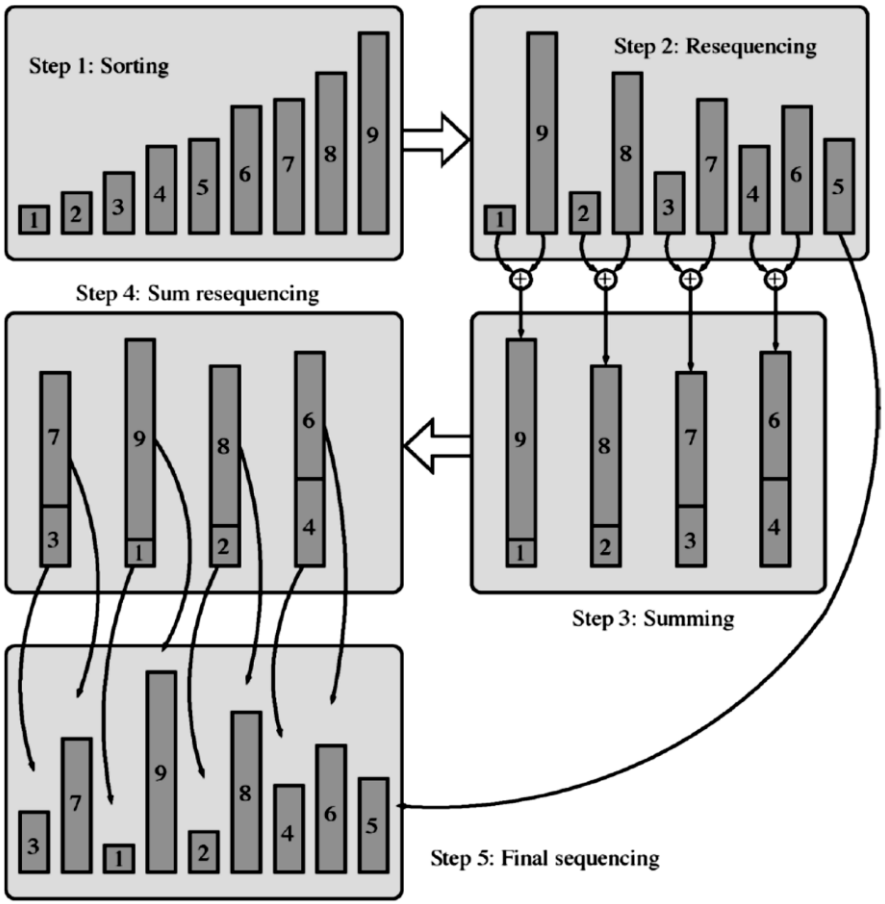


Change **Switching sequence**

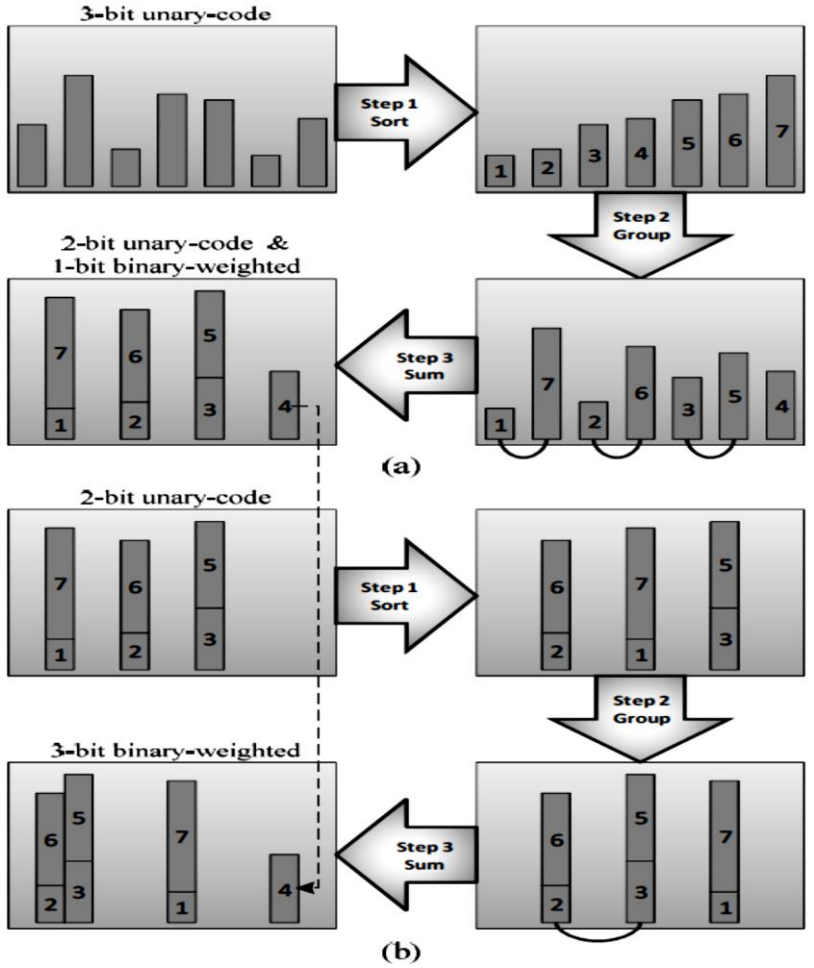


Published Sort & Group Procedures

T. Chen, JSSC (2007)

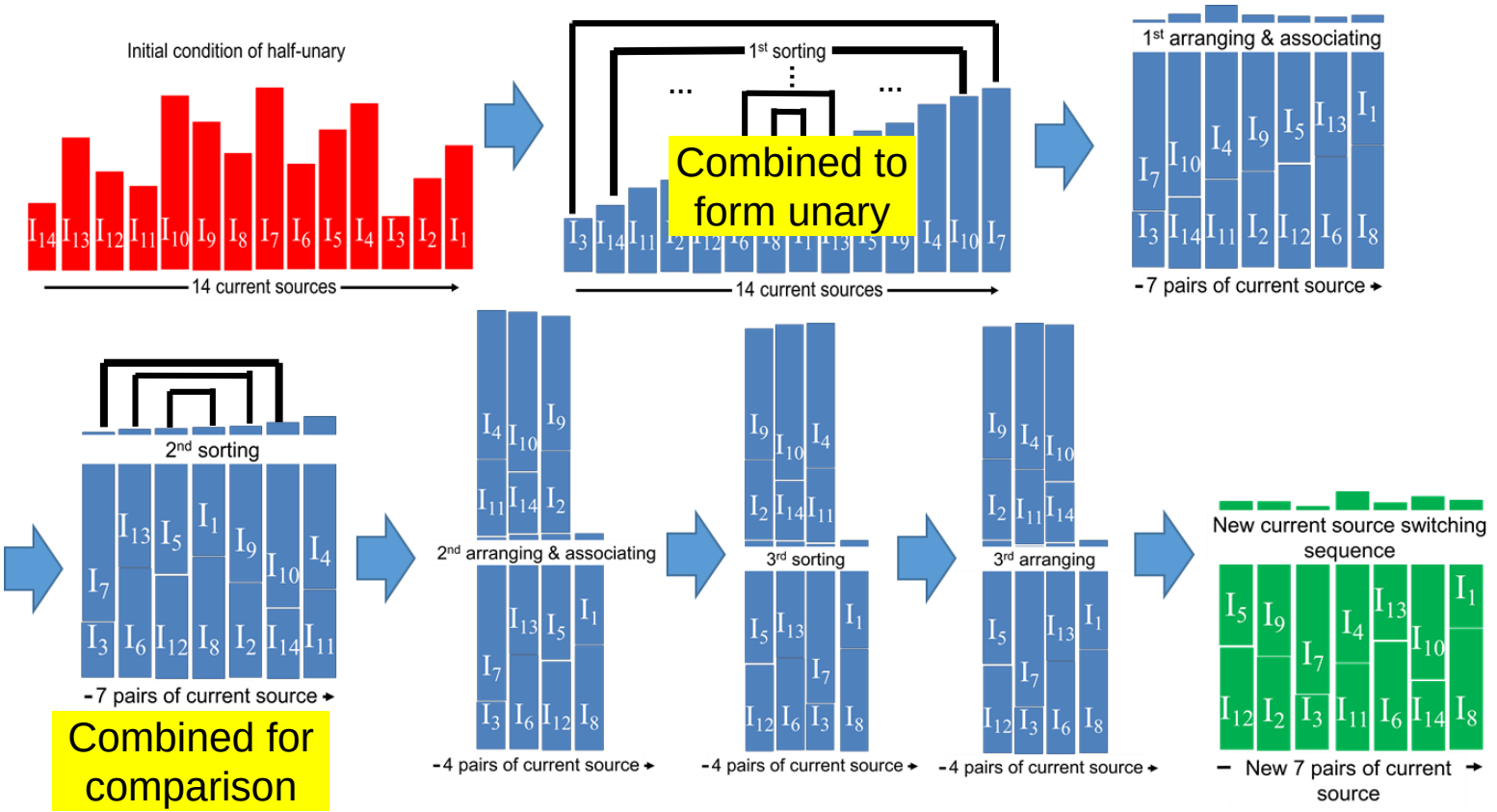


T. Zeng, ISCAS (2010)



CS – current source

Proposed Current Source 3-stage Sort & Group Algorithm



New switching sequence

➔ More linearity improvement ☺!!!

CS – current source

Sort & Group Techniques Comparison

Technique	Features	Advantages	Drawbacks
SSPA JSSC 2007 [2]	• 2-stage sort & group • Change switching sequence	• Improve INL only	• Require additional current sources
Complete-folding ISCAS 2010 [3]	• Convert unary to binary	• Improve INL & DNL	• Procedure steps increase by DAC resolution
This work	• 3-stage sort & group • Convert half-unary to unary • Change switching sequence	• Improve more INL & DNL • Less procedure steps compared to [3]	• Require twice current sources

SSPA –Switching sequence post-adjustment

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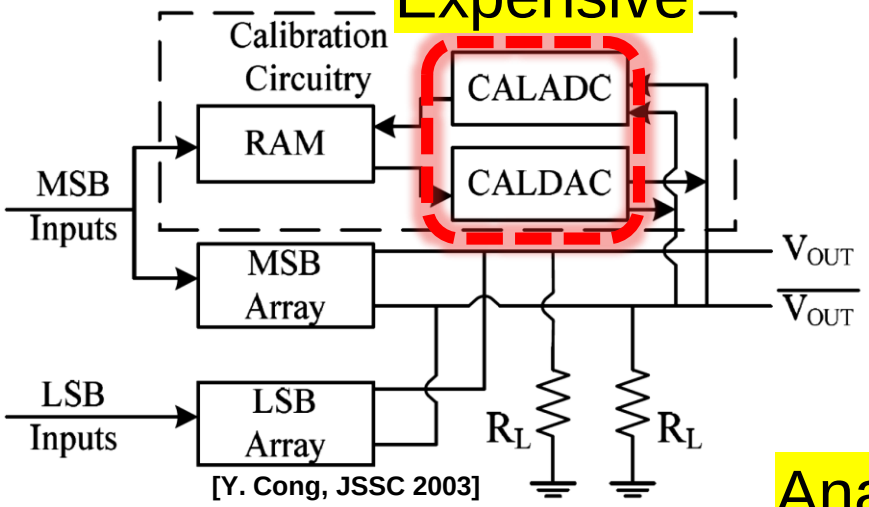
Previous Calibration Circuits

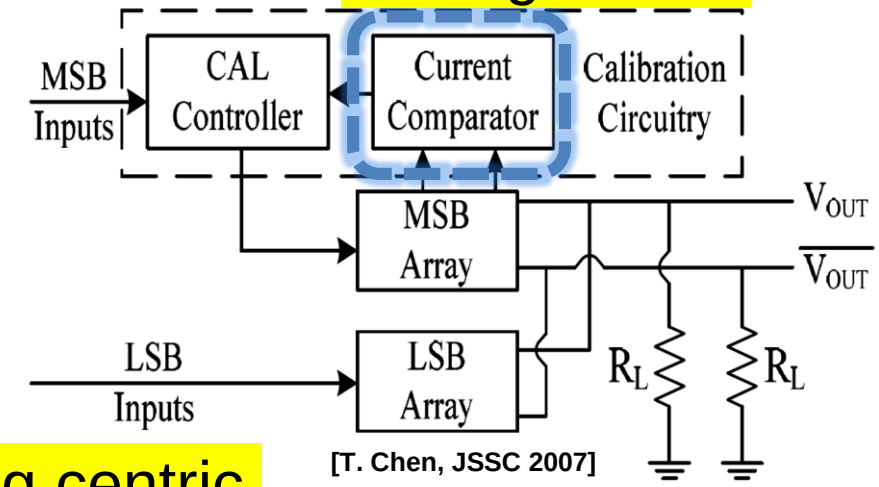
Expensive



[Y. Cong, JSSC 2003]

Fig.1 Block diagram of self-calibration technique

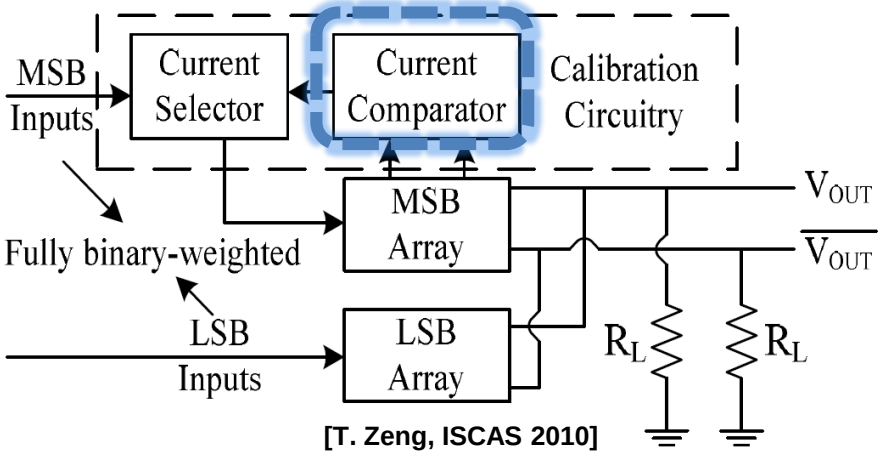
Analog centric



[T. Chen, JSSC 2007]

diagram of SSPA calibration technique

Analog centric



[T. Zeng, ISCAS 2010]

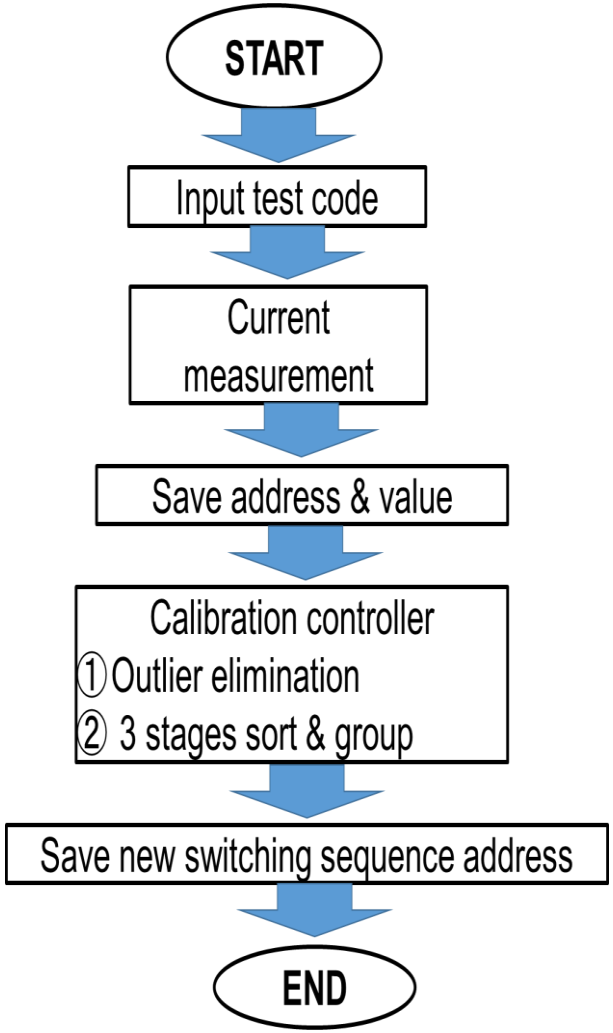
Fig.4 Block diagram of complete-folding calibration technique

Published Calibration Circuit Comparison

Technique	Advantages	Drawbacks
Self calibration [JSSC 2003] [14-b 100MHz] [1]	• High precision calibration	• Require high precision calibration ADC
SSPA [JSSC 2007] [14-b 200MHz] [2]	• Minimum additional analog & digital circuit • Defect current source replacement • Improve INL	• No DNL improvement • Analog current comparator
Complete-folding [ISCAS 2010] [14-b] [3]	• Minimum additional analog & digital circuit • Improve INL & DNL • Low voltage	▪ Analog current comparator

Proposed Calibration

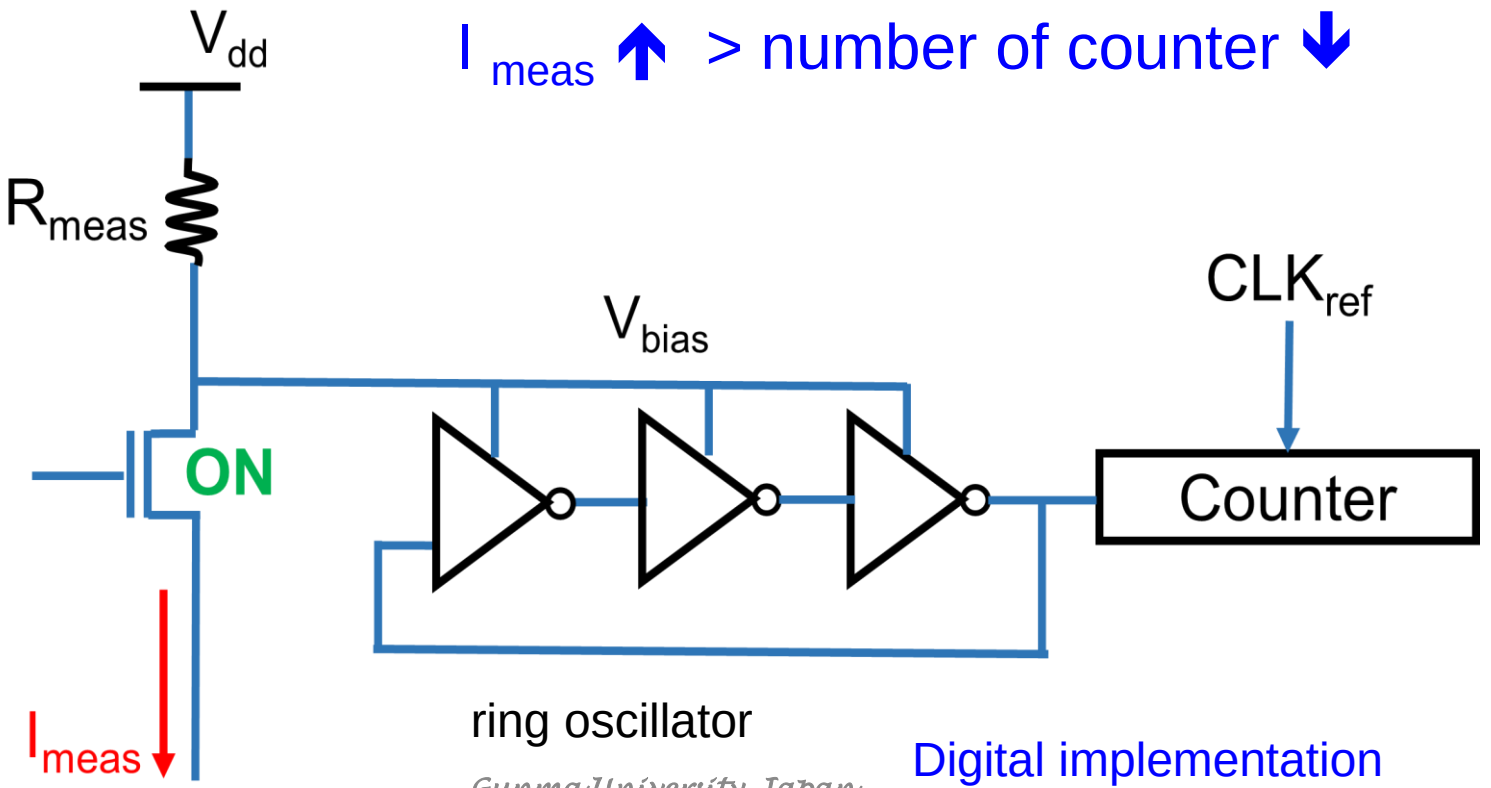
- Foreground Calibration
- Measure each current source
- Saving its value in memory (RAM).
- Calibration controller
  - Outlier elimination
  - 3-stage sort & group
- Obtained switching sequence is stored in look-up-table based decoder.
- Use during normal conversion operation.



Current Measurement Circuit

Only need order of current values.

Which current source is the largest,
the second largest, …, the smallest ?

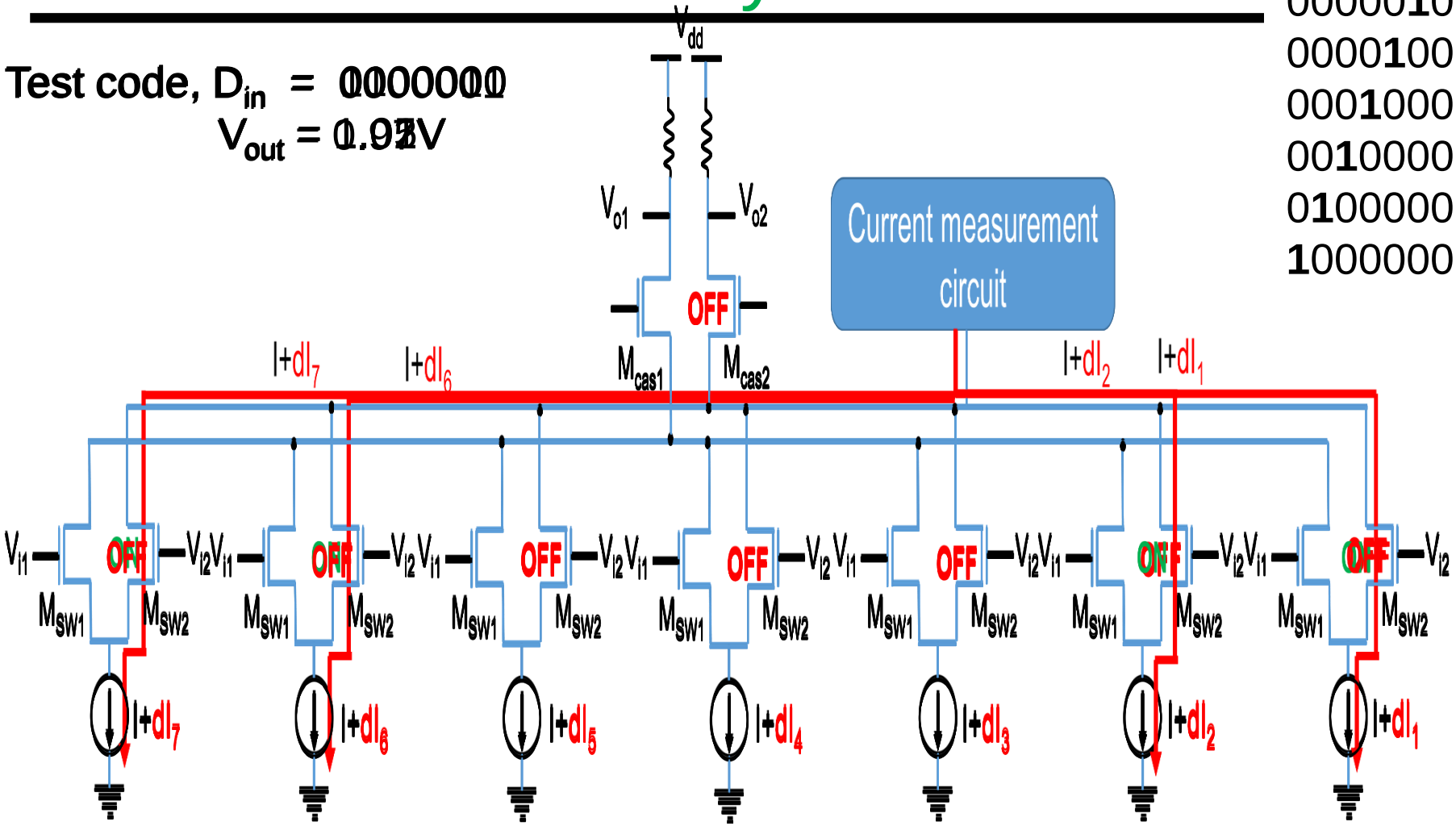


Digital implementation

Unit Current Measurement of Unary DAC

Test code:
0000001
0000010
0000100
0001000
0010000
0100000
1000000

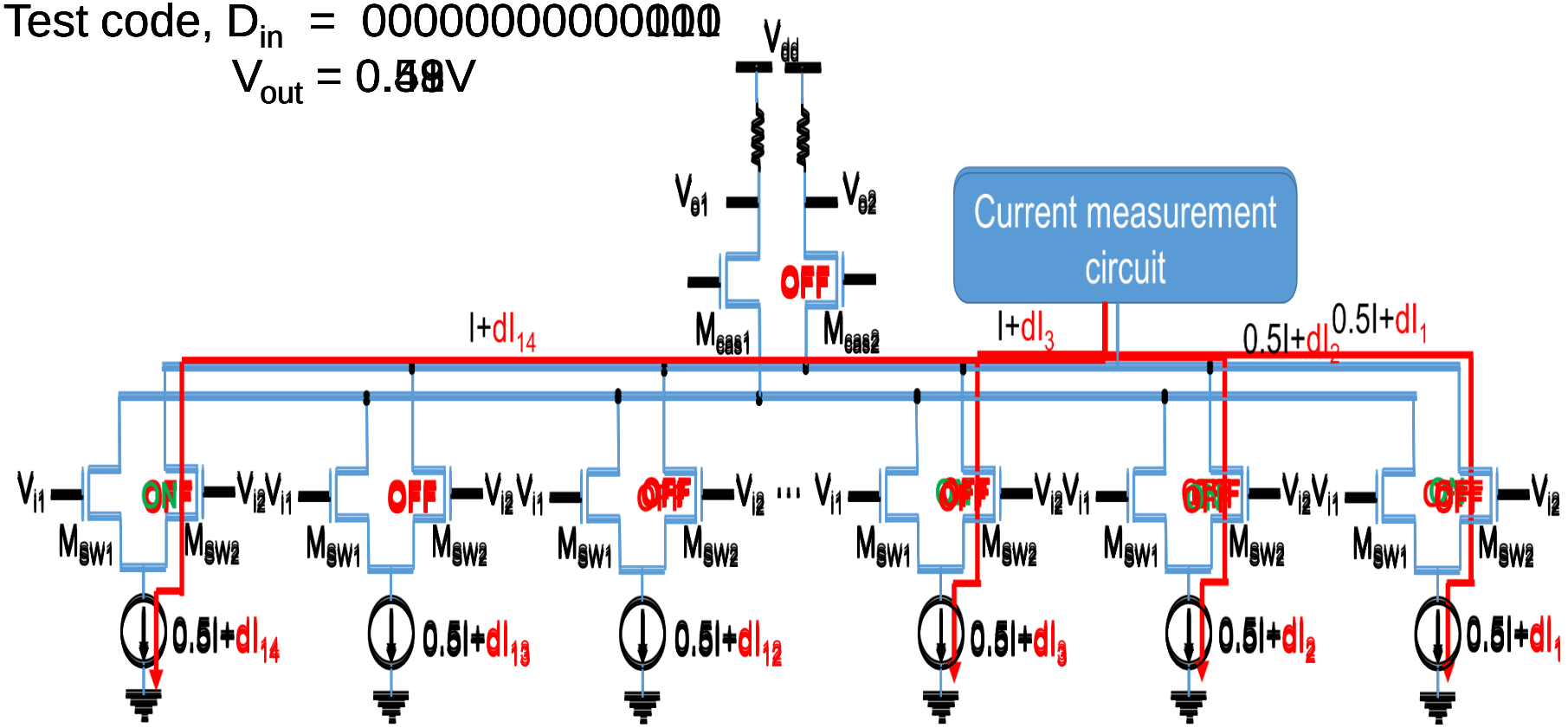
Test code, D_{in} = 0000001
V_{out} = 1.92V



Unit Current Measurement of Half-Unary DAC

Test code, D_{in} = 0000000000000

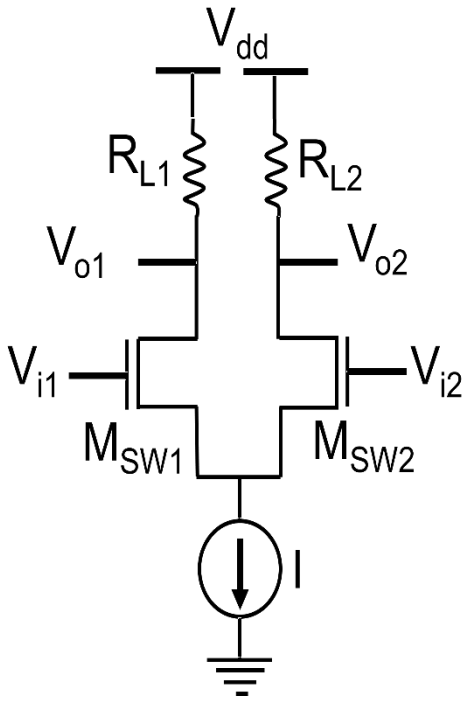
V_{out} = 0.5V



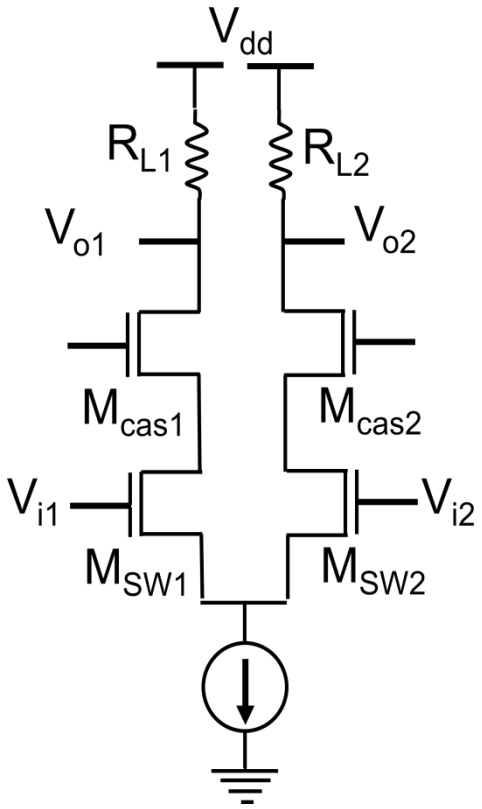
- No additional analog circuit (switches or routing).
- Only add digital circuit for switch control

Current Source & Current Switch

- Basic



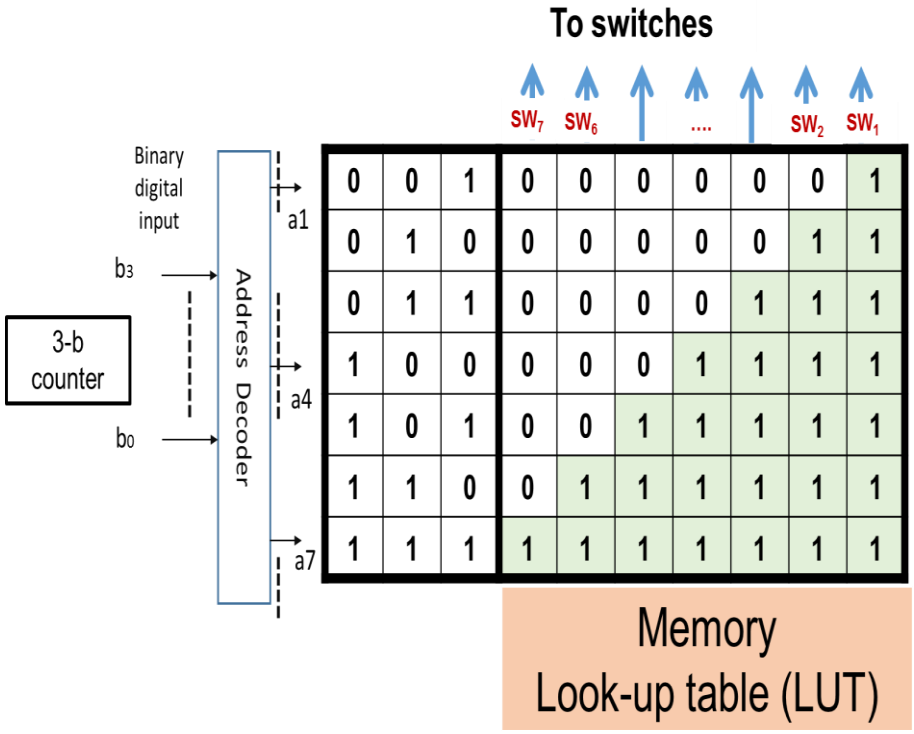
- Cascode



➔ **Reduce code-dependent load variation ☺ !!!**

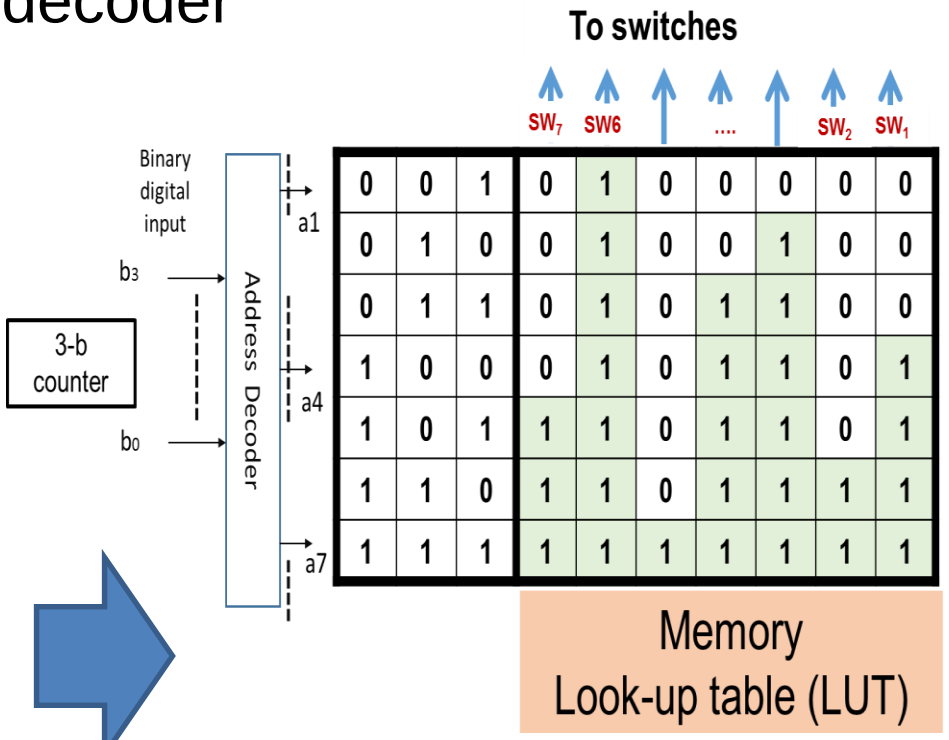
Look Up Table-based Decoder

Binary-to-thermometer decoder



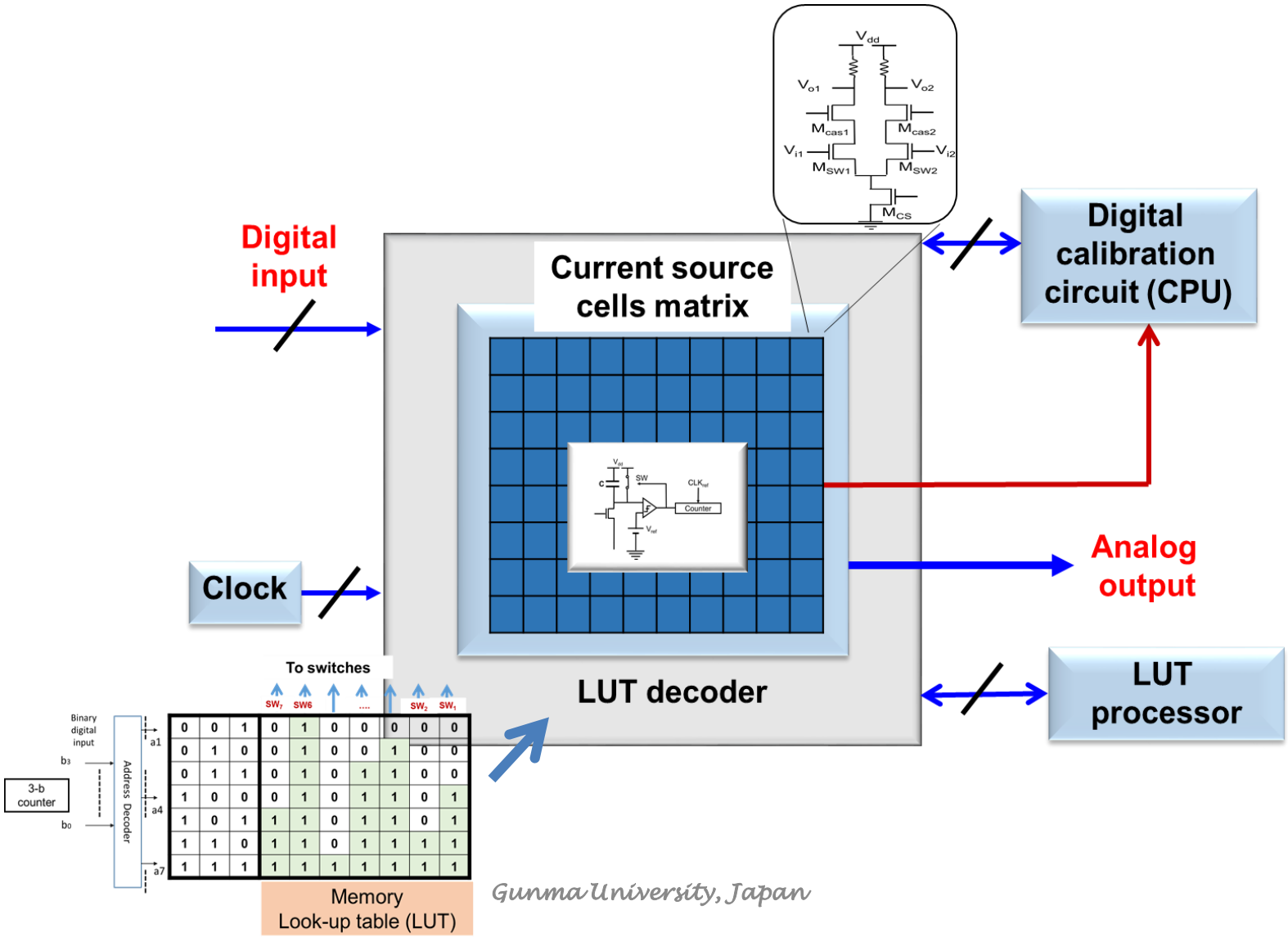
For conventional unary DAC

Binary-to-[stored-switching-sequence-code] decoder



For proposed half-unary DAC

Whole DAC Block Diagram



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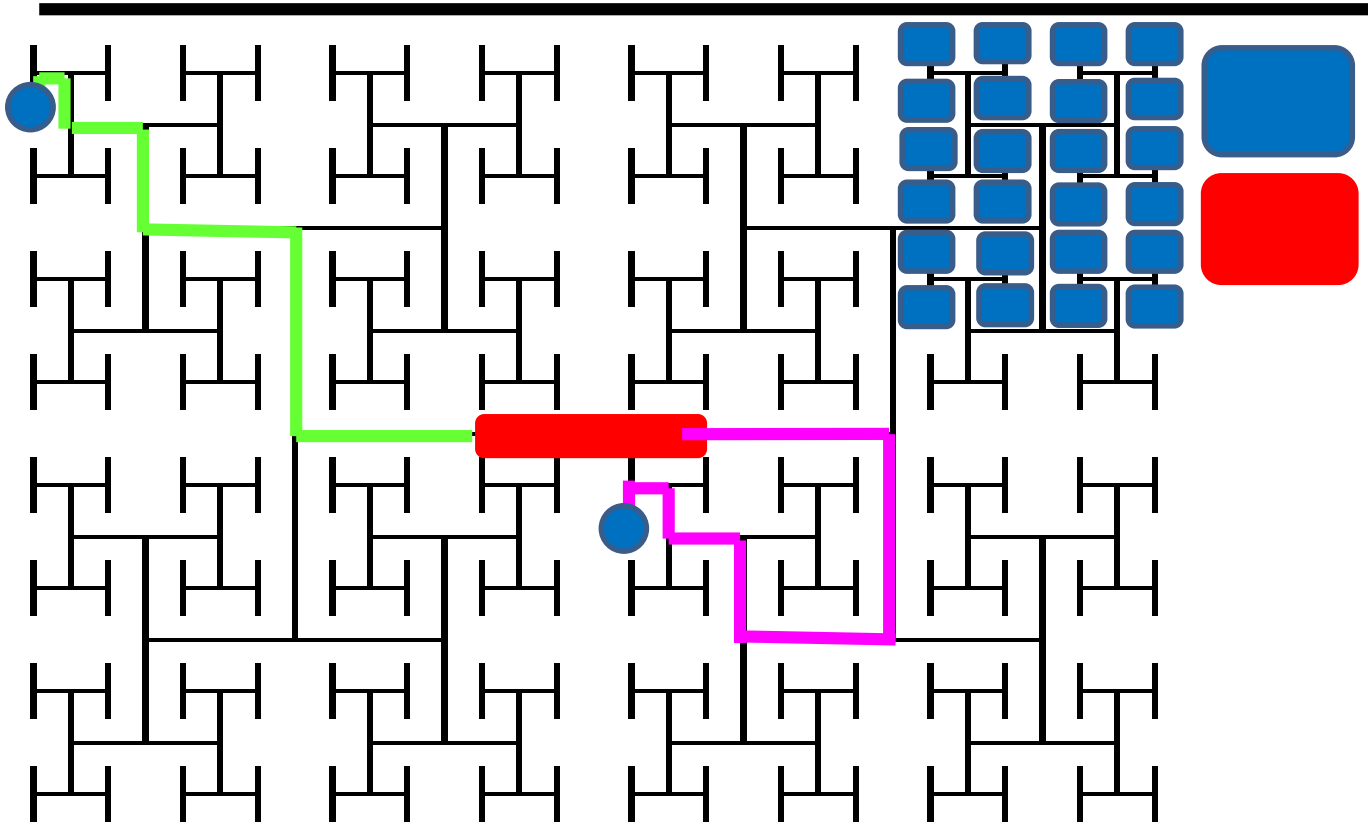
Layout of Current Cells

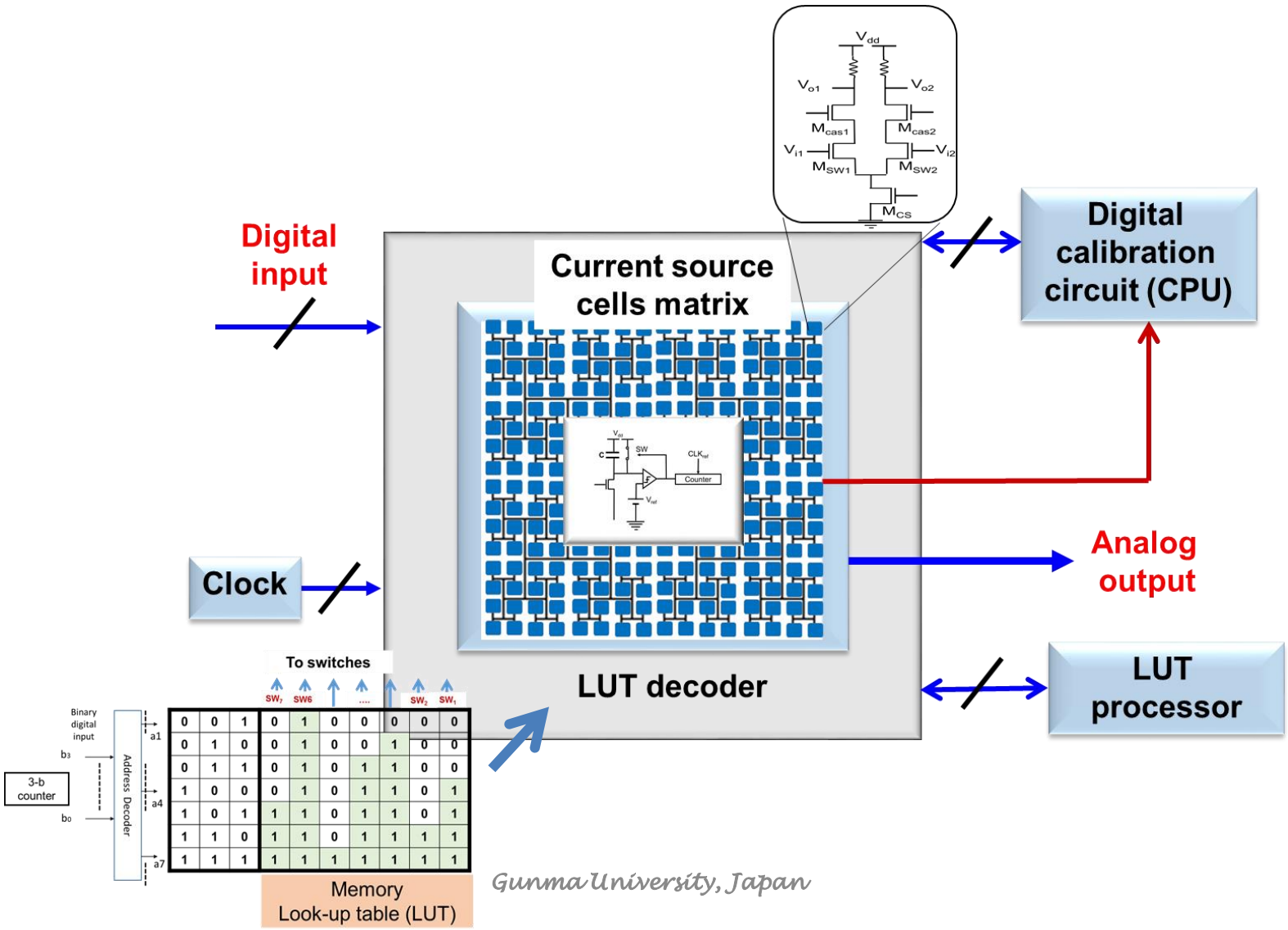


- Current cells (current sources & switches)
- Load resistor

For every cell, equal length of interconnection to load resistor.

➡ Minimum timing skew ☺!!!

Floor Plan of Whole DAC



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MATLAB simulation

- Case of unary DAC
- Case of half-unary w/o additional current sources
- Case of half-unary w/ additional current sources

- Simulation condition

  Fin = 102.4MHz, Fs = 819.2MHz

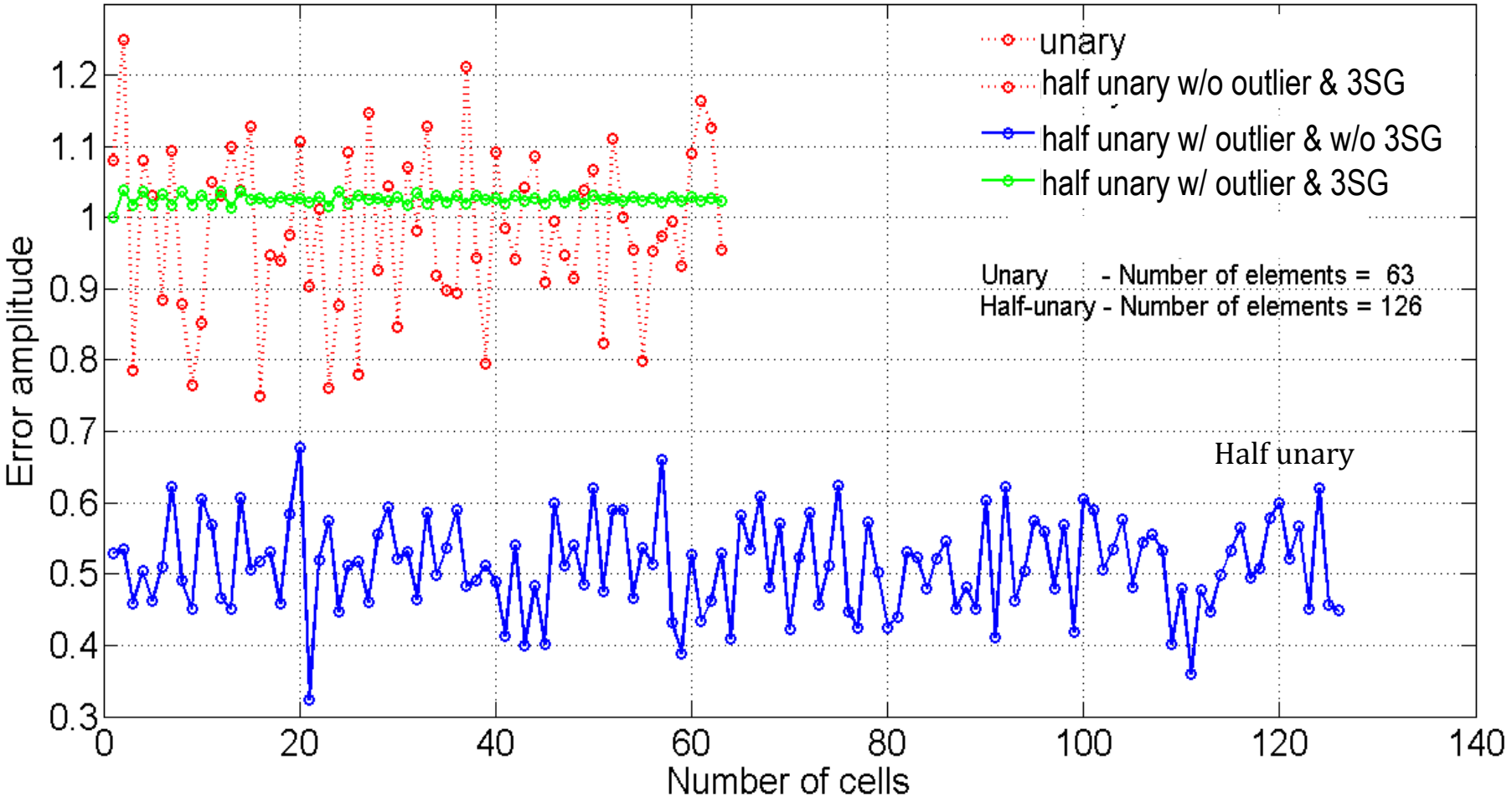
  fft = 32768 point

  Error range = [-0.25 ~0.25]

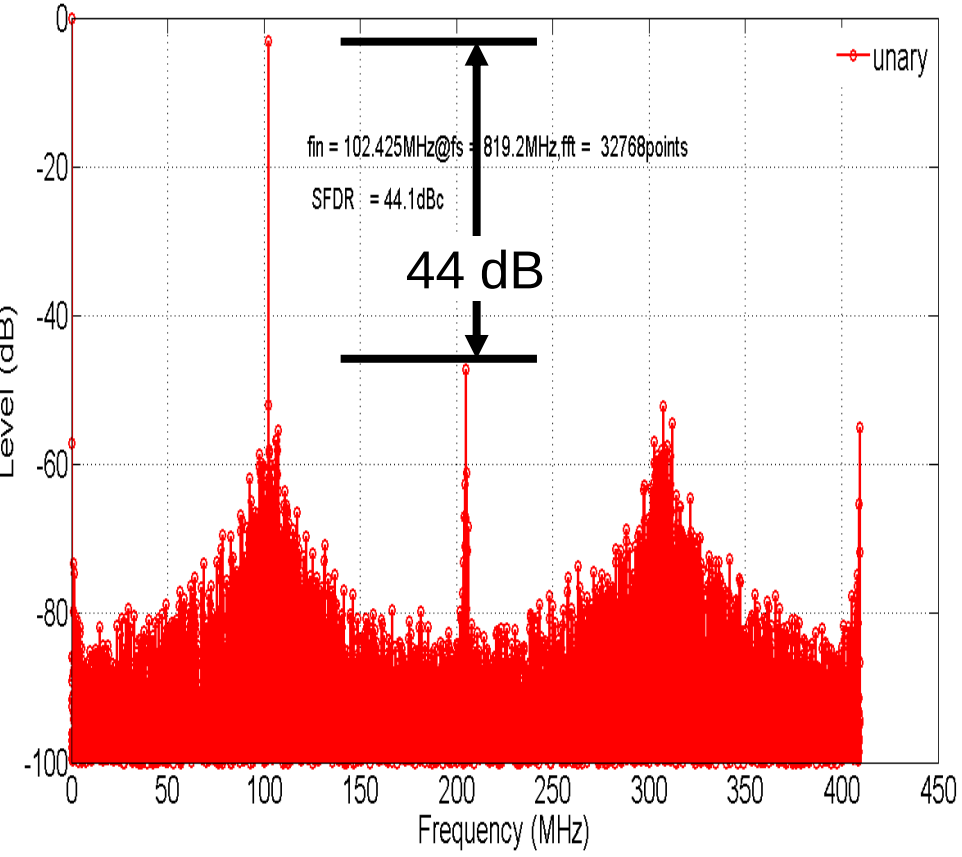
  Unary = 63 & 100 Half-unary = 126 & 196

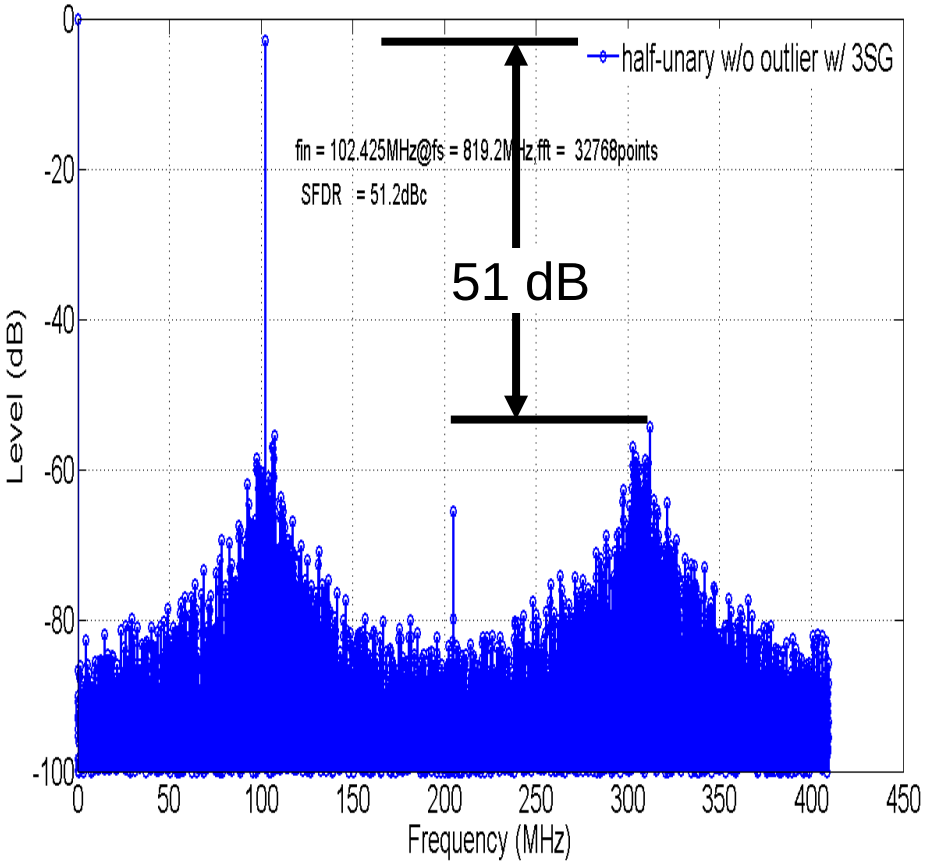
  Ideal SFDR = 51.3 dB

Simulation result
Error distribution w/o outlier



Simulation result (half-unary w/o outlier w/ 3SG)

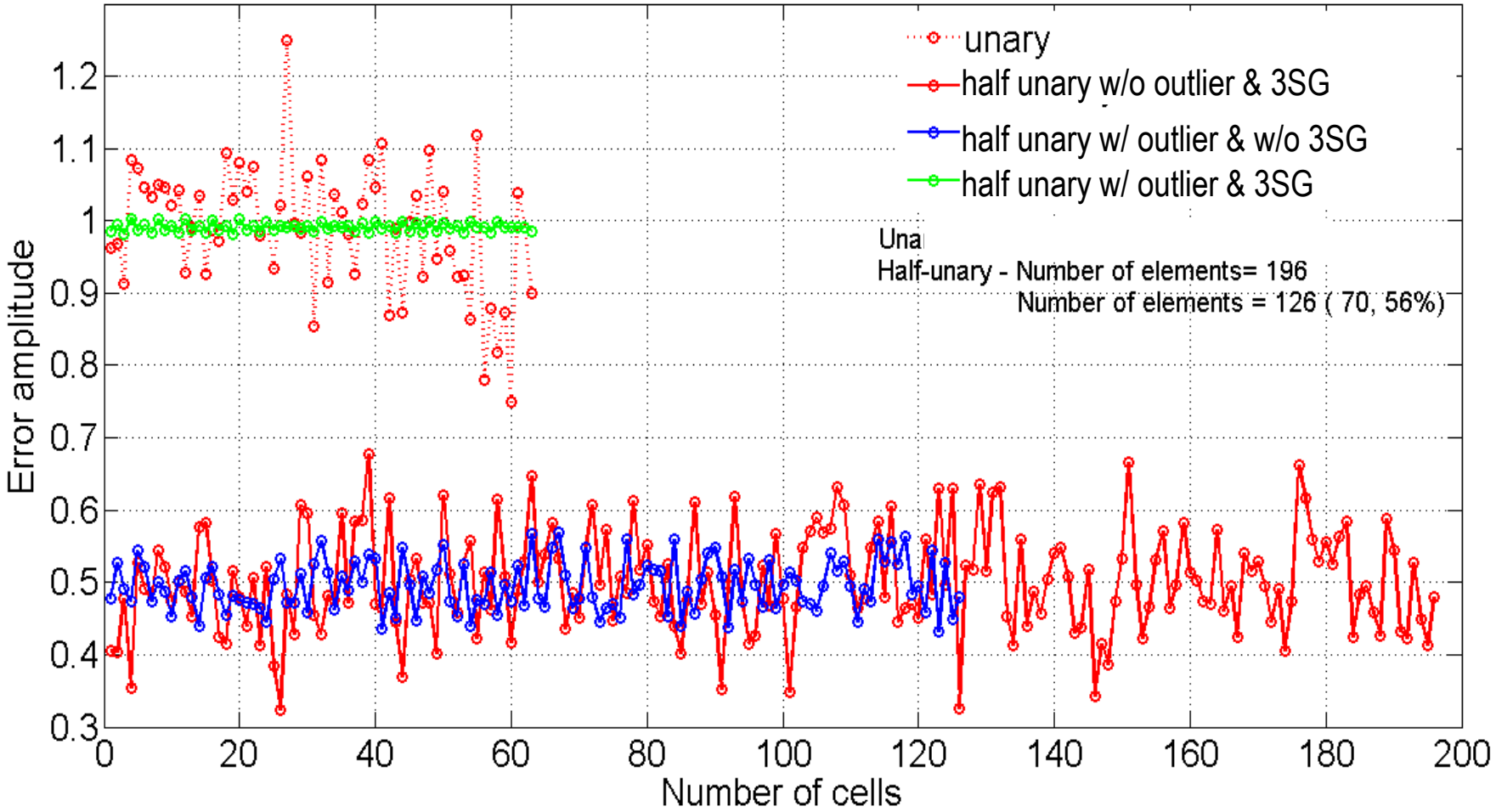




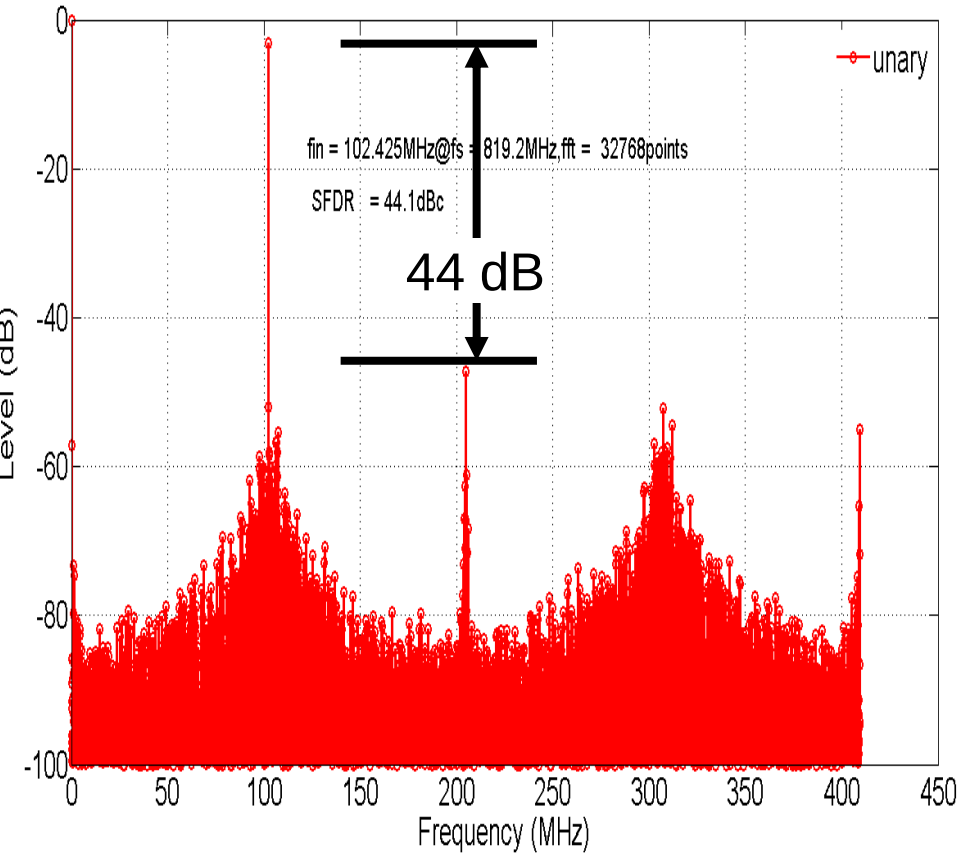
Unary = 44 dB Half-unary w/o outlier & w/ 3SG = 51dB

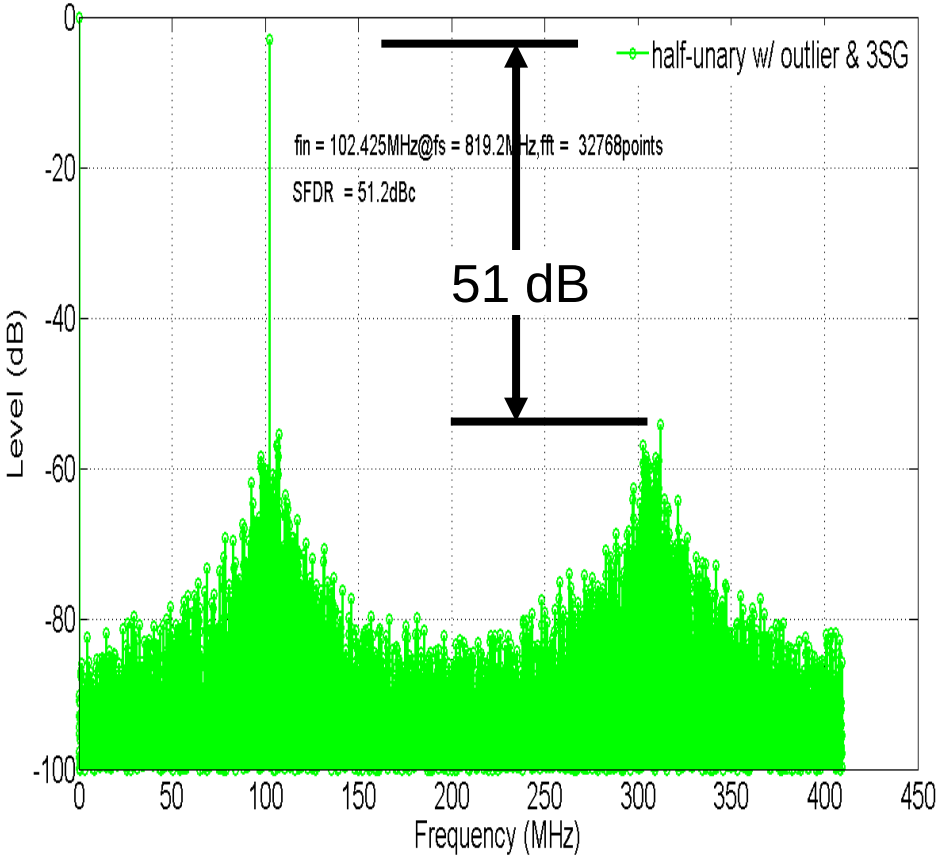
→ +7 dB compared to unary

Simulation result
Error distribution w/ outlier



Simulation result (half-unary w/ outlier & 3SG)





Unary = 44 dB Half-unary w/ outlier & 3SG = 51dB

→ **+7 dB compared to unary**

Summary

Simulation condition

Fin = 102.4MHz, Fs = 819.2MHz

fft = 32768 point

Error range = [-0.25 ~0.25]

Unary = 63 Half-unary = 126 & 196

Architecture	SFDR, dBc Ideal = 51.3 dB	Compared to average Compared to unary
Unary	45 dB	-
Half-unary + 3SG	46 - 51 dB	+5 dB + 6 dB
Half-unary+ outlier+3SG	49 – 51 dB	+2 dB +6 dB

Calibration Technique Comparison

Technique	Advantages	Drawbacks
Self calibration [JSSC 2003] [14-b 100MHz] [1]	• High precision calibration	• Require high precision calibration ADC
SSPA [JSSC 2007] [14-b 200MHz] [2]	• Minimum additional analog & digital circuit • Defect current source replacement • Improve INL	• No DNL improvement • Analog current comparator
Complete-folding [ISCAS 2010] [14-b] [3]	• Minimum additional analog & digital circuit • Improve INL & DNL • Low voltage	▪ Analog current comparator
This work	• Digital centric • More INL improvement	• Twice or more current cells

Outline

- Introduction
- Problem Statement
- Proposed Techniques
  - Half-Unary Current-Steering DAC
  - Outlier Elimination
  - Current Source Sorting
  - Circuit
  - Layout
- Simulation Result
- Conclusion

Conclusion

- High SFDR current-steering DAC
  for communication application with fine digital CMOS

- For DAC static linearity improvement
  ① Half-unary DAC architecture
  ② Current source outlier elimination
  ③ 3-stage sort & group algorithm for current sources
  ➡ Performed MATLAB simulation
- For DAC dynamic linearity improvement
  ① Well-balanced layout of current cells
  for interconnection R, C skew minimization.

Reference

Calibration (sort & group)

[1] Y. Cong and R. Geiger, “A 1.5-V 14-bit 100-MS/s self-calibrated DAC,” *IEEE J. Solid-State Circuits*, vol. 38, pp. 2051-2060, Dec. 2003.

[2] T. Chen and G. Gielen, “A 14-bit 200-MHz current-steering DAC with switching-sequence post-adjustment calibration,” *IEEE J. Solid-state Circuits*, vol. 42, No. 11, pp. 2386-2394, Nov. 2007. (SSPA)

[3] T. Zeng and D. Chen, “New Calibration Technique for Current-Steering DACs”, *Int. Symposium on Circuits Syst. (ISCAS),* pp. 573-576, 2010. (CF)

Switching sequence

[4] T. Miki, Y. Nakamura, M. Nakaya, S. Asai, Y. Akasaka, and Y. Horiba,“An 80-MHz 8-bit CMOS D/A converter,” *IEEE J. Solid-State Circuits*, vol. SSC-21, no. 12, pp. 983–988, Dec. 1986.

[5] Y. Cong and R. L. Geiger, “Switching sequence optimization for gradient error compensation in thermometer-decoded DAC arrays,” *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, Vol. 47, No. 7, pp. 585–595, Jul. 2000.

[6] K. C. Kuo and C. W. Wu, “Switching Sequence for Linear Gradient Error Compensation in the DAC Design”, *IEEE Trans. Circuits Syst. II: Express Briefs*, Vol. 58, No. 8, pp. 502-506, Aug. 2011.

Thank you very much
for your kindly attention

Q&A

Presentation:

Page 36:

Q : Why are you include the measurement circuit? Is it will increase another mismatch from the measurement circuit itself?

A : Measurement circuit is used to measure error of each current sources. It is digital implementation, so I don't think that it will produces another error.

Q: Did you believe that your measurement circuit is accurate enough to measure such a current with the small value?

A:Yes. Because our measurement circuit use counter that realize in digital circuit.

Q&A

Kenichi Okada sensei, Tokyo Institute Tech, Univ

Page 49:

Q: Why are you need calibration? DAC with the resolution less than 10 bit is not necessary to calibrate.

A: Actually, I plan these research to imply in segmented DAC as a MSB with resolution more than 10 bits.

Q:Did you think that current source is the main problem of the DAC?

A: Yes.

Advice: Actually, current source is not a main problem but the mismatch is related to current which is determined by the length L & width W of the current source.

Q&A

Kenichi Okada sensei, Tokyo Institute Tech, Univ

Page 49:

Q: What is assumption that you did in this analysis? What kind of error distribution? How about the standard deviation?

A: I used the random distribution but I don't really know about the standard deviation (show equation that being used)

Advice: If you used the flat distribution error, it will be a strange result.

Page10:

Q: Why you said that binary DAC has small chip area compared to unary?

A: I think, it is due to the number of current sources.

Advice: Binary & unary has almost the same of current source chip area but the different is L & W.

Q&A

Poster session:

Q: Why you don't use another algorithm such as DEM because it is more easy and require more less hardware implementation?

A: Before this, I had used DEM method such DWA & OES but I thought that by using such algorithm it can only be used for certain error type.

By using measurement circuit, I can obtained more accurate error value.

Q: How long the calibration time?

A: I don't know but that why calibration did in calibration mode. May be once during manufacturing.

Q:What the clock speed that you want to use for your calibration circuit?

A: I still don't think about that.

Q&A

Q: What is the SFDR means? How to relate between nonlinearity and SFDR ?

Q: What the meaning of 3-stages sort & group?

A: First sorting for combining the current source while 2^{nd} & 3^{rd} for switching sequence arrangement.