Gate Voltage Dependent 1/f Noise Variance Model in n-Channel MOSFETs

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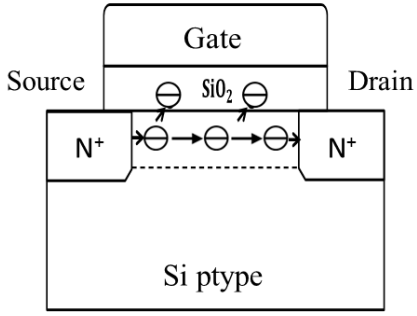
Outline of our Research

Research Purpose

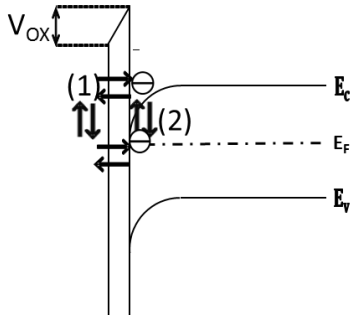
- **Development of 1/f noise variance model in MOSFETs**

Research Approach

1/f noise caused
by Mobility Fluctuation and
Interface Traps



from the Si to the gate oxide



between interface traps

Increase of
Oscillator Circuits Noises

SPICE2 type model

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① Interface Trap Number
② Mobility Fluctuation
③ Process Variation
④ Time & Temperature Degradation

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Proposed Model

Research Goal

- Present the model derivation
- Implementation on our SPICE3 (MDW-SPICE) circuit simulator

Research Results

SPICE2 Model

$$S_{I_D} = \frac{KF \cdot {I_{ds}}^{AF}}{C_{OX} {L_{eff}}^2 f^{EF}}$$

Hooge's 1/f Model : Mobility Fluctuation Model

$$S_{I_D} = \frac{\alpha_H \cdot \mu_{eff} \cdot 2kT \cdot I_D}{f L^2}$$

Comparison with These Models

→ Variability model incorporated in mobility fluctuations

$$\boldsymbol{KF = C_{OX} \cdot \mu_{eff} \cdot 2 \cdot k \cdot T \cdot \alpha_{H_{nominal}} \cdot D \cdot e^{-(V_{gs}-V_{th})}}$$

Simulation and Measurement Results

Proposed model agreed with measurement results !