3-Stage Current Sorting Algorithm for Current-Steering DAC Linearity Improvement

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Outline

- Introduction
- Problem Statement
- Proposed Techniques
  - Half-Unary Current-Steering DAC
  - Current Source Sorting
  - Circuit & Layout
- Simulation Result
- Conclusion

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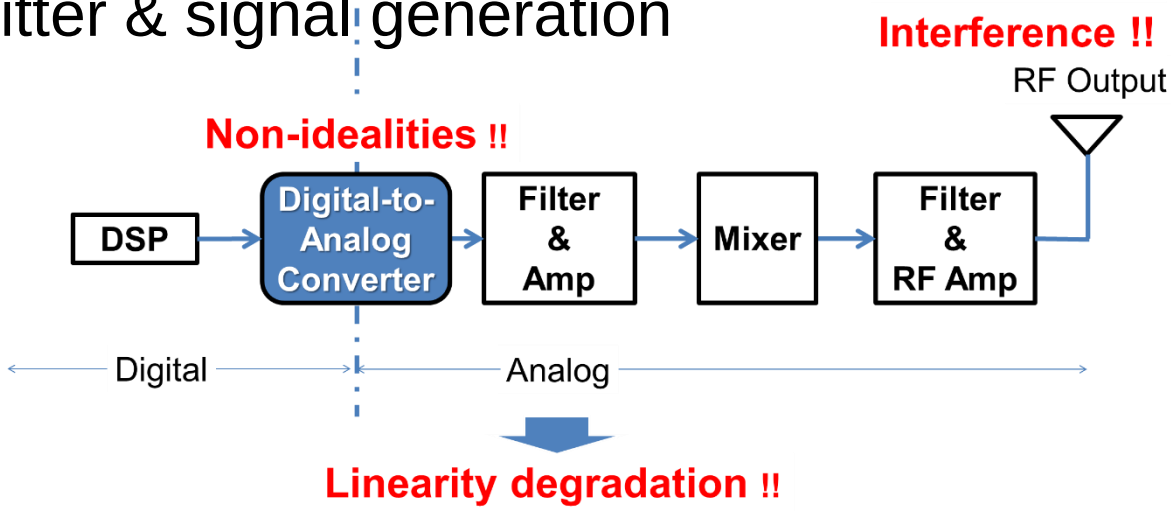
Introduction

- **Background**
  - Telecommunication devices
    - Mobile phones, wireless modems & avionics
    - **High-speed, high-accuracy**

      Digital-to-Analog Converter (DAC)

- **Problem**
- Transmitter & signal generation



Objective & Investigated Method

- **Objective**
  - High SFDR current-steering DAC for communication or signal generation application

    SFDR: Spurious Free Dynamic Range

    DAC: Digital-to-Analog Converter
- **Proposed method**
  - Current source mismatch effect reduction
    - ① Half-unary DAC architecture
    - ② Current source sorting

    ⇒ Static linearity improvement
  - Layout strategy

    ⇒ ③ Clock-tree-like layout of current sources & switches

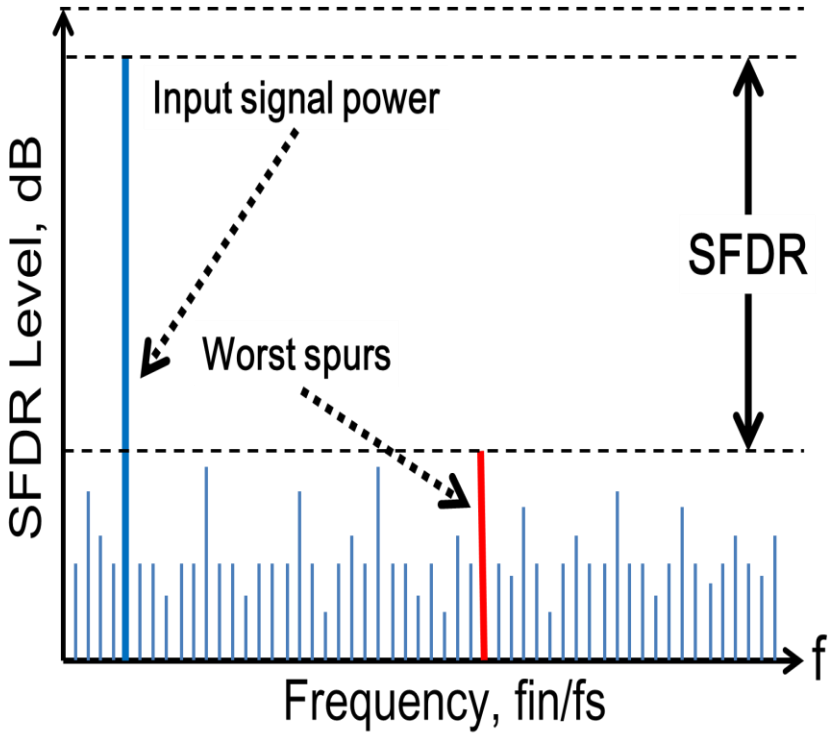
    Dynamic linearity improvement

SFDR – Spurious Free Dynamic Range

Spurious Free Dynamic Range (SFDR)

SFDR Degradation Sources

- Unit current source mismatches
  - ➔ Static nonlinearity
- Data-dependent output load variations
  - ➔ Dynamic nonlinearity



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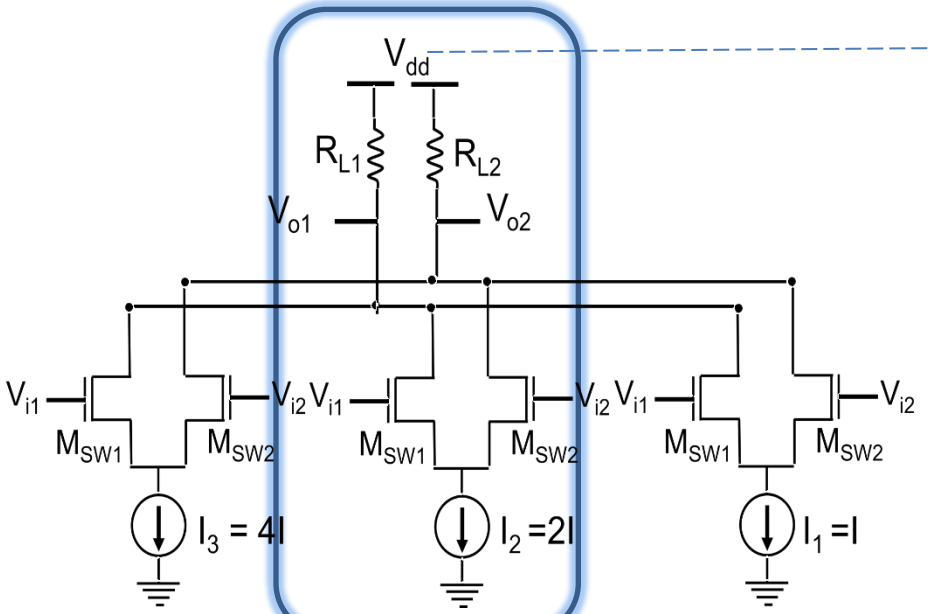
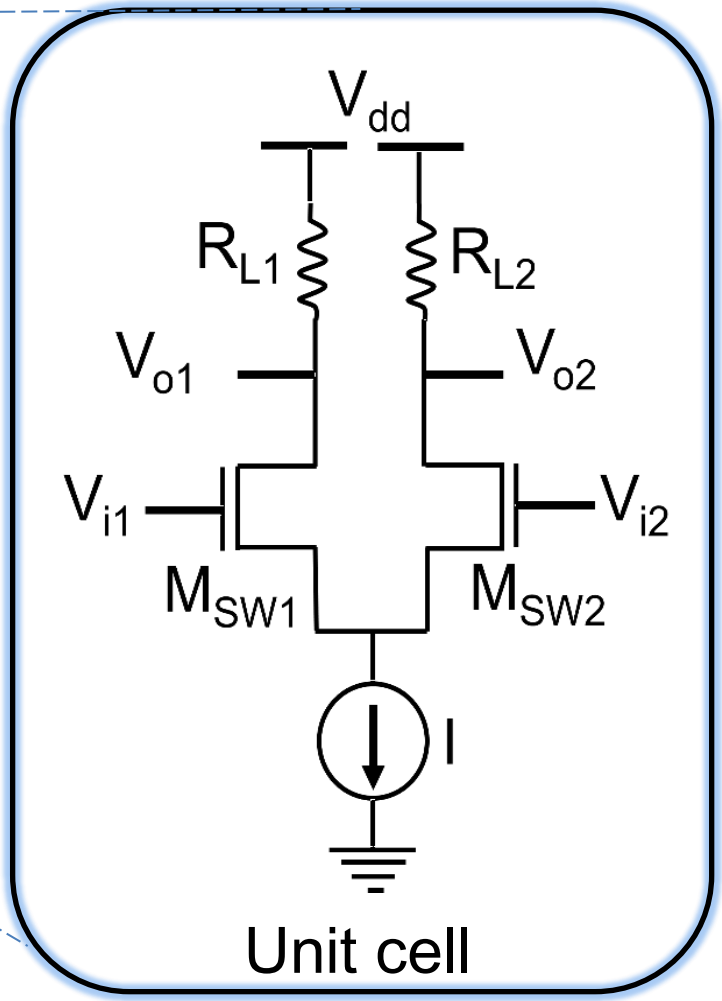
Current-Steering DAC

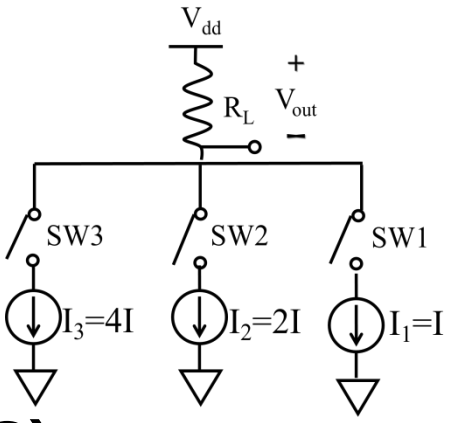




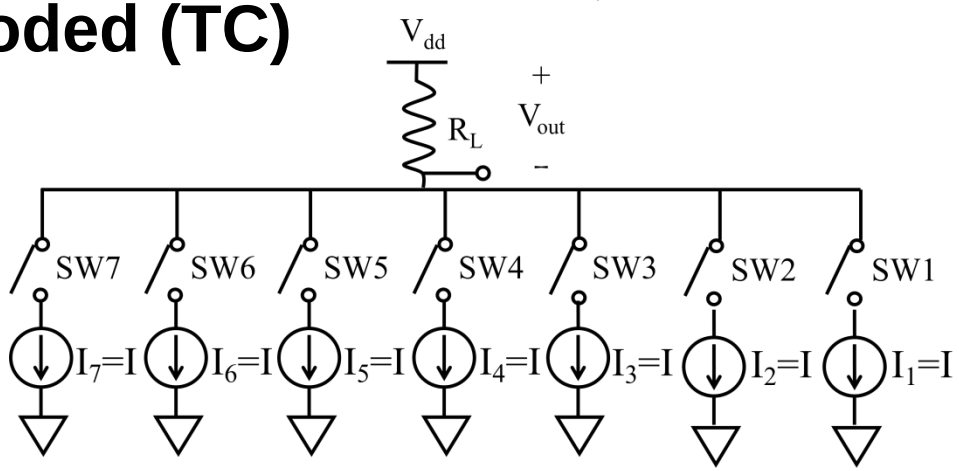
- High speed
- High resolution
- Small chip area

Binary versus Unary CS DAC

- **Binary**
  - Small silicon area ☺
  - High speed ☺
  - Large glitch energy ☹



- **Unary / Thermometer-coded (TC)**
  - Small glitch energy ☺
  - Redundancy ☺
  - Low speed ☹
  - Large silicon area ☹



→ Segmented for balanced performance !!! 😐

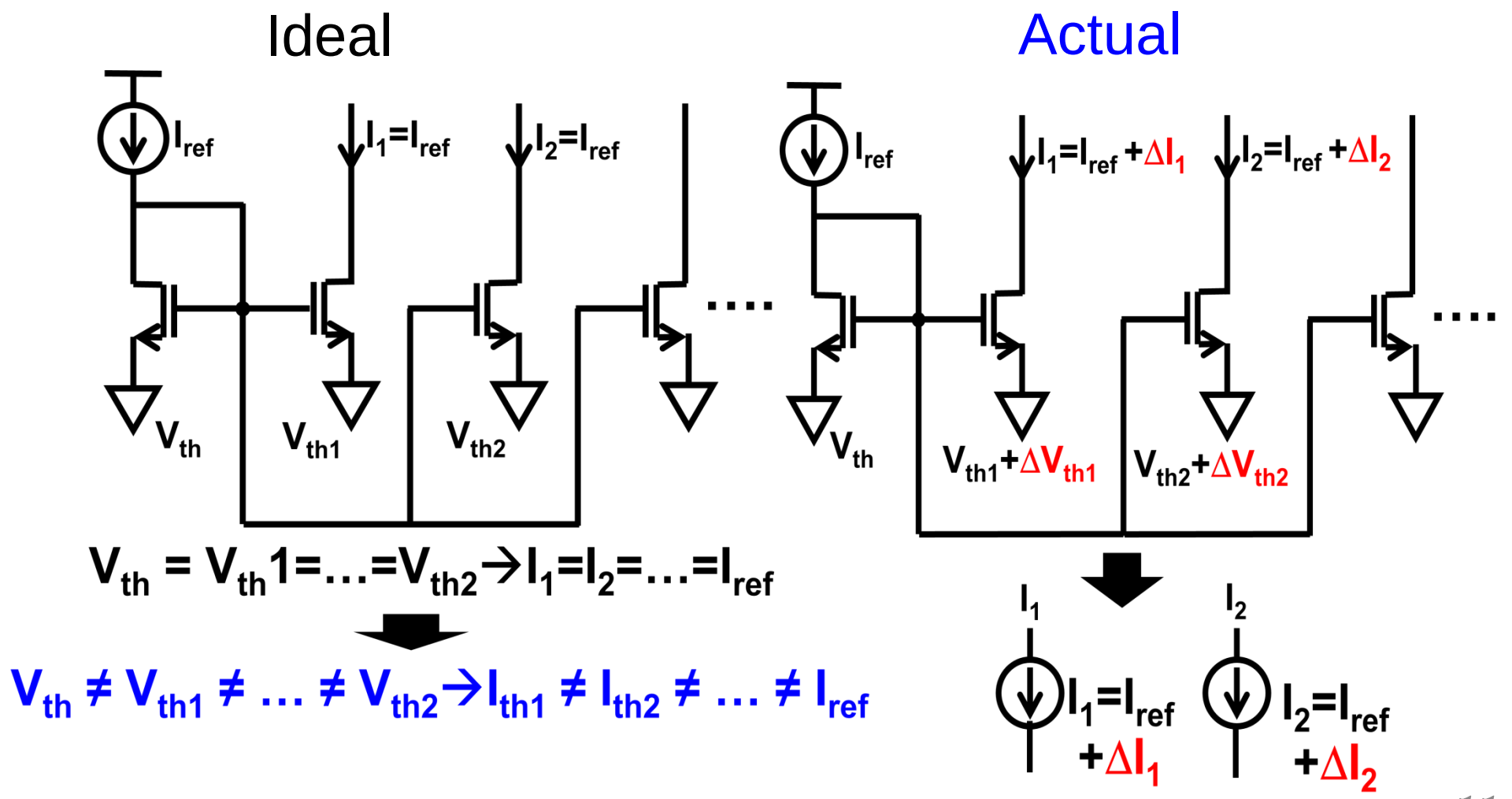
Current-steering DAC Limitation

- Transistor matching error
  - Amplitude errors - current sources
    - Dominant at low input frequency
  - Timing errors – switches
    - Dominant at high input frequency

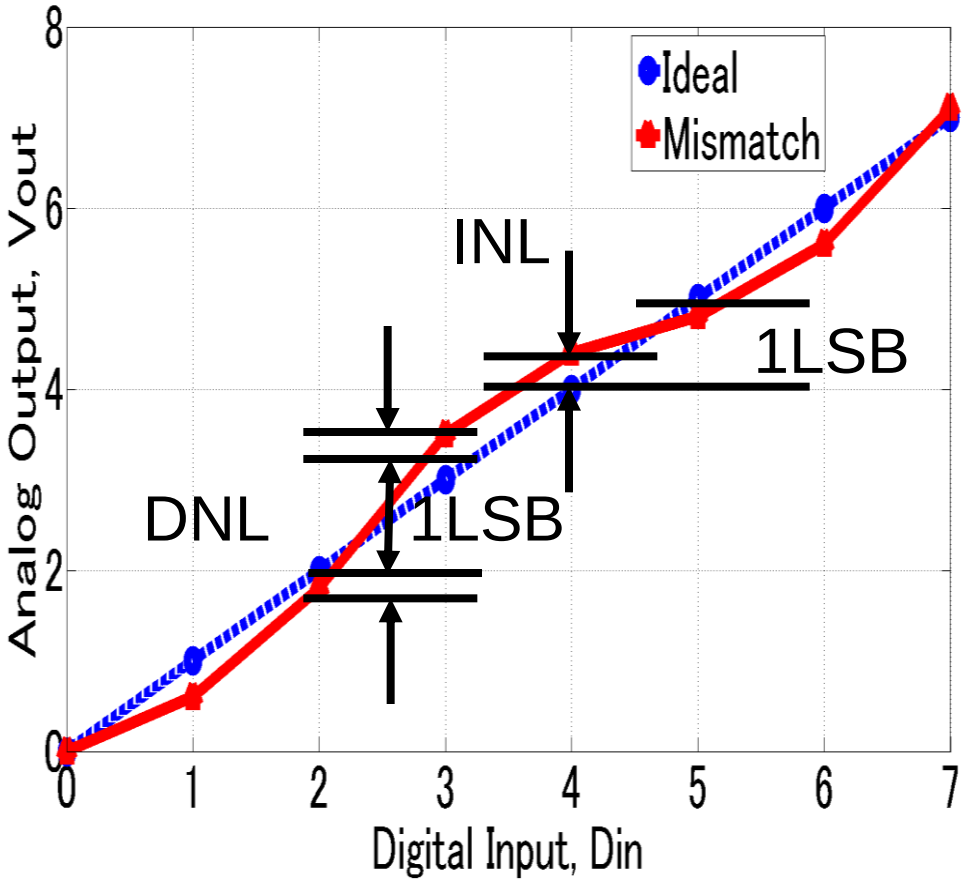
DAC static & dynamic non-linearity

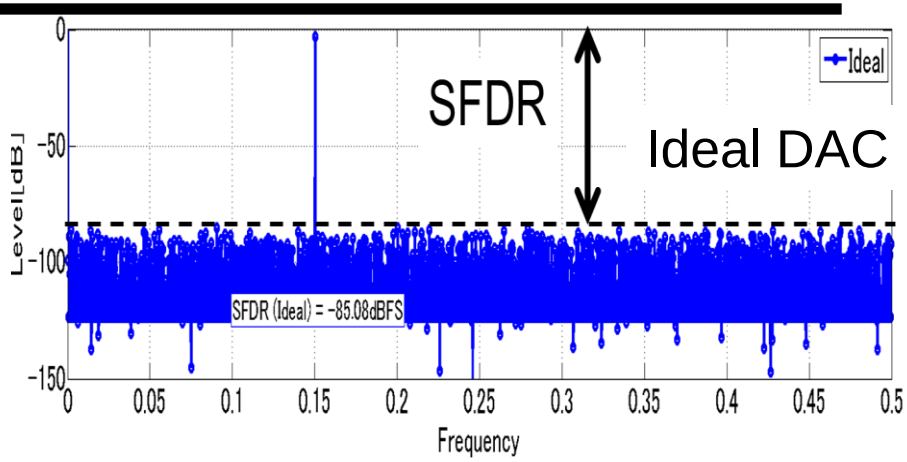
- Better transistor matching
  - large size ➔ Power loss ☹
  - Laid out close to each other ➔ Complicated ☹

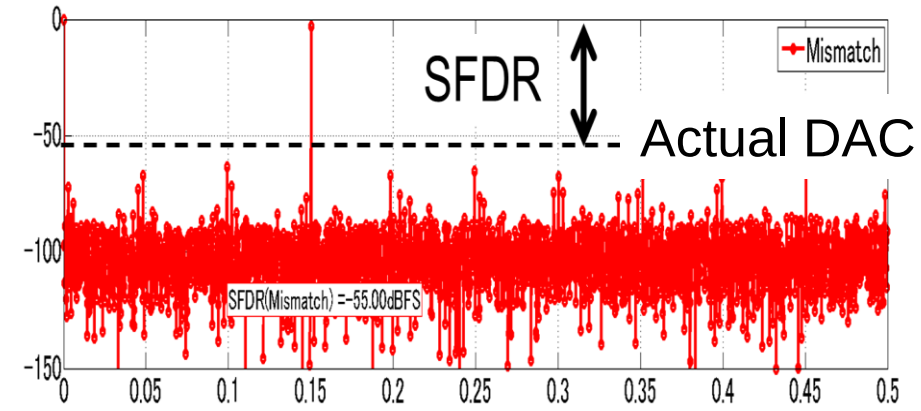
Current Source Mismatch (Amplitude)



Nonlinearity & SFDR degradation



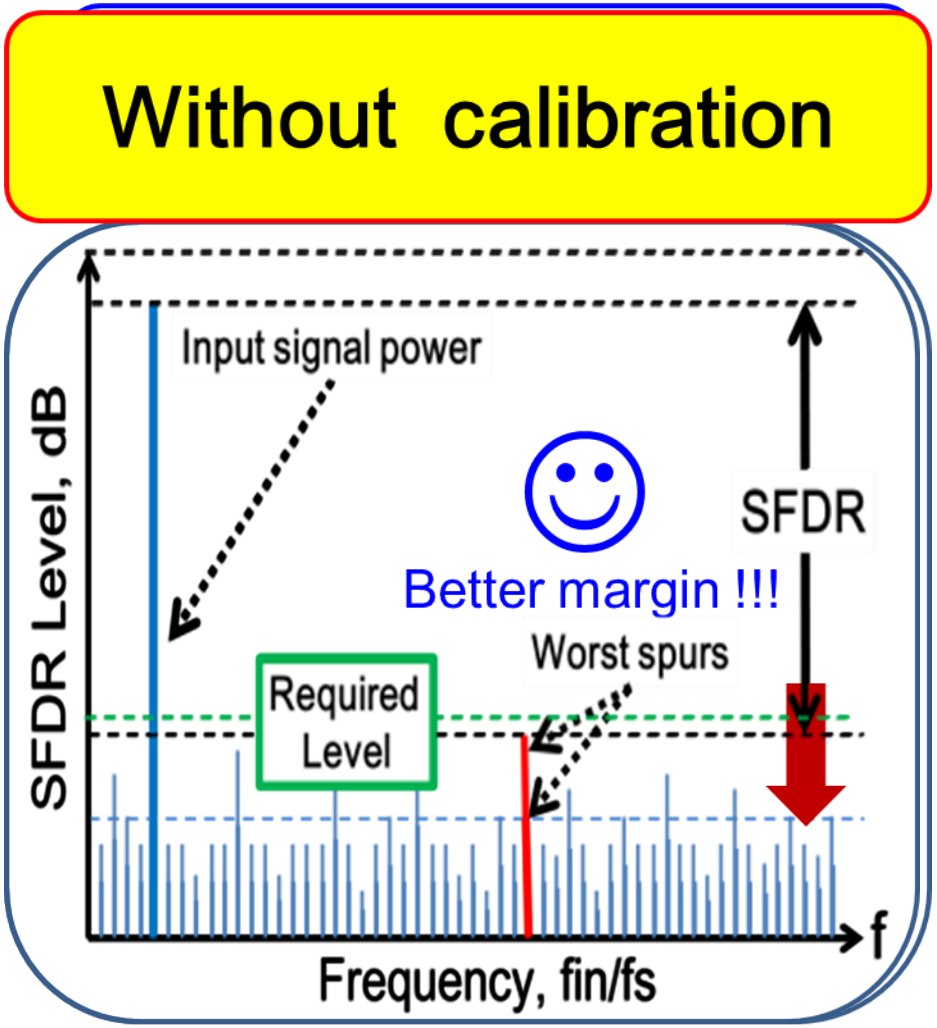




Current source mismatch
➔ DAC nonlinearity ☹

➔ SFDR degradation ☹

SFDR Improvement With Calibration



Design Approach

- **Analog**
  - Complex hardware
  - Not programmable
  - Costly

- **Digital**
  - Simple
  - Programmable
  - Low-cost

➔ **Digital rich approach**
for fine CMOS implementation

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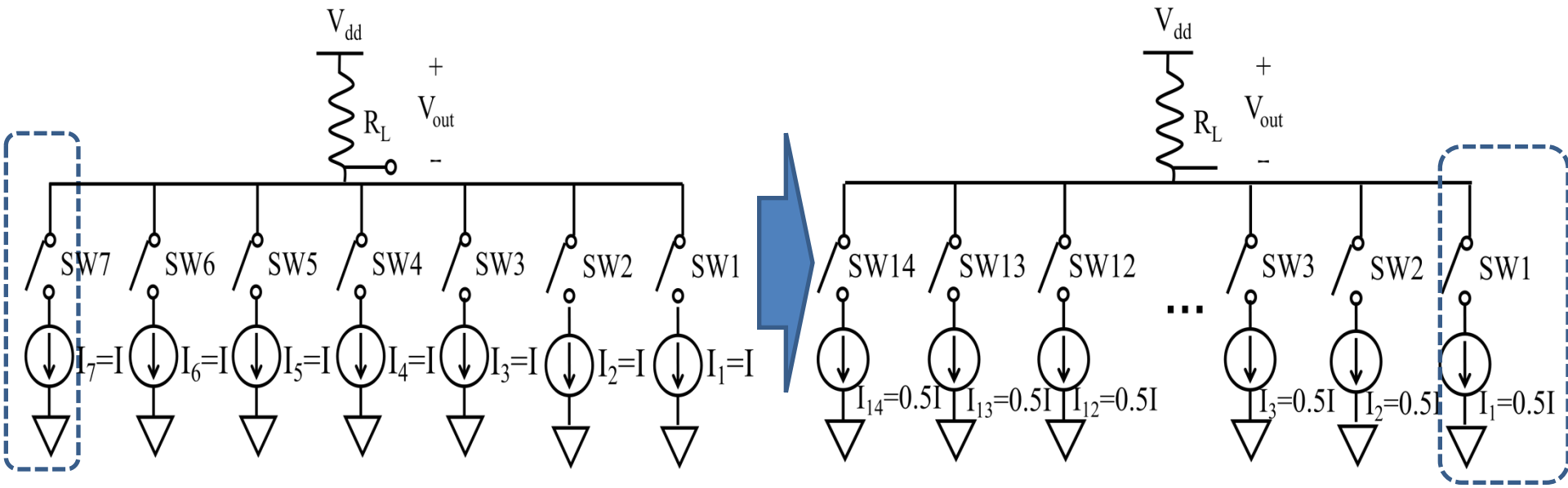
What is half-unary?

Unary

Half-unary

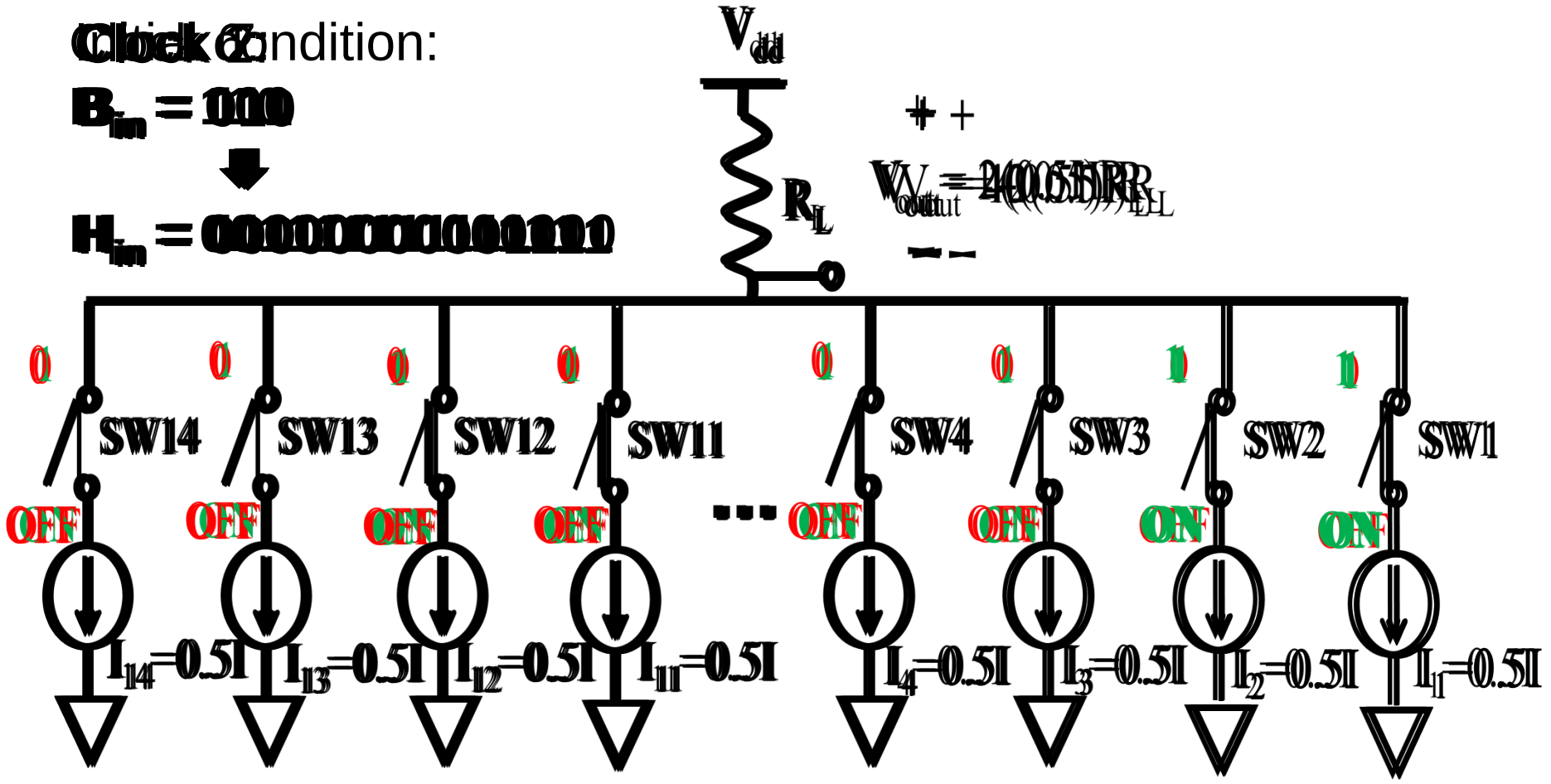


- Each current source cell = I

Each current source cell = 0.5I

- Pair of 0.5I & 0.5I for output of I

Half-unary current steering DAC



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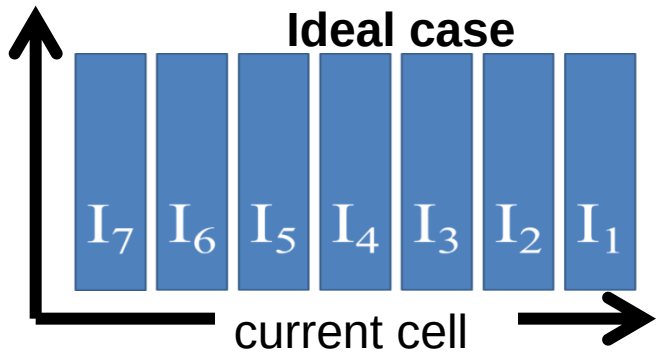
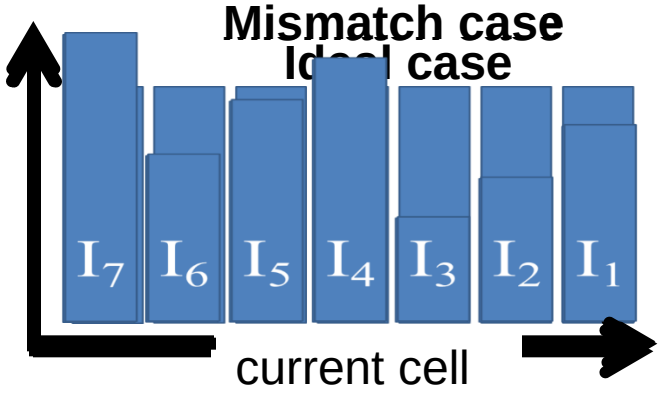
Unit Current Cell Switching Sequence

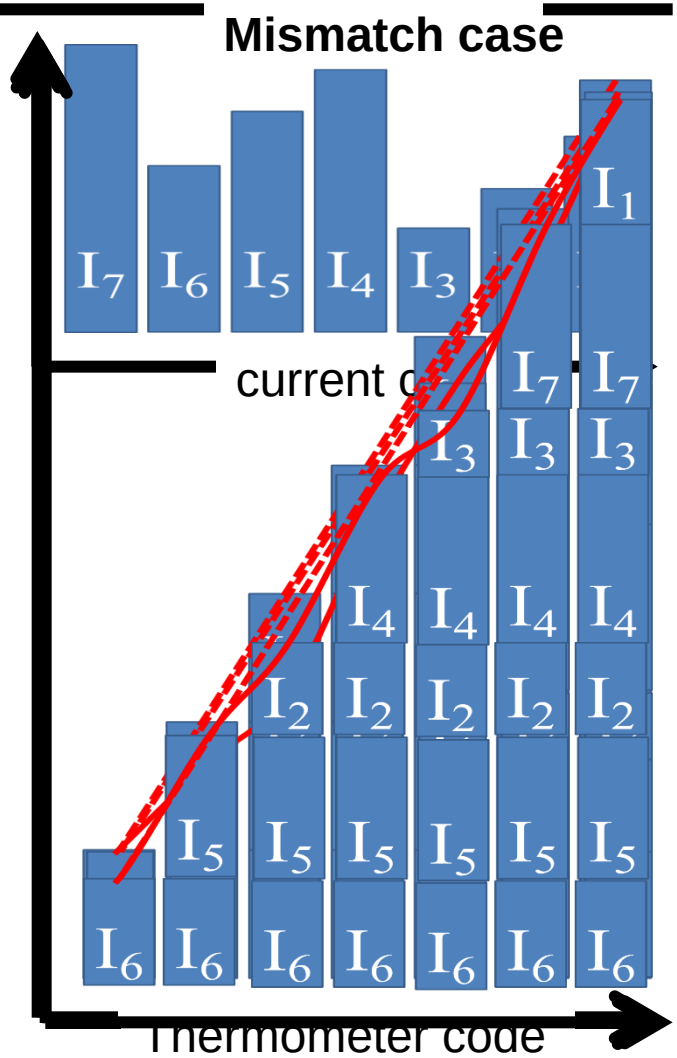


Process Variation

Switching sequence
➔ Integral nonlinearity improvement ☺

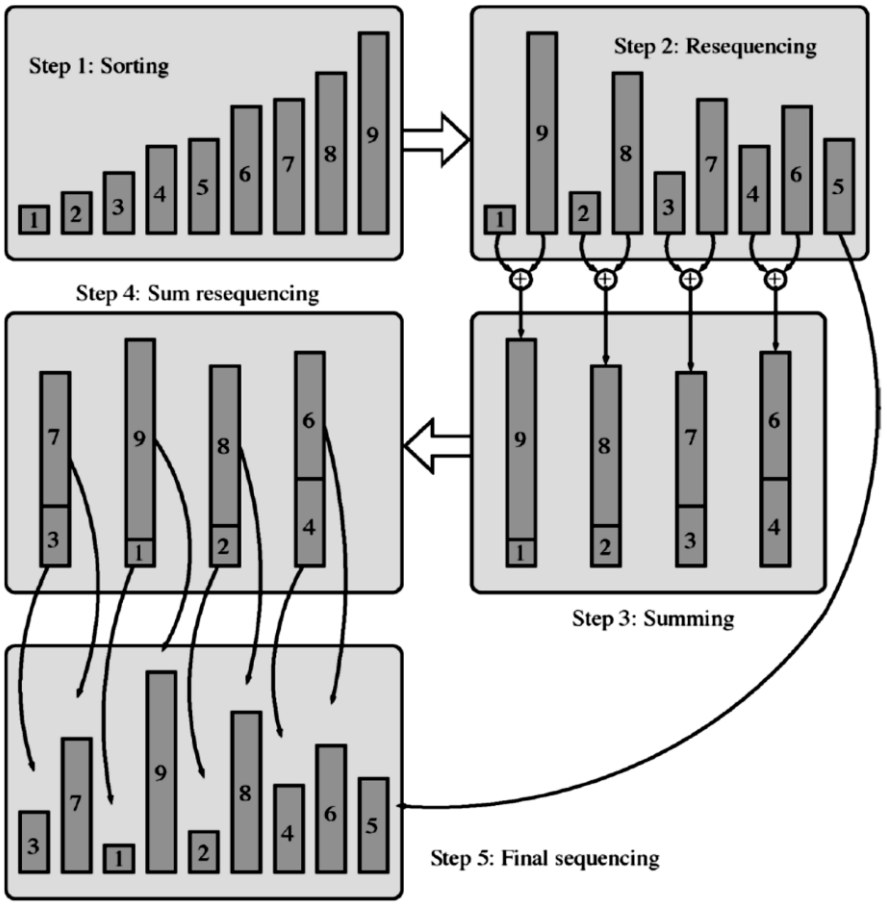


New Switching sequence

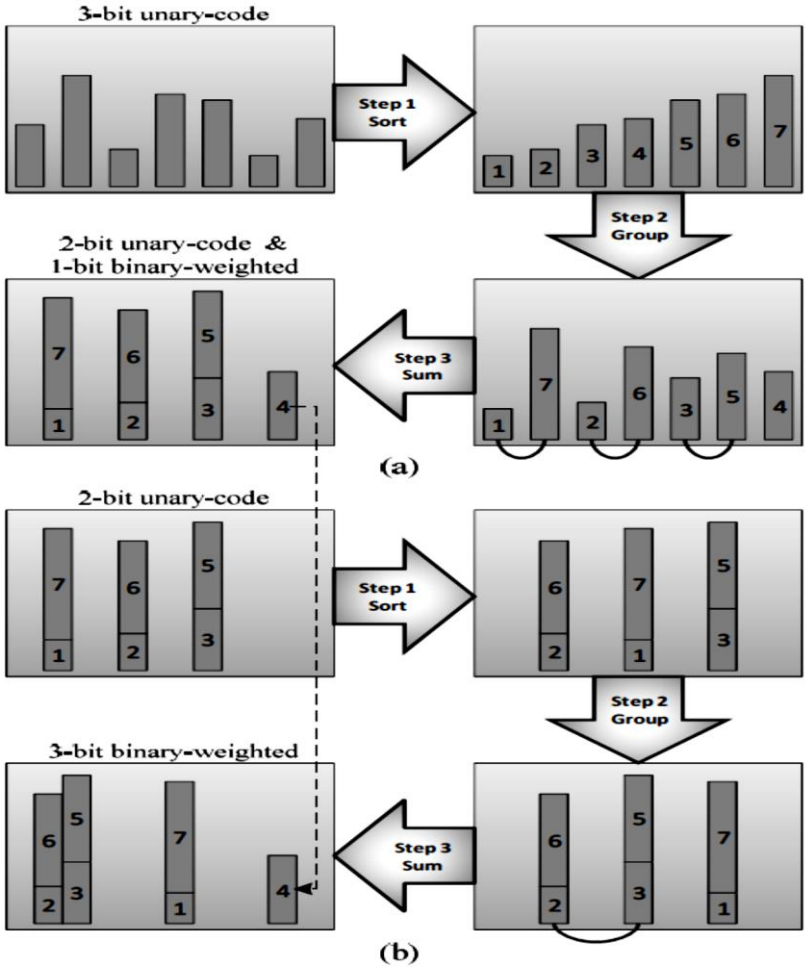


Published Current Sorting Procedures

T. Chen, JSSC (2007)

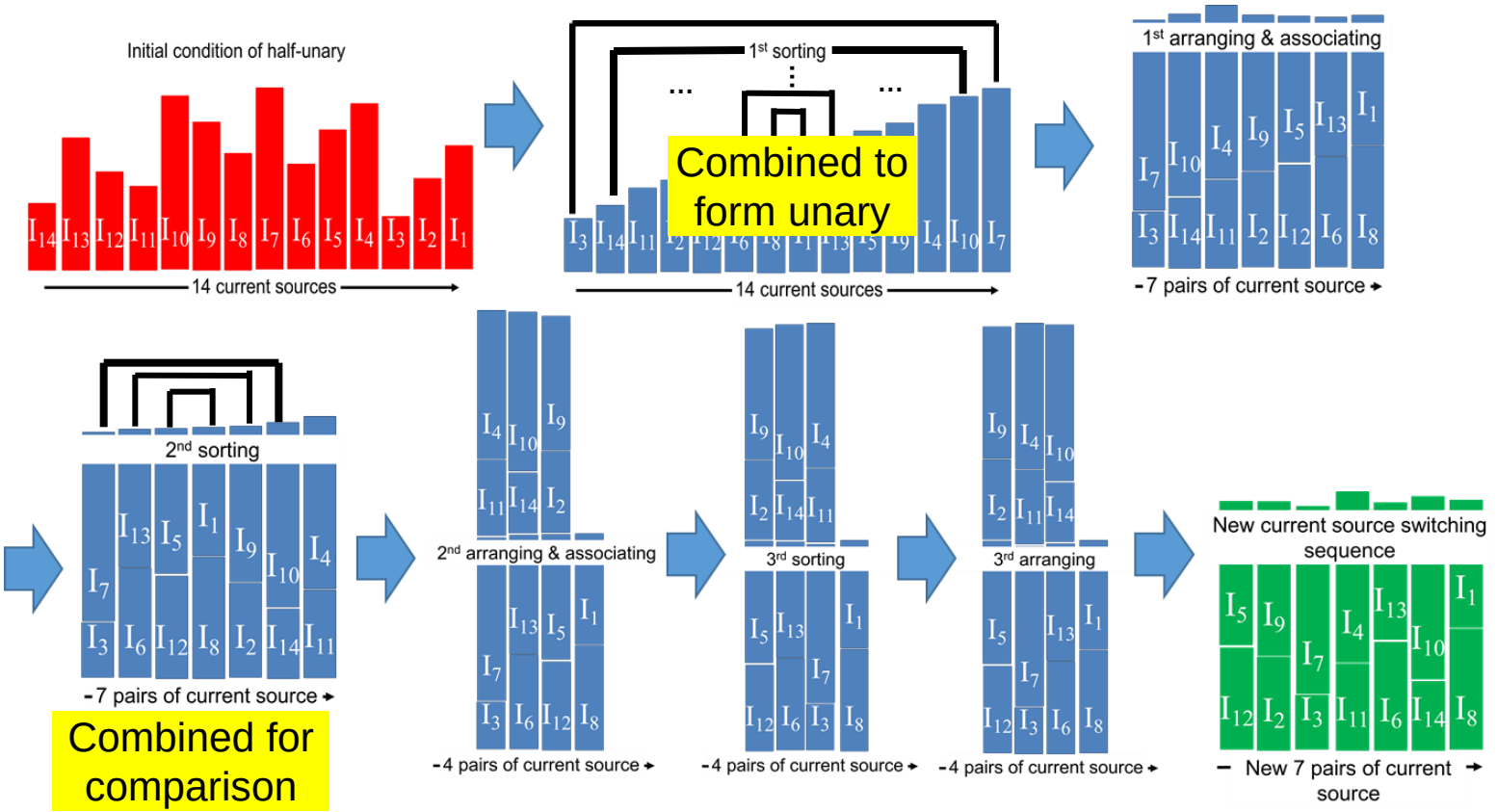


T. Zeng, ISCAS (2010)



CS – current source

3-stage Current Sorting Algorithm (3S-CS)



New switching sequence

➔ More linearity improvement ☺!!!

CS – current source

Current Sorting Techniques Comparison

Technique	Features	Advantages	Drawbacks
SSPA JSSC 2007 [2]	• 2-stage current sorting • Change switching sequence	• Improve INL only	• Require additional current sources
Complete-folding ISCAS 2010 [3]	• Convert unary to binary	• Improve INL & DNL	• Procedure steps increase by DAC resolution
This work	• 3-stage current sorting • Convert half-unary to unary • Change switching sequence	• Improve more INL & DNL • Less procedure steps compared to [3]	• Require twice current sources

SSPA –Switching sequence post-adjustment

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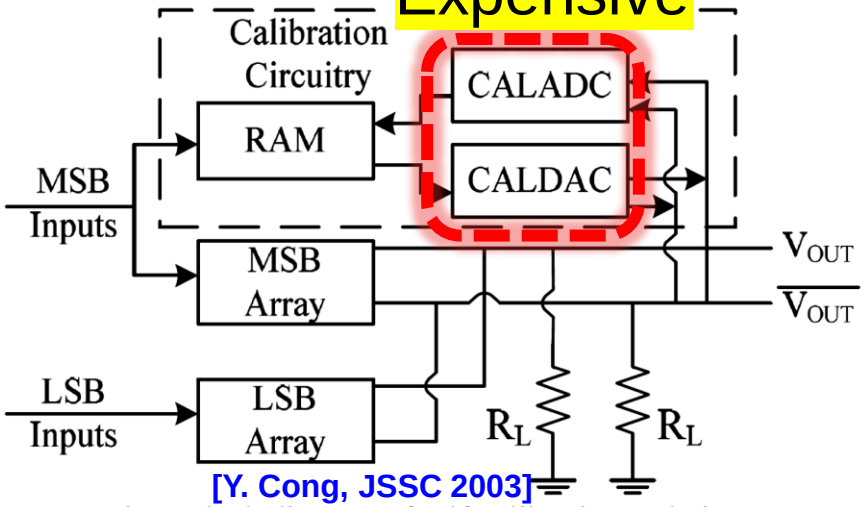
Previous Calibration Circuits

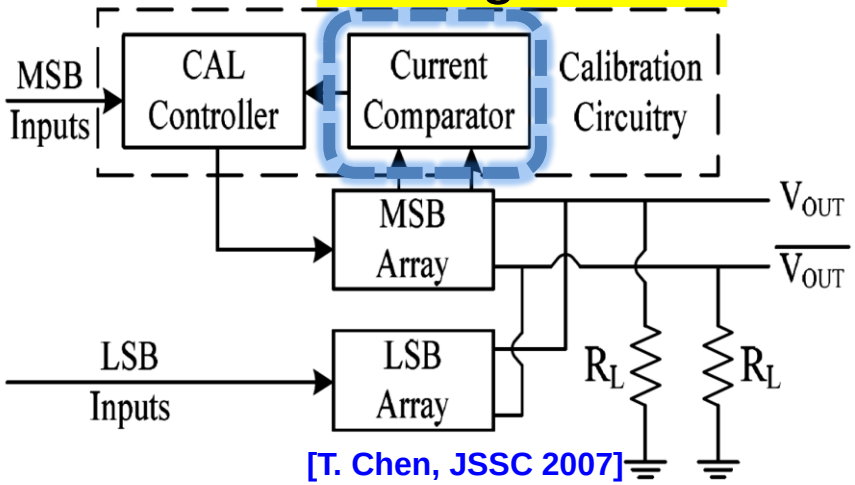
Expensive



[Y. Cong, JSSC 2003]

Fig.1 Block diagram of self-calibration technique

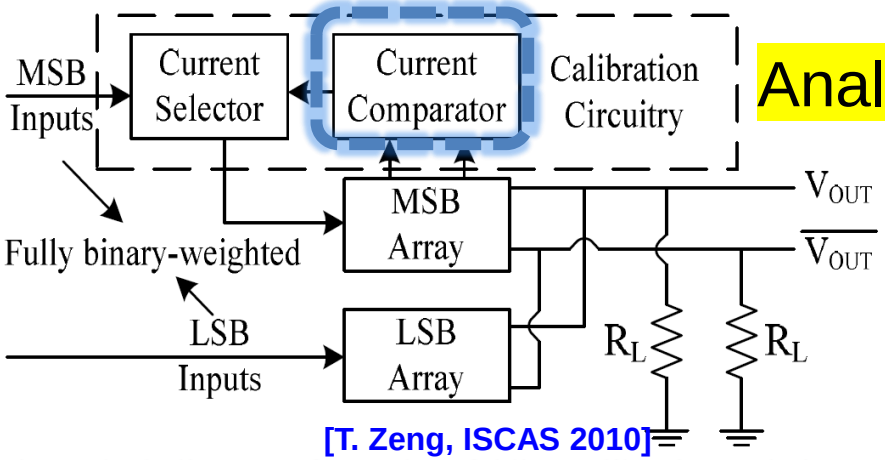
Analog centric



[T. Chen, JSSC 2007]

Fig.2 Block diagram of SSPA calibration technique

Analog centric



[T. Zeng, ISCAS 2010]

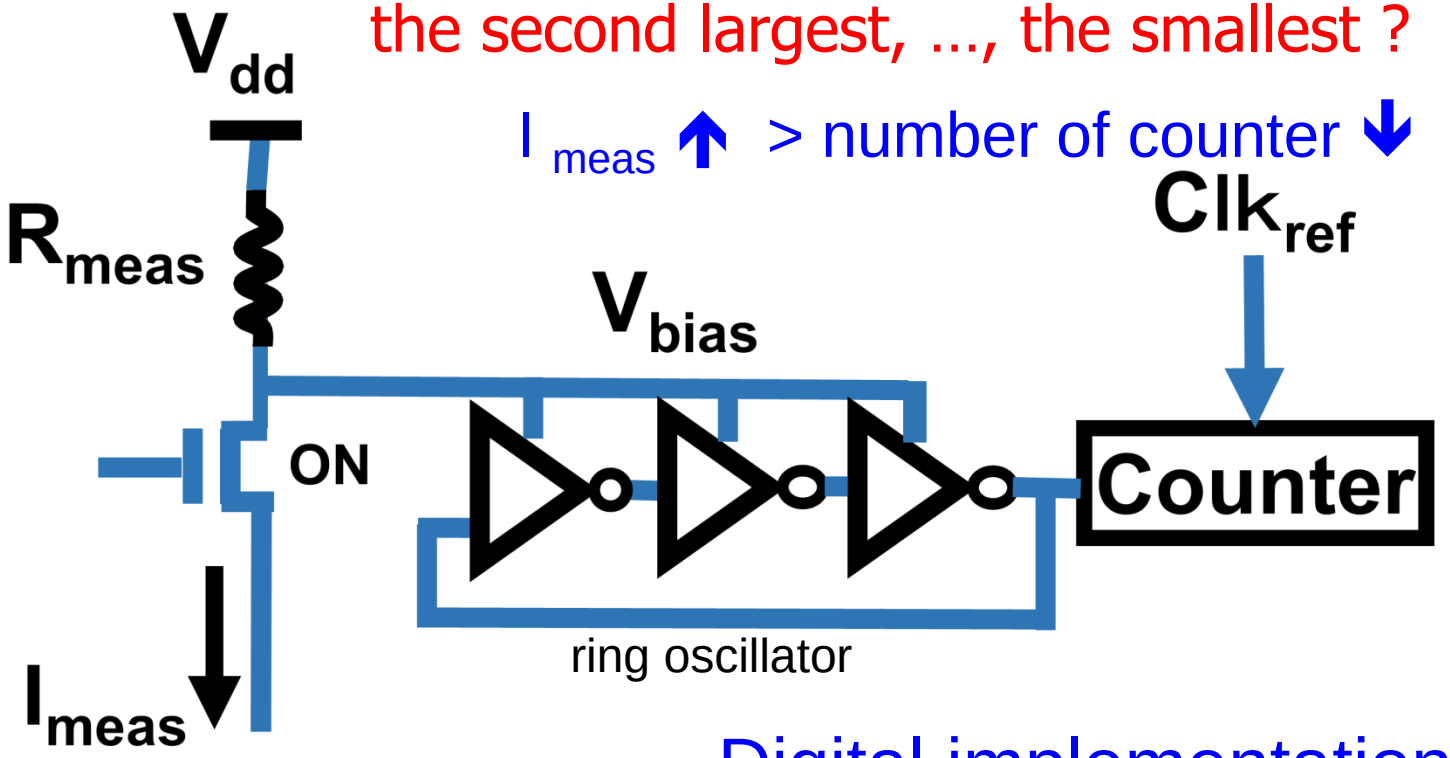
Fig.4 Block diagram of complete-folding calibration technique

Current Measurement Circuit

Only need order of current values.

Which current source is the largest,
the second largest, …, the smallest ?

I_{meas} ↑ > number of counter ↓



Digital implementation!!! ☺

Calibration of Half-Unary DAC

Test code

$H_{in(1)}$ = 00000000000001

⋮

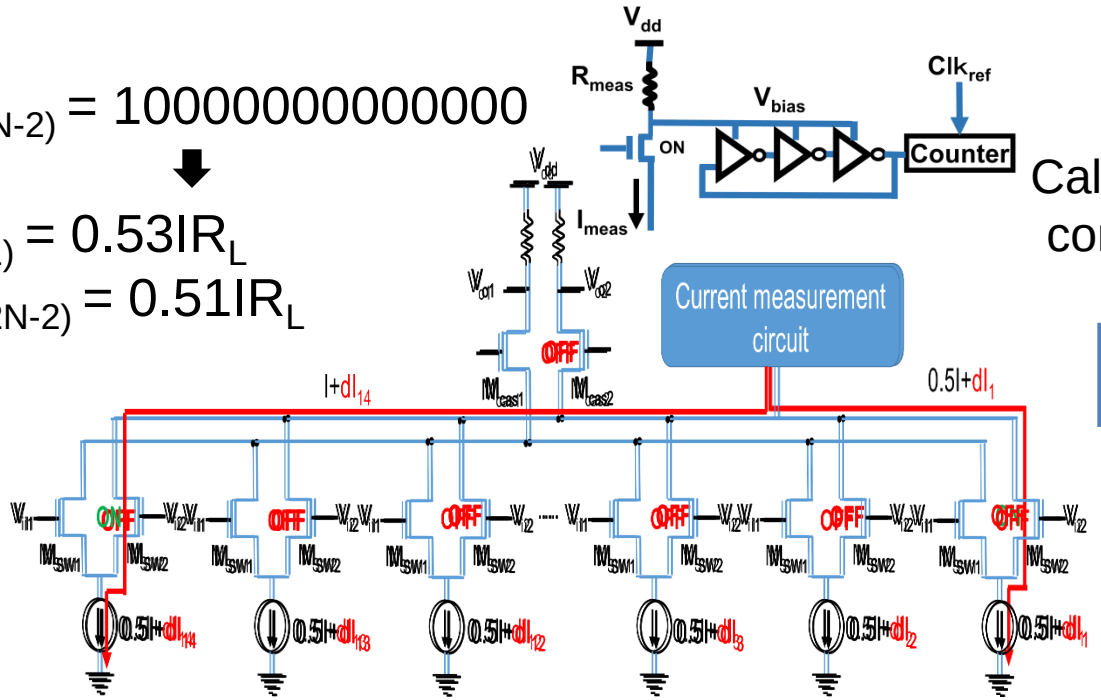
$H_{in(2N-2)}$ = 10000000000000

⬇ ⬇

$V_{out(1)} = 0.53IR_L$

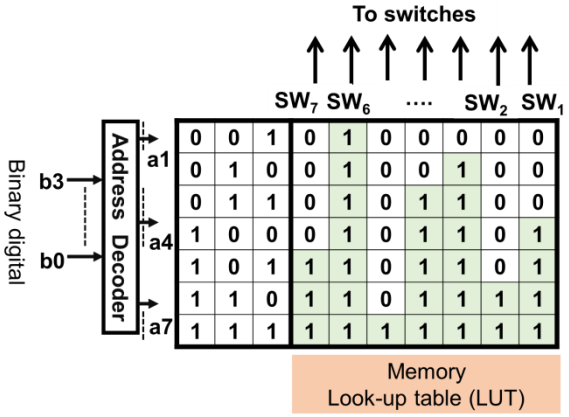
$V_{out(2N-2)} = 0.51IR_L$

Ring oscillator based current measurement circuit



Calibration controller

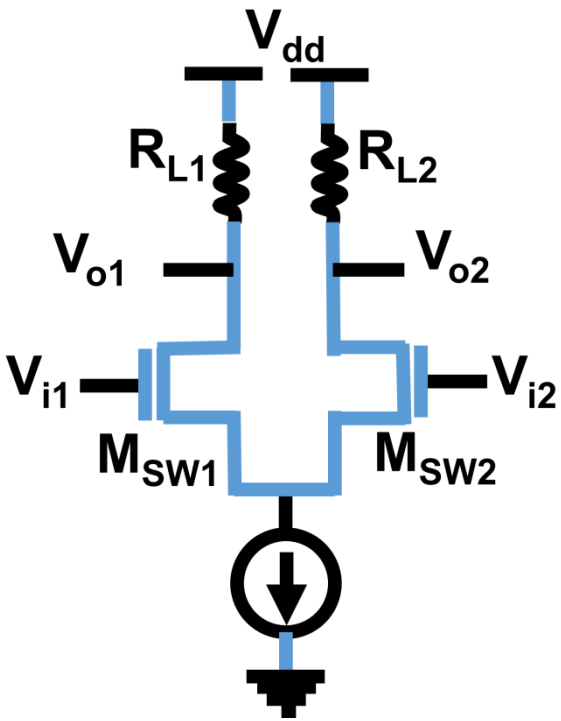
Binary-to-[stored-switching-sequence-code] decoder



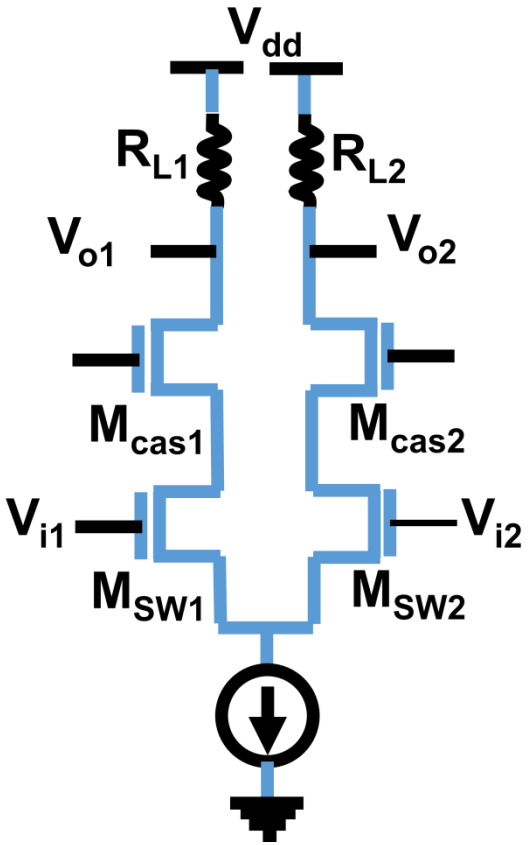
- No additional analog circuit (switches or routing).
- Only add digital circuit for switch control

Current Source & Current Switch

- Basic

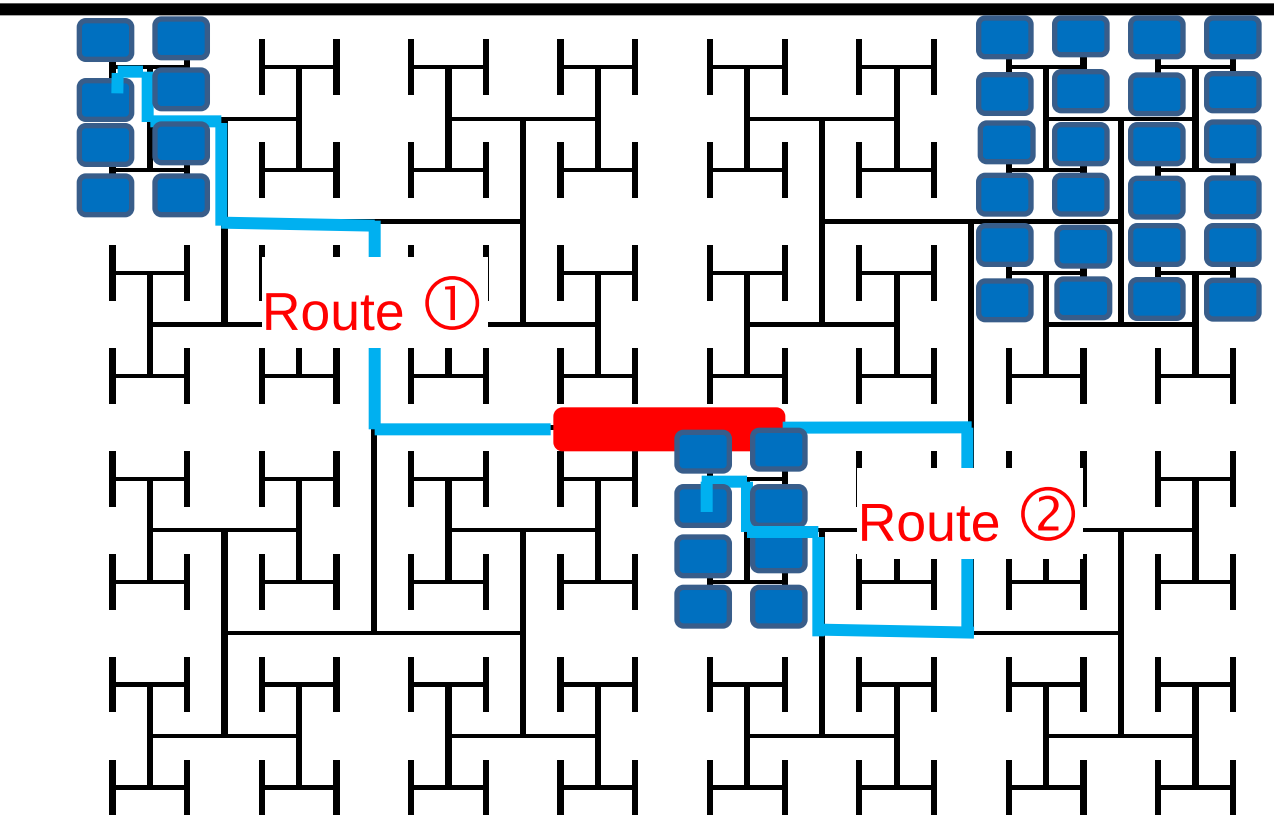


- Cascode



➔ **Reduce code-dependent load variation ☺ !!!**

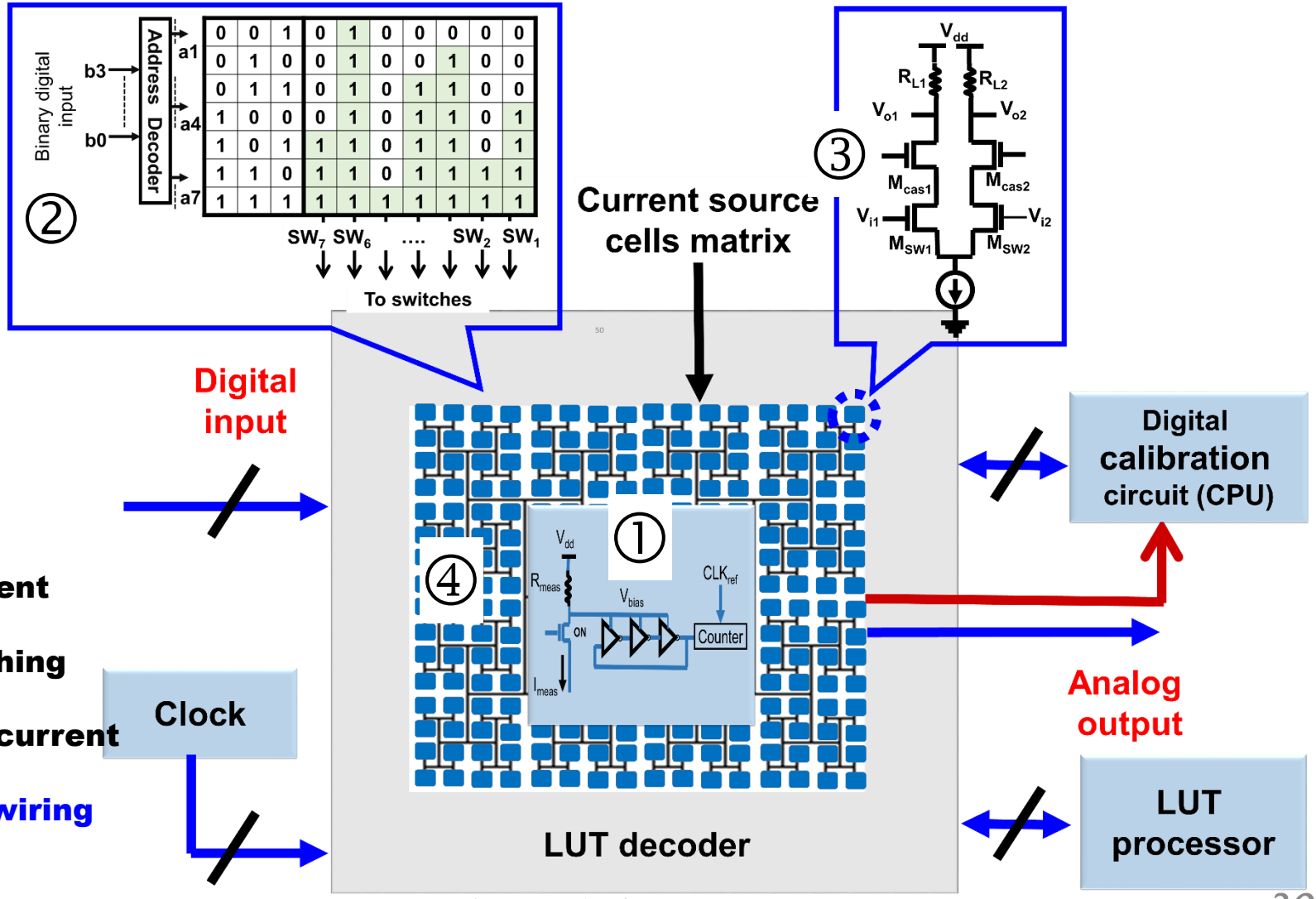
Layout of Current Cells



For every cell, equal length of interconnection to load resistor.

➔Minimum timing skew ☺!!!

Floor Plan of Whole DAC



Features:

① **Digital measurement circuit**

② **New switching scheme**

③ **Cascoded current source**

④ **Isometric wiring**

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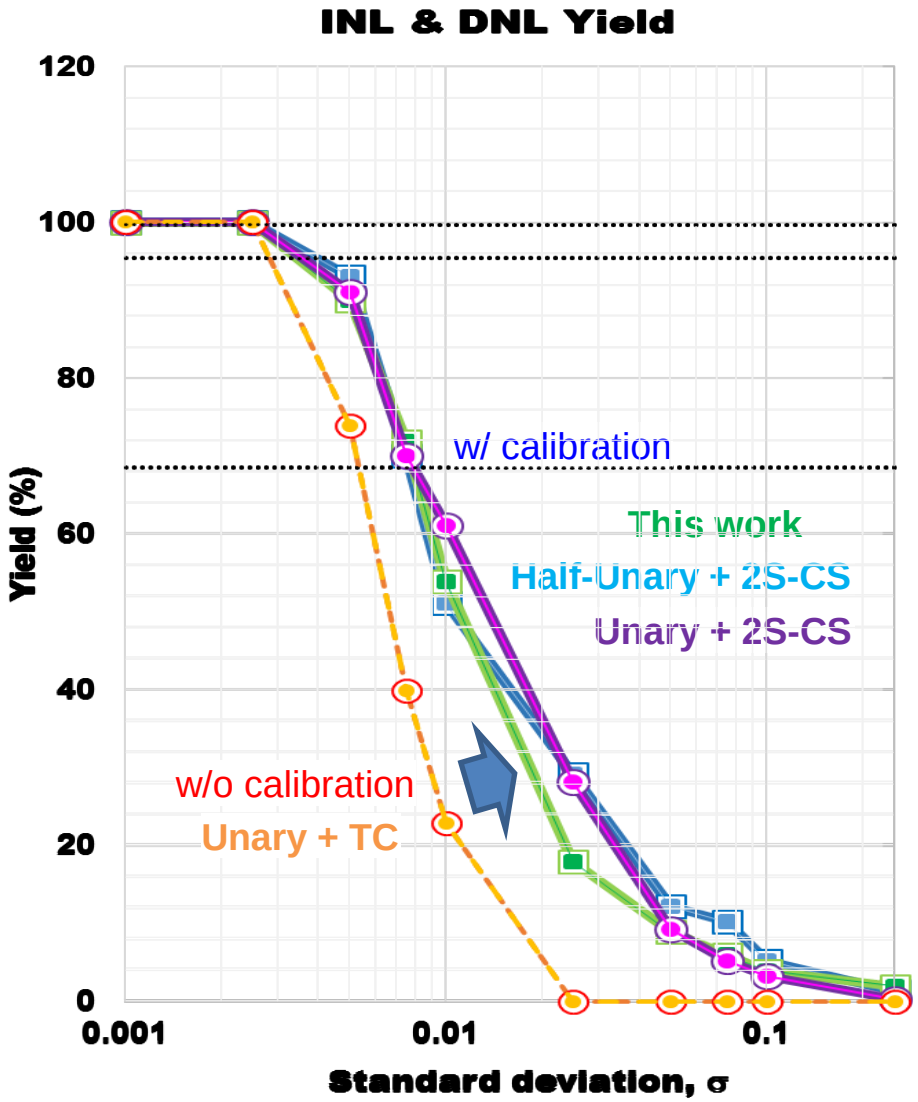
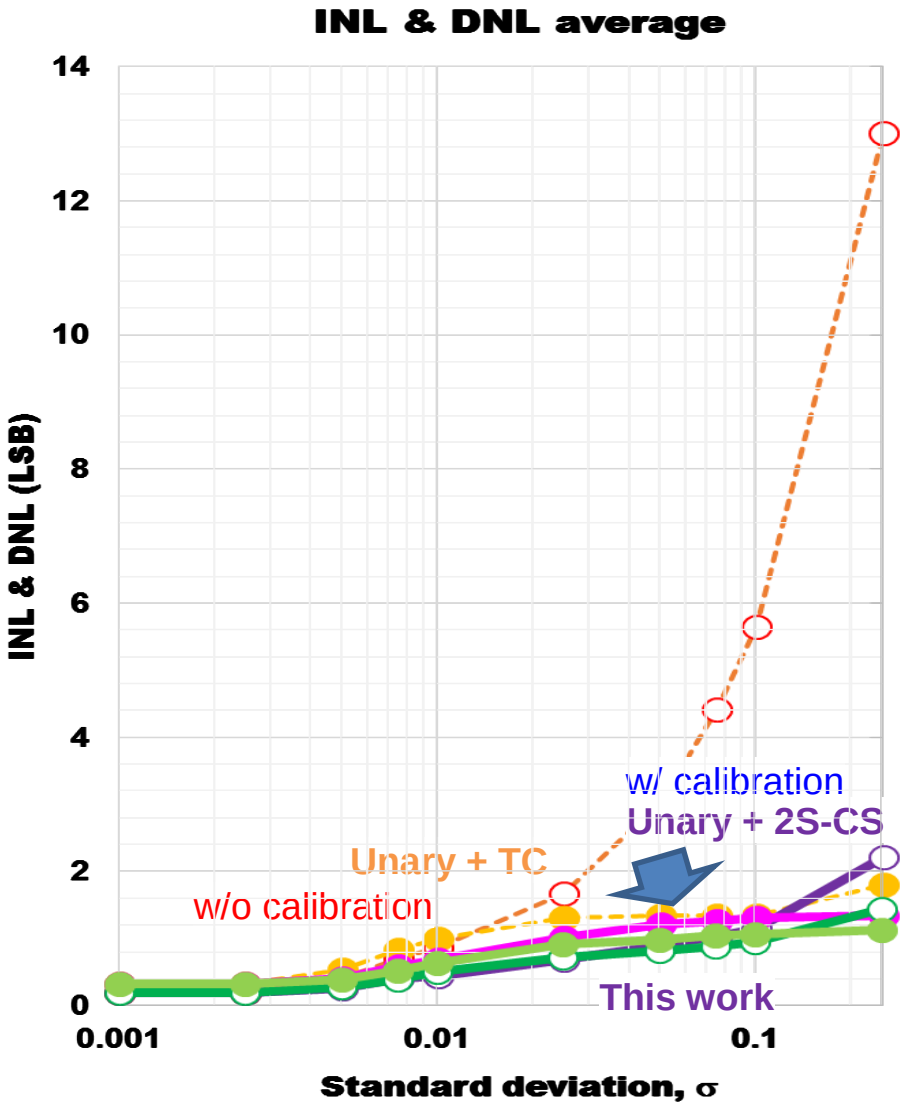
Simulation condition

- Resolution = 12 bit
- Input frequency = 12.8 MHz
- Sampling frequency = 819.2 MS/s
- V_{FS} = 4095 V
- Simulation = 100 times
  - Current source mismatch :

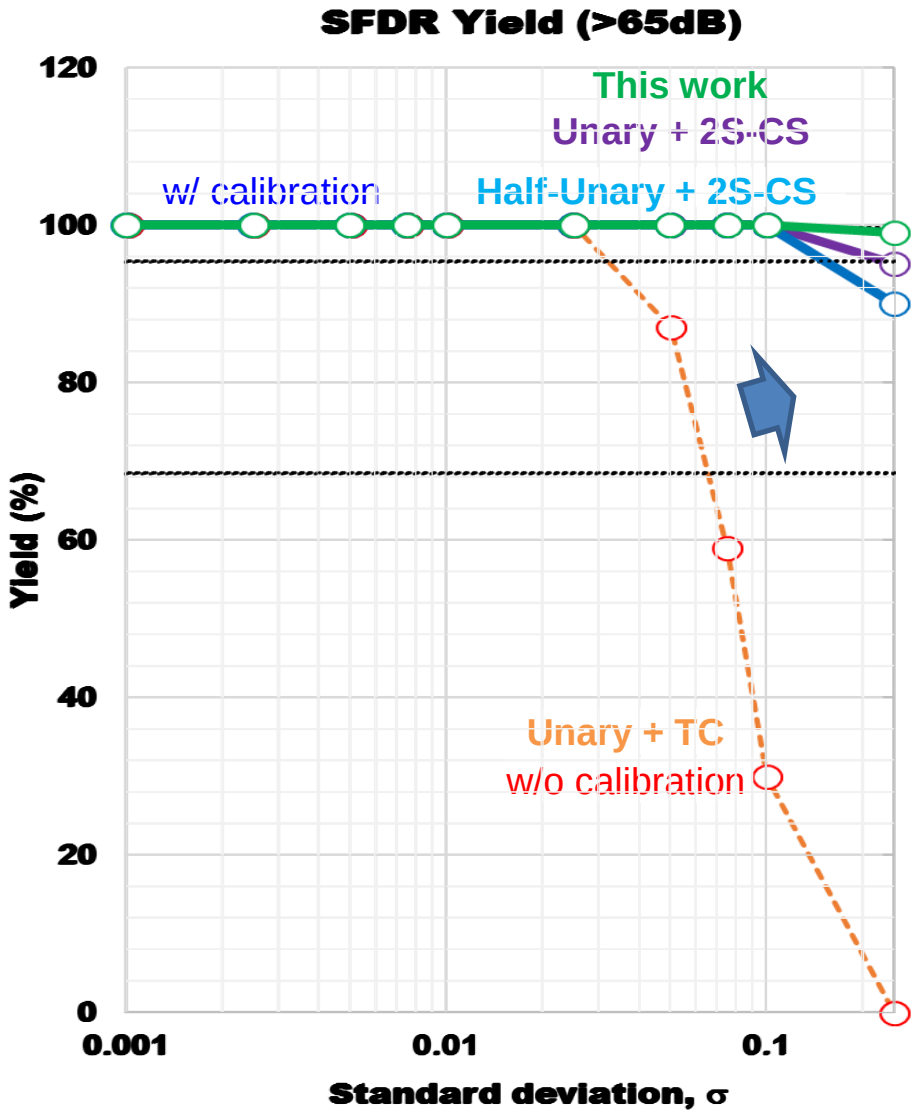
    Normal distribution, N(0, σ)
- Parameter : standard deviation, σ = 0.001 ~0.25
- Switching scheme :
  - Thermometer coded, 2S-CS & 3S-CS

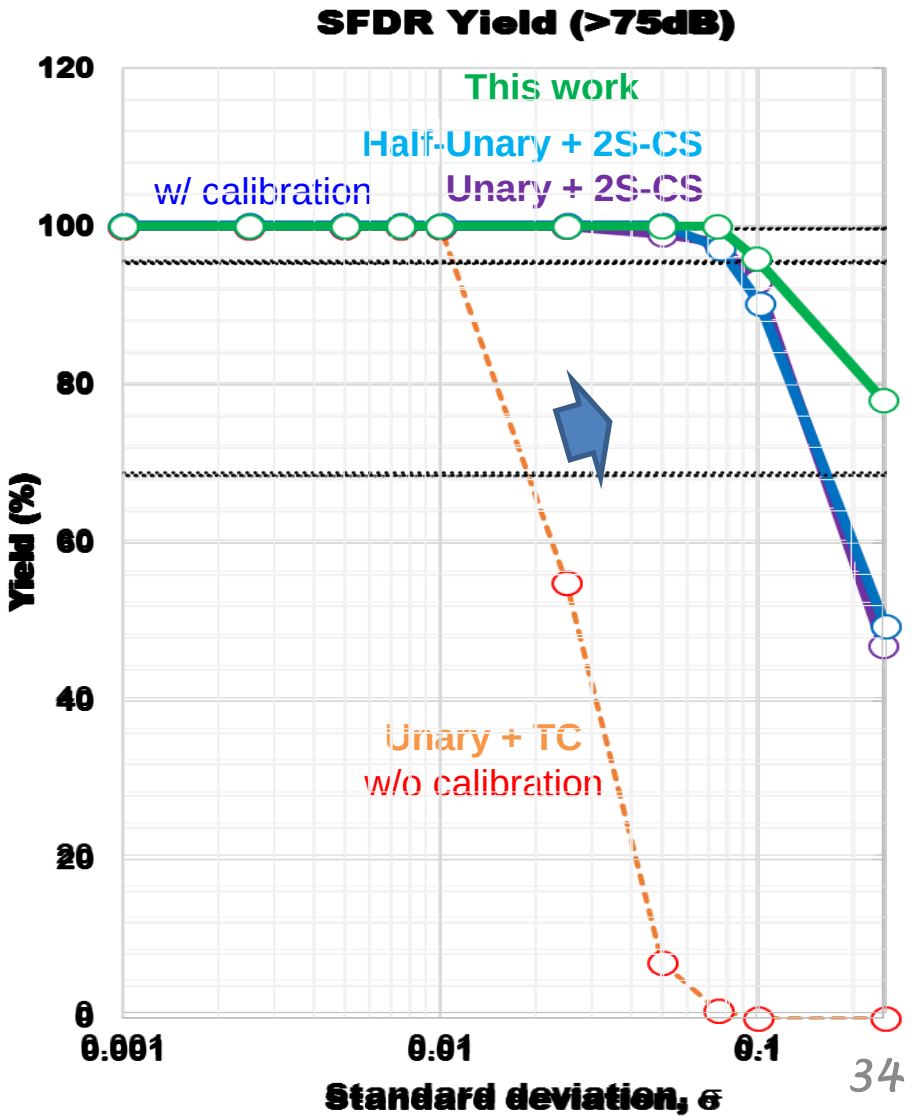
INL & DNL Yields



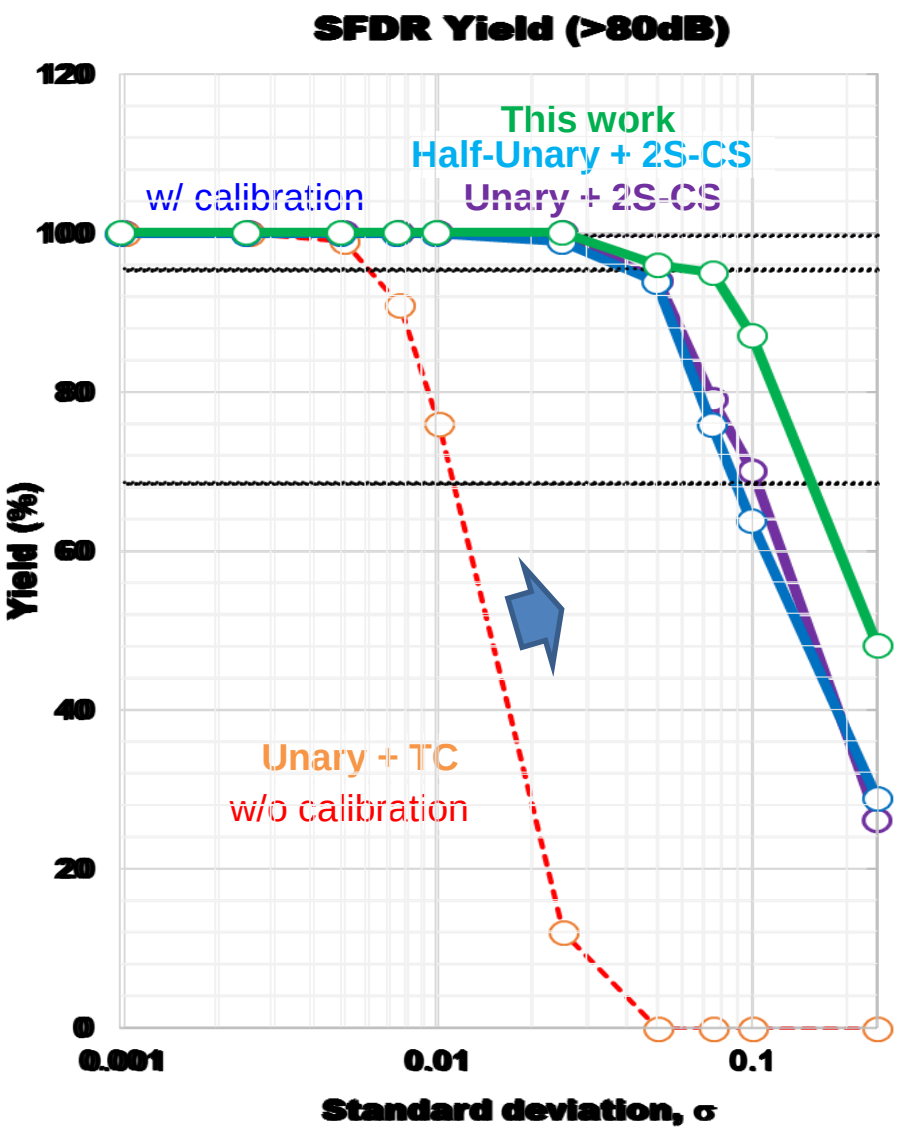


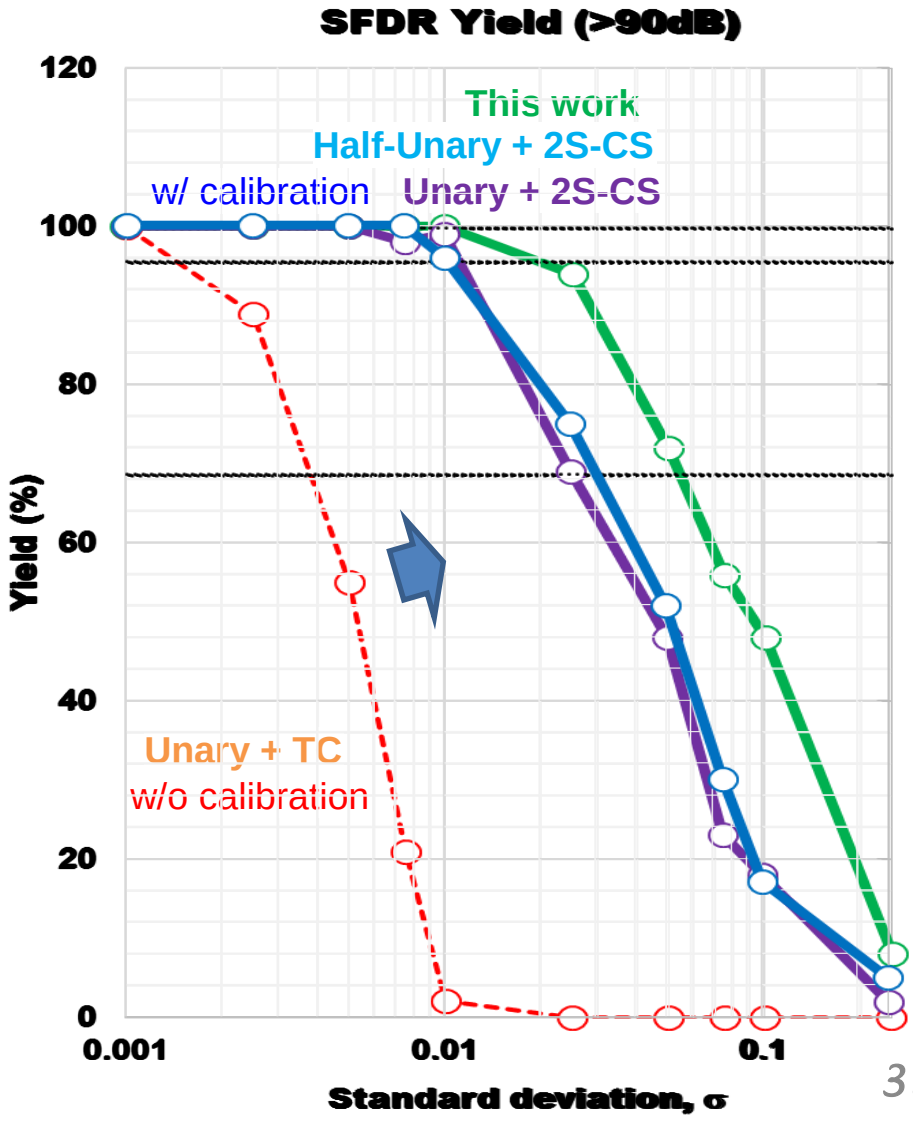
Difference SFDR Yields



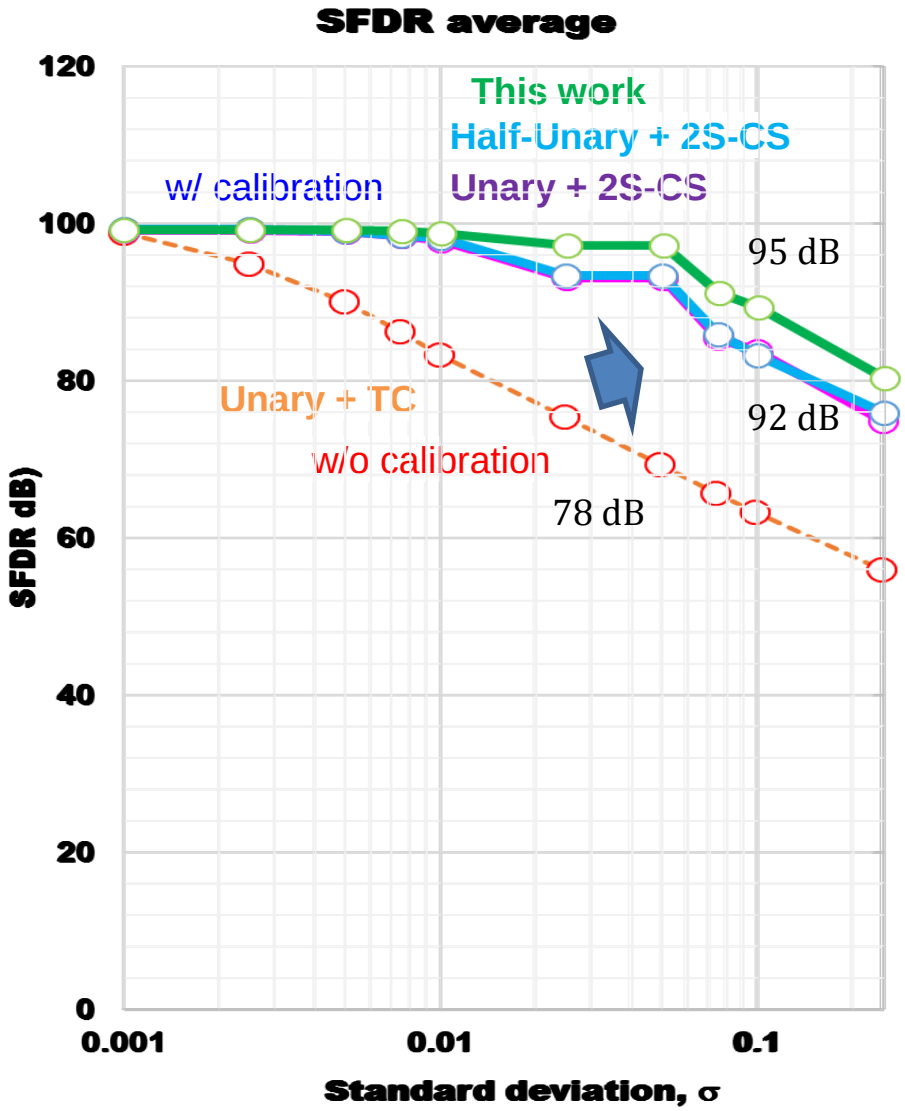


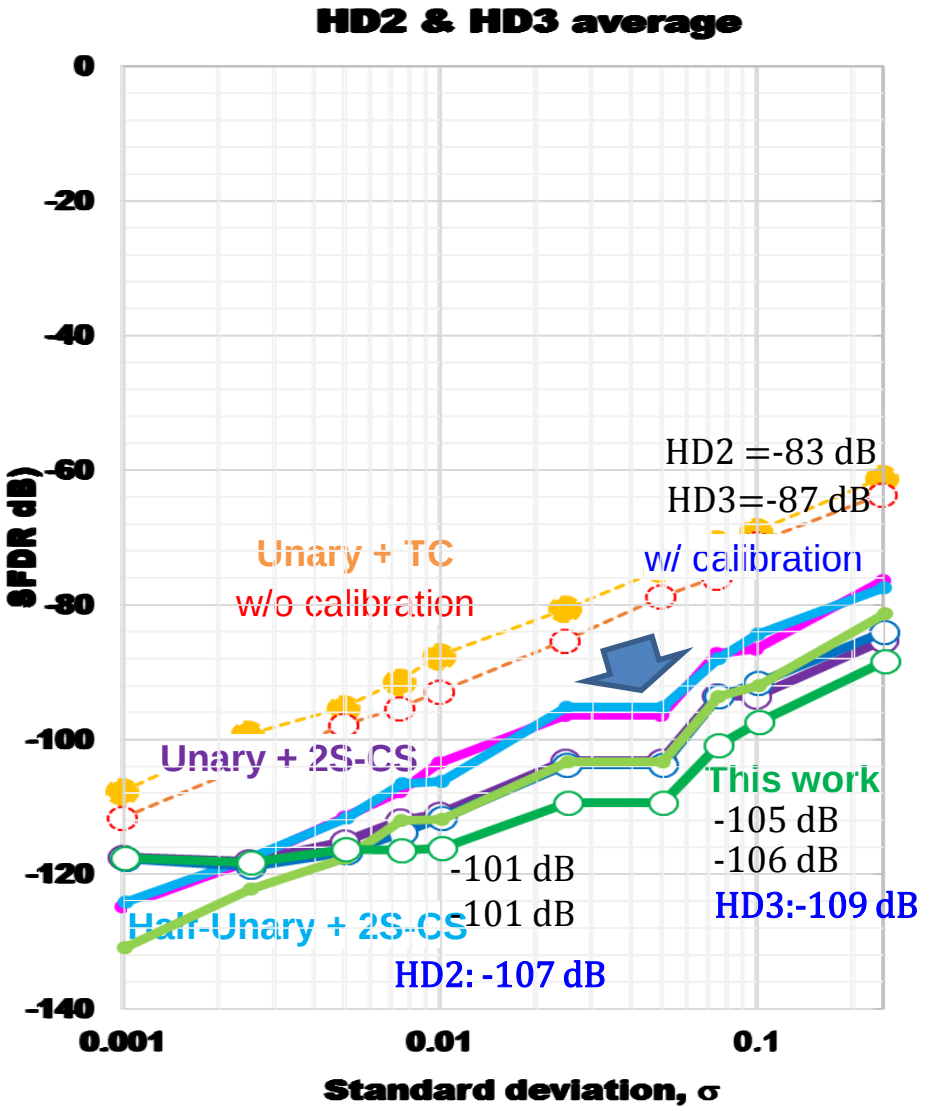
Difference SFDR Yields





Comparison
SFDR & 2nd & 3rd HDs





Calibration Technique Comparison

Technique	Advantages	Drawbacks
Self calibration [JSSC 2003] [14-b 100MHz] [1]	• High precision calibration	• Require high precision calibration ADC
SSPA [JSSC 2007] [14-b 200MHz] [2]	• Minimum additional analog & digital circuit • Defect current source replacement • Improve INL	• No DNL improvement • Analog current comparator
Complete-folding [ISCAS 2010] [14-b] [3]	• Minimum additional analog & digital circuit • Improve INL & DNL • Low voltage	▪ Analog current comparator
This work	• Digital centric • More INL & DNL improvement • Relax matching requirement	• Twice or more current cells

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Conclusion

- High SFDR based current steering DAC with fine digital CMOS implementation
- For DAC static linearity improvement
  - ① Half-unary DAC architecture
  - ② 3-stage sort & group algorithm for current sources
  - ⇒ Performed MATLAB simulation with difference switching schemes
    - Better INL & DNL yields ☺
    - Better SFDR level ☺
- For DAC dynamic linearity improvement
  - ① Well-balanced layout of current cells for interconnection R, C skew minimization.

Thank you very much
for your kindly attention

Q&A

Q : Why use 3-stage current sorting rather than
2-stage current stage?

A : In order to improve both INL & DNL,
the 3-stage current sorting is chosen.

Q : How about the range of the sampling rate use?

A : Sampling rate
between 100MS/s and 1 GS/s is considered.

Q & A

Q : The number of bits and process node?

A : Stand alone of 12b half-unary and 14b and above of segmented structures.

In term of process node, we will decide after further verification has been done.


3-Stage
Alg
Current
Linearity


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Background
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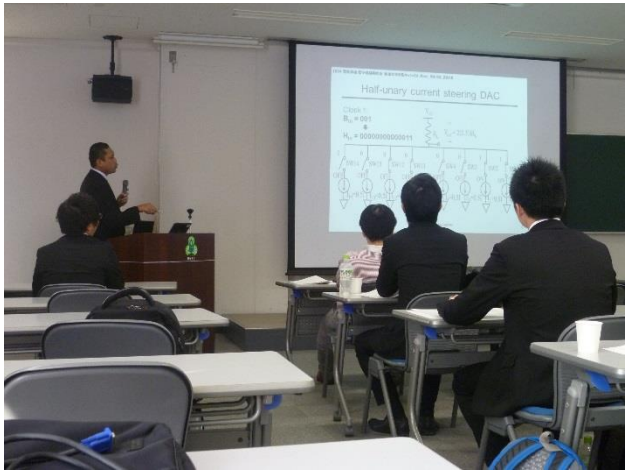
Digital-to-Analog Converter (DAC)
Problem
Transmitter & signal generation


Half-unary current steering DAC