P85

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Linearity Improvement Algorithm for Current-Steering DAC Based on 3-Stage Sorting of Half-Unary Current Sources

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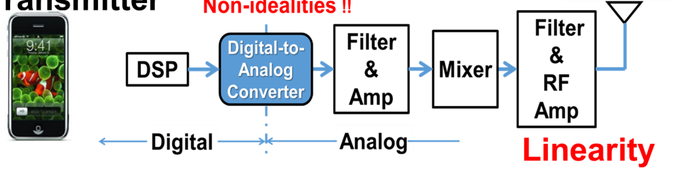
Introduction

- **Background**
  - **Telecommunication devices**
    - **Mobile phones, wireless modems & avionics**
    - **High-speed, high-accuracy digital-to-analog converter (DAC)**

- **Problem**
  - **Transmitter**

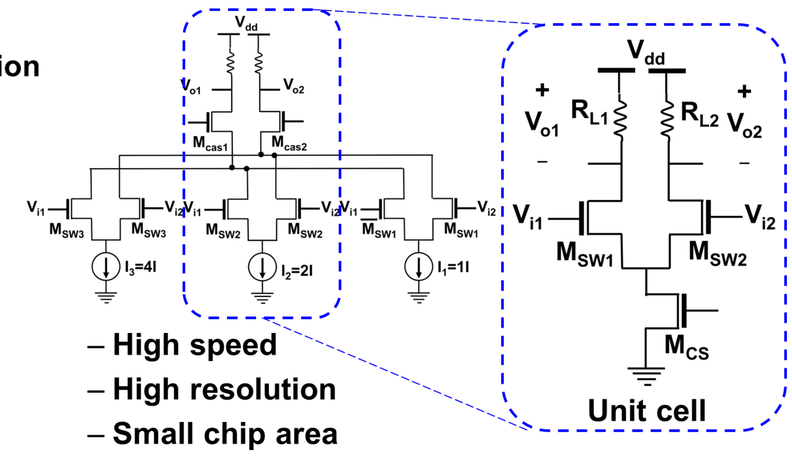


Linearity degradation!!! ☹

Objective

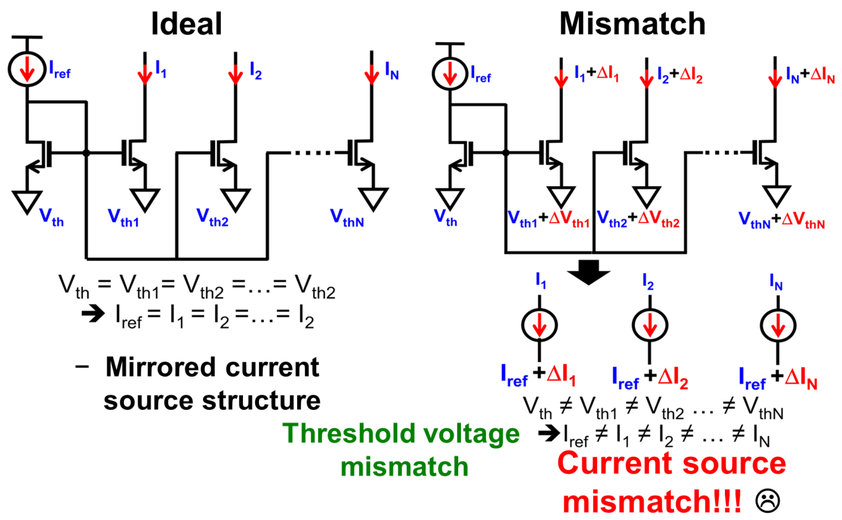
- **Objective**
  - **High SFDR current-steering DAC for communication**
- **Proposed method**
  - **Current source mismatch effect reduction**
    - ① **Half-unary DAC architecture**
    - ② **Current source sorting algorithm**
      - ➔ **Static linearity improvement**
  - **Layout strategy**
    - ① **Clock-tree-like layout of current sources & switches**
      - ➔ **Dynamic linearity improvement**

Current-steering DAC



- **High speed**
- **High resolution**
- **Small chip area**

Mismatch



$V_{th} = V_{th1} = V_{th2} = \ldots = V_{th2}$
➔ $I_{ref} = I_1 = I_2 = \ldots = I_2$

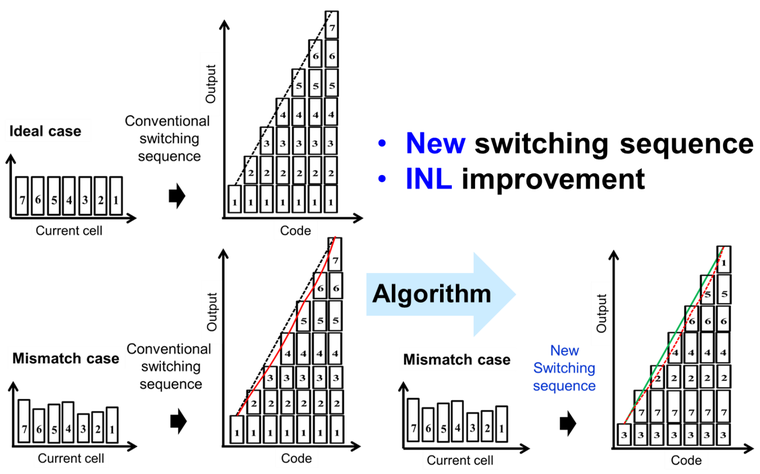
- **Mirrored current source structure**

Threshold voltage mismatch

$V_{th} \neq V_{th1} \neq V_{th2} \ldots \neq V_{thN}$
➔ $I_{ref} \neq I_1 \neq I_2 \neq \ldots \neq I_N$

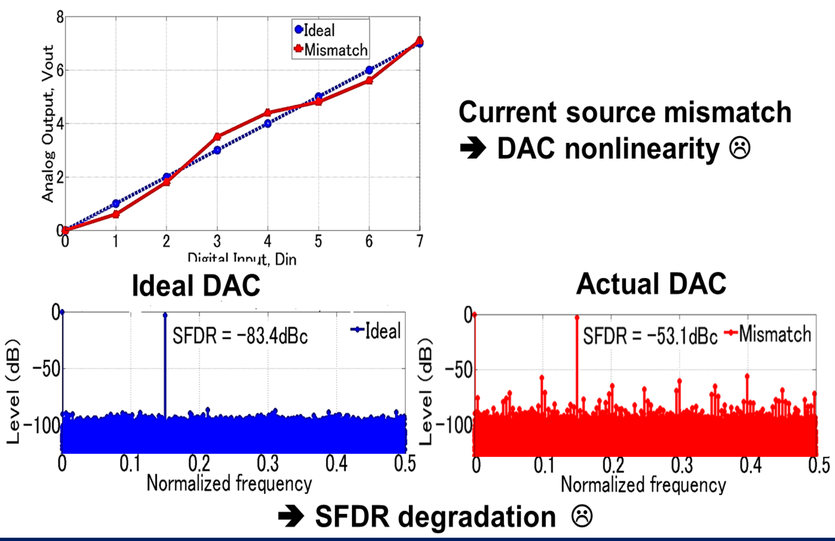
Current source mismatch!!! ☹

Switching Sequences



- **New switching sequence**
- **INL improvement**

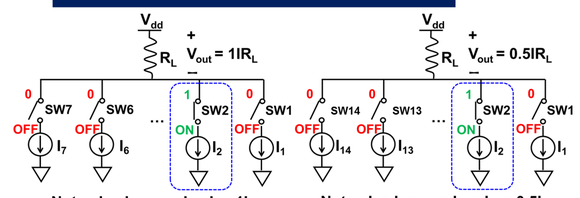
Nonlinearity



Current source mismatch ➔ DAC nonlinearity ☹

➔ **SFDR degradation** ☹

Half-unary

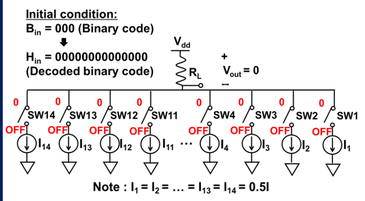


Note : $I_1 = I_2 = \ldots = I_6 = I_7 = 1I$

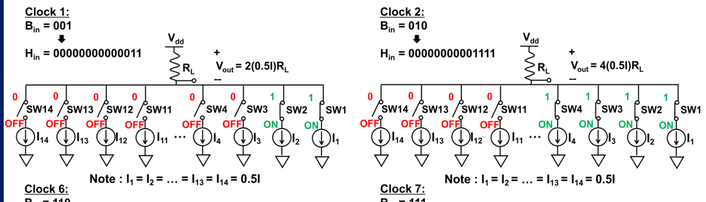
Note : $I_1 = I_2 = \ldots = I_{13} = I_{14} = 0.5I$

	Unary	Half-unary
Number of CS	2^N-1	$2(2^N$-1)
Current value	I	0.5I

N : number of bit



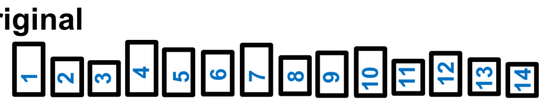
Note : $I_1 = I_2 = \ldots = I_{13} = I_{14} = 0.5I$



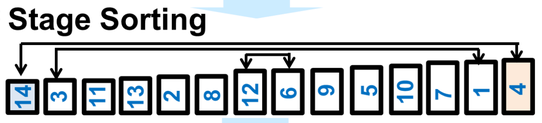
Note : $I_1 = I_2 = \ldots = I_{13} = I_{14} = 0.5I$

Digital algorithm

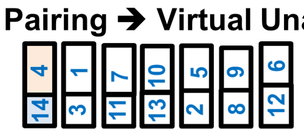
- **Original**



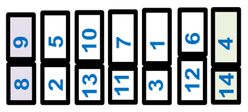
- **1st Stage Sorting**



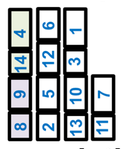
- **1st Stage Pairing ➔ Virtual Unary**



- **2nd Stage Sorting**

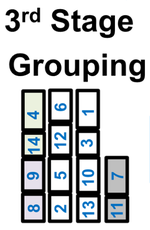


- **2nd Stage Grouping**

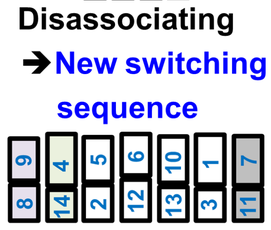


- **3rd Stage Sorting**

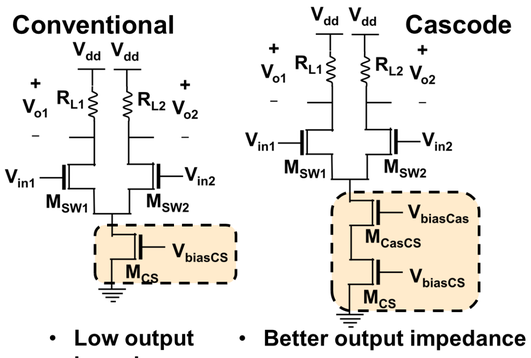
- **3rd Stage Grouping**



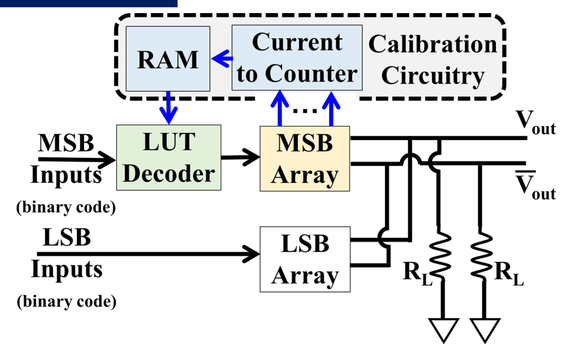
- **Disassociating ➔ New switching sequence**



Circuit

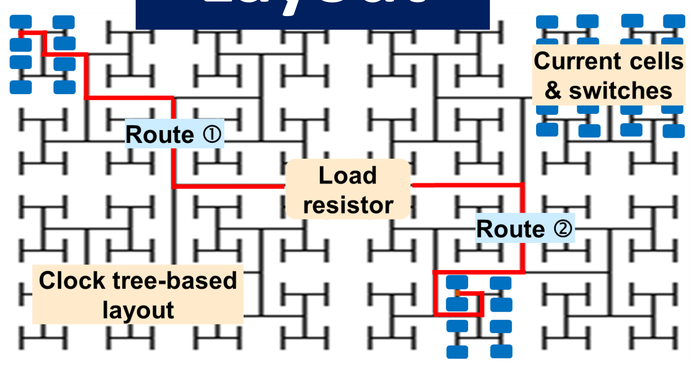


- **Low output impedance**
- **Better output impedance**
- **Better node isolation**



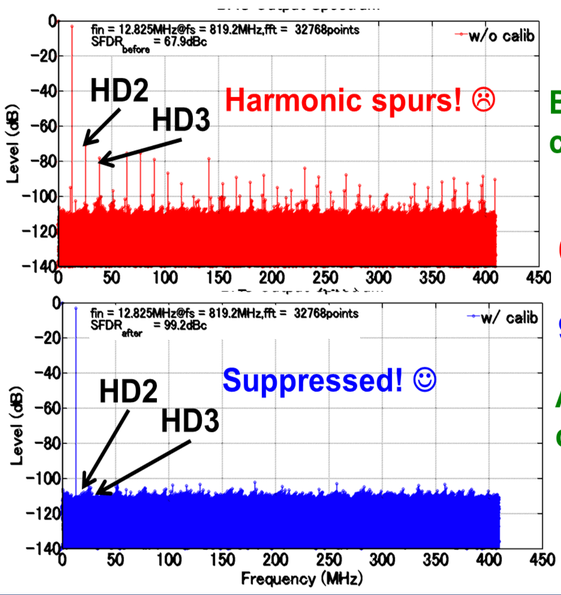
- **No additional analog circuit (switches or routing).**
- **Only add digital circuit for switch control**

Layout



Isometric of interconnection to load resistor
➔Minimum timing skew ☺!!!

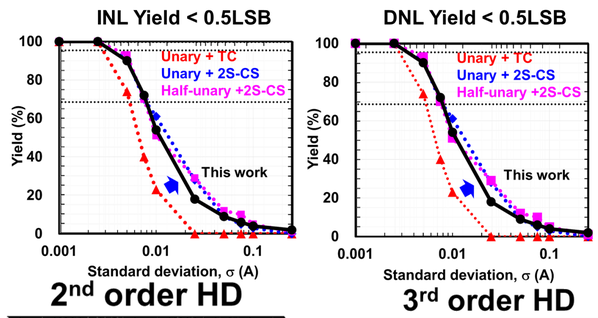
Simulation Result

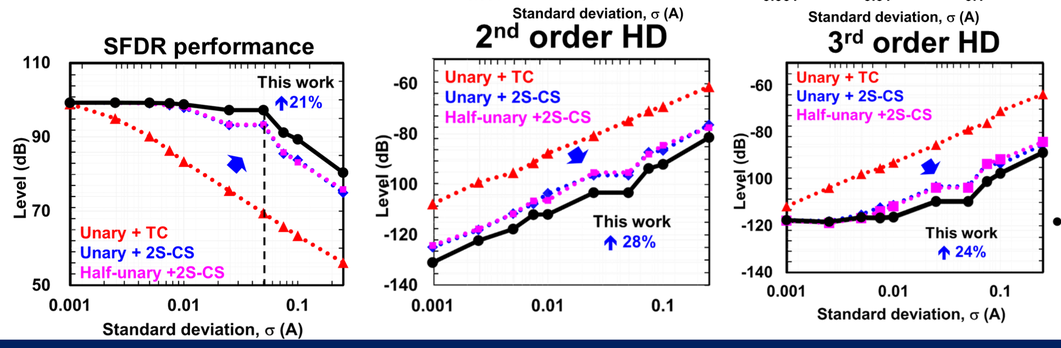


Before calibration

SFDR:
67.9 dB
⬇
99.2 dB

After calibration





Summary

- **High SFDR CS DAC for fine CMOS**
- **Static linearity improvement**
  - ① **Half-unary DAC architecture**
  - ② **3-stage current sorting algorithm (calibration)**
  - ➔ **Performed MATLAB simulation with different switching schemes**
    - **Better INL & DNL yields ☺**
    - **Better SFDR, 2nd & 3rd HDs level ☺**
- **Dynamic linearity improvement**
  - ① **Well-balanced layout of current cells for interconnection R, C skew minimization.**