**Research Motivation**

- Time-to-Digital Converter (TDC) measures time interval between two signal transitions, into digital signal.
  - (1) High speed and high frequency signal testing circuit
    - Timing testing of data and clock in DDR memory
    - Phase noise testing
  - (2) Analog circuit design in nano-CMOS SoC

**Research Objective**

- Development of timing measurement & testing circuit
  - Short measurement time
  - Fine time resolution
  - High linearity
  - Digital output

**Our Approach**

- Multi-bit ΔΣ TDC with DWA Algorithm
  - ΔΣ TDC
    - Fine time resolution
    - Small circuit
    - Digital output
  - Multi-bit
    - Short measurement time
  - Data Weighted Averaging (DWA) Algorithm
    - High linearity

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**Single-bit ΔΣ TDC**

- **Advantages**
  - Fine time resolution
  - High linearity
  - Simple circuit

- **Problem**
  - Long measurement time

- **Advantage**
  - Short measurement time by 1/2^n

- **Input timing range:** \(-\frac{\Delta T}{N}<\Delta T<\frac{\Delta T}{N}\)

- **Time resolution:** \(\frac{2\tau}{N}\)

- **Input timing range:** \(D_{out}=0\) : \(D_{out}=0\)

- **Input timing range:** \(D_{out}>0\) : \(D_{out}=1\)

**Multi-bit ΔΣ TDC**

- **Advantage**
  - Nonlinearity due to delay mismatches

- **Problem**
  - Average due to mismatch of all delays.

**DWA Algorithm**

- **Advantage**
  - Short measurement time

- **Input timing range:** \(D_{out}(\text{FlashADC})=0\)

**Delta mismatch time-average by equal usage of all delays.**

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**Multi-bit ΔΣTDC Design**

- **Analog FPGA Implementation**
  - External board
  - Analog FPGA (PSoC)

- **DWA Circuit Implementation**
  - Comparator’s output is 1
    - Without DWA
    - Time N+1
  - Comparator’s output is 2
    - With DWA
    - Time N+1

**Summary**

- We have implemented a multi-bit ΔΣ TDC employing DWA algorithm with analog FPGA.
- We have confirmed its operation, and DWA effectiveness.
- It can be timing testing BOST
  - Fine time resolution
  - Short testing time
  - High linearity
  - Small circuit.

**References**


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**Measurement results**

- **INL**
  - Without DWA
  - With DWA

- **DWA improves TDC linearity.**