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# Analog FPGA Implementation of Multi-bit Delta-Sigma TDC


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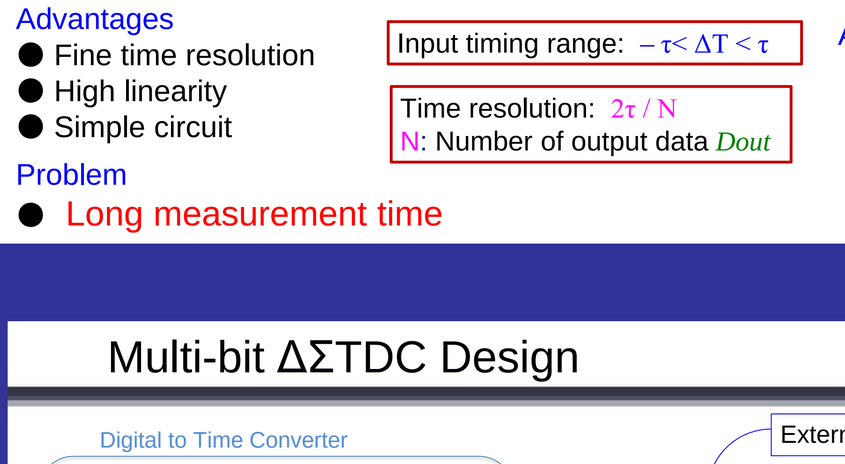
## Introduction

### Research Motivation

Time-to-Digital Converter (TDC) measures time interval between two signal transitions, into digital signal.

(1) High speed and high frequency signal testing circuit
- Timing testing of data and clock in DDR memory
- Phase noise testing

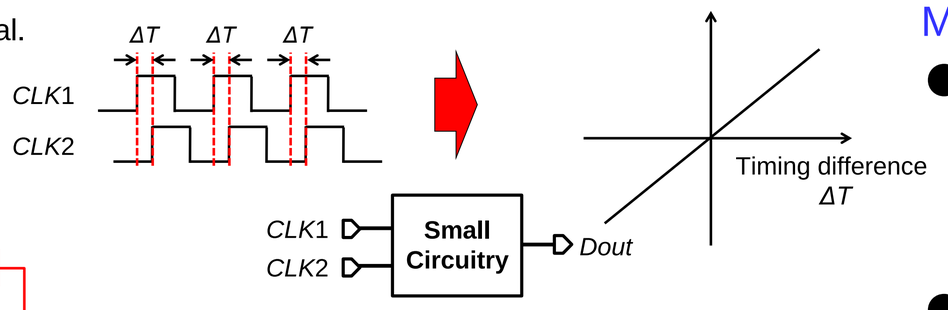
(2) Analog circuit design in nano-CMOS SoC




facing difficulties due to reduced supply voltage

becoming superior

### Research Objective




Development of timing measurement & testing circuit
- short measurement time
- fine time resolution
- high linearity
- digital output

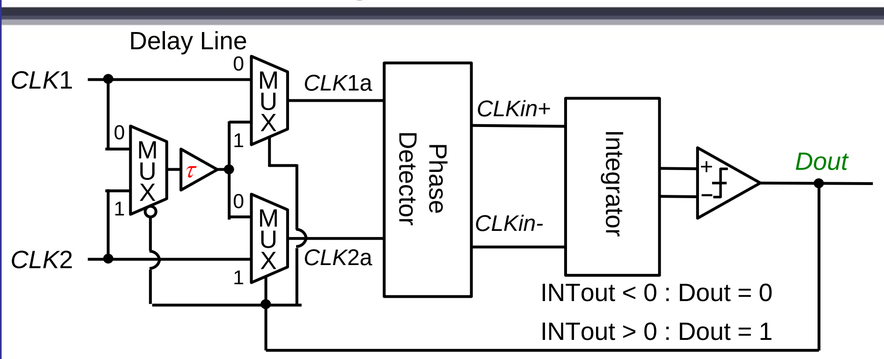
### Our Approach

Multi-bit ΔΣ TDC with DWA Algorithm

- ΔΣ TDC
  - Fine time resolution
  - ➡ Small circuit
  - Digital output
- Multi-bit
  - ➡ Short measurement time
- Data Weighted Averaging (DWA) Algorithm
  - ➡ High linearity

## Proposed Circuit

### Single-bit ΔΣ TDC



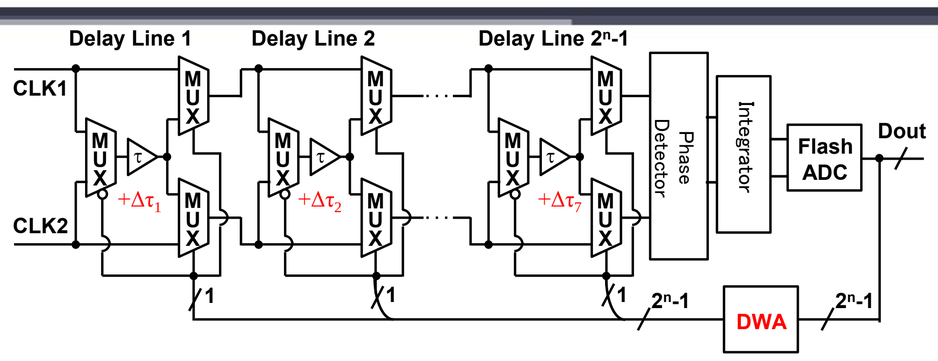

Advantages
- Fine time resolution
- High linearity
- Simple circuit

Input timing range: $-\tau < \Delta T < \tau$

Time resolution: $2\tau / N$
N: Number of output data *Dout*

Problem
- Long measurement time

### Multi-bit ΔΣ TDC

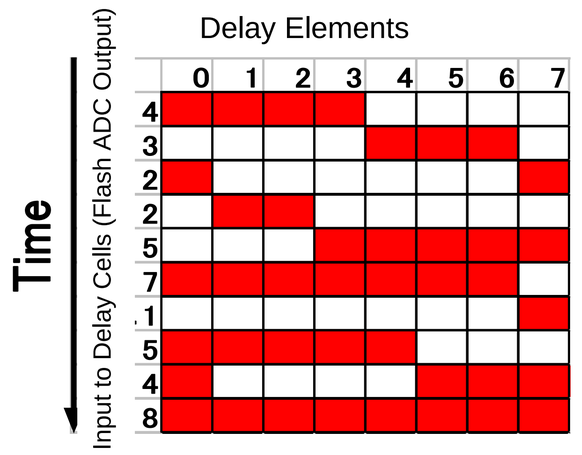



Advantage
Short measurement time by $1/2^n$

Problem
Nonlinearity due to delay mismatches

Solution DWA algorithm

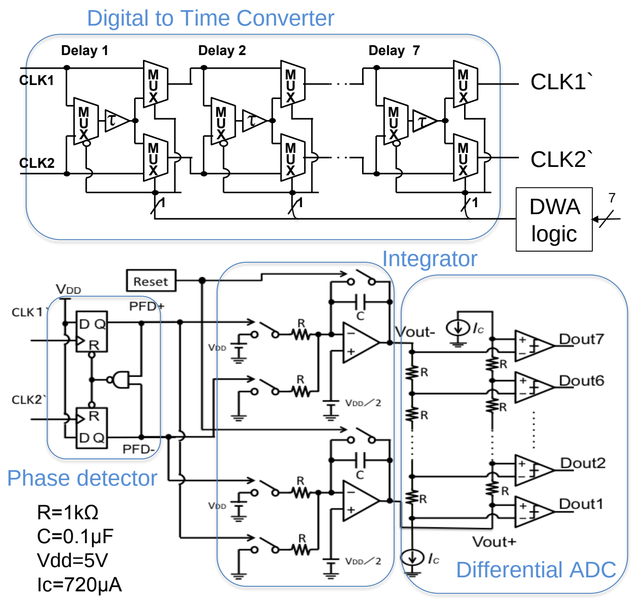
### DWA Algorithm



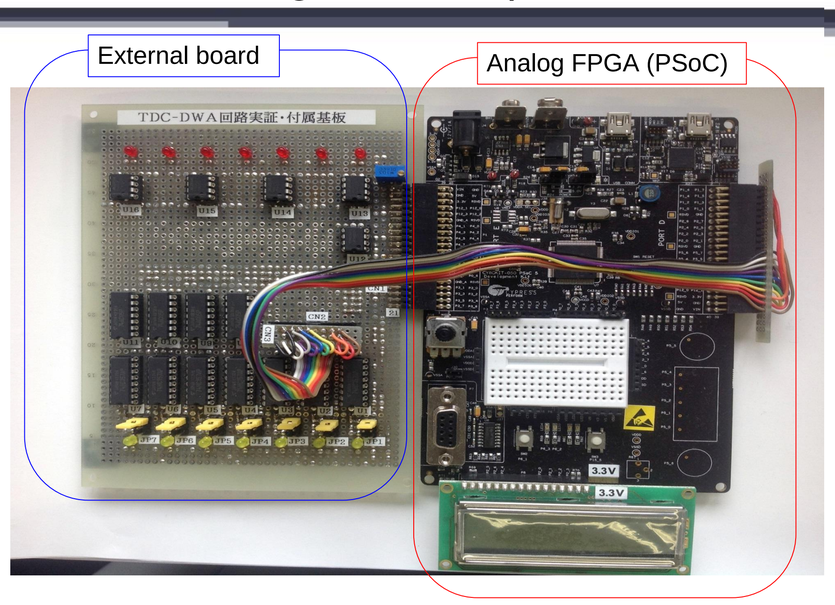

Delay mismatch time-average by equal usage of all delays.

## Experiment

### Multi-bit ΔΣTDC Design

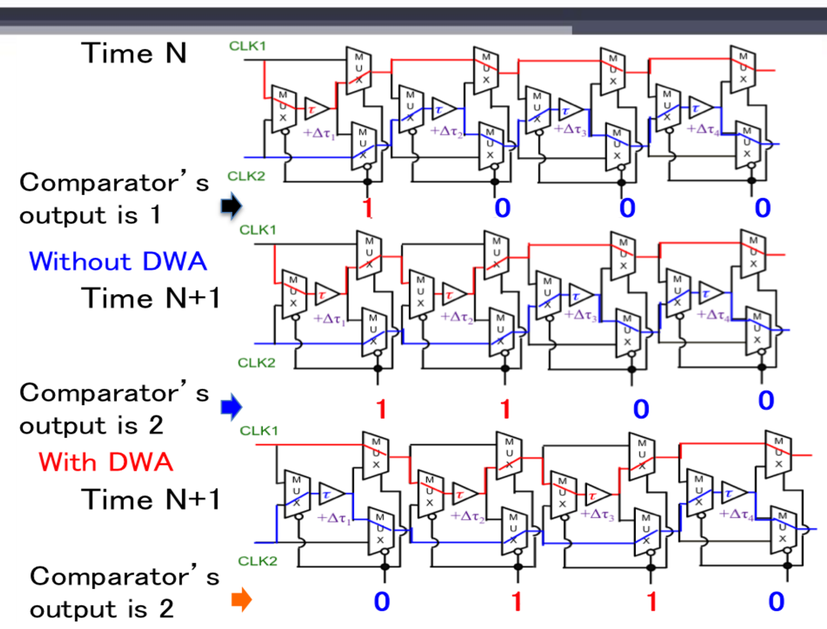



### Analog FPGA Implementation

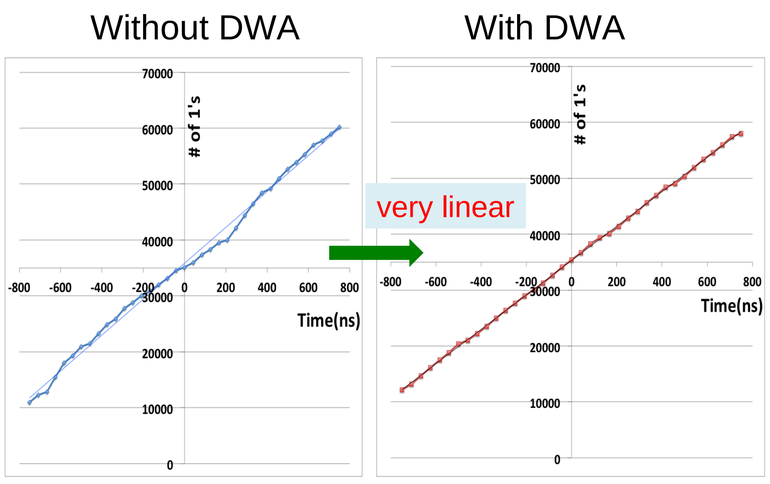



PSoC5LP(Programmable System-on-Chip, Cypress Semiconductor)
External board（Delay line, Differential ADC ）

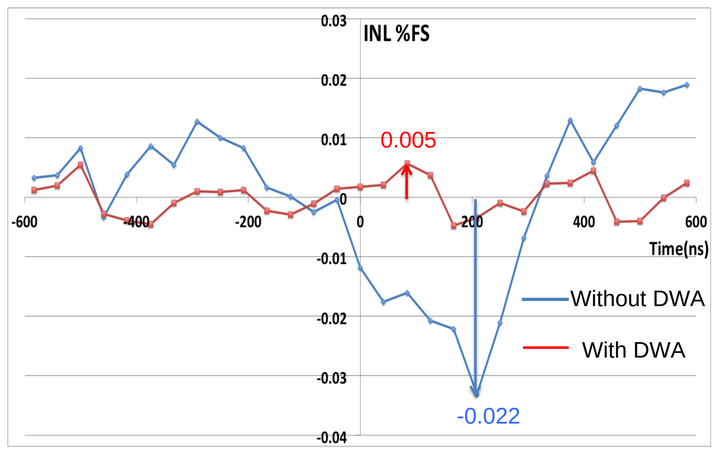
### DWA Circuit Implementation




## Measurement results




## INL




DWA improves TDC linearity.

## Summary

- We have implemented a multi-bit ΔΣ TDC employing DWA algorithm with analog FPGA .
- We have confirmed its operation, and DWA effectiveness.
- It can be timing testing BOST
  - fine time resolution
  - short testing time
  - high linearity
  - small circuit.

## References


[1] S. Uemori, M. Ishii, H. Kobayashi, et. al., "Multi-bit Sigma-Delta TDC Architecture with Improved Linearity," J. of Electronic Testing, Springer, vo. 29, no. 6, pp.879-892 (Dec. 2013).

[2] Y. Osawa, D. Hirabayashi, N. Harigai , H. Kobayashi, et. al., "Phase Noise Measurement Techniques Using Delta-Sigma TDC", IMS3TW'14, Porto Alegre, Brazil (Sept.2014).