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Analog FPGA Implementation of Multi-bit Delta-Sigma TDC

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I/O interfacing circuits such as double-data-rate (DDR) memory interfaces are very important, and their low-cost, high-quality test is challenging. This paper describes simple circuitry for measuring digital signal timing (Fig.1), and we design a multi-bit delta-sigma time-to-digital converter (TDC), as shown in Fig.2, exploiting the following features:

1) **Delta-sigma TDC:** Fine time resolution, Small circuit, Digital output (Fig.1)

2) **Multi-bit:** Short measurement time

3) **Data weighted averaging (DWA) algorithm:** High linearity (Figs 3, 4)

We have implemented the multi-bit delta-sigma TDC with analog FPGA (Fig.5), and Fig.6 shows its measurement results. We see that the DWA algorithm improves the overall linearity of the TDC.

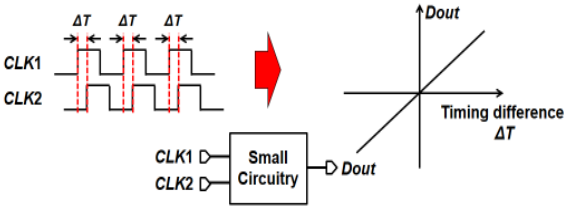


Fig.1 Timing Measurement Circuit

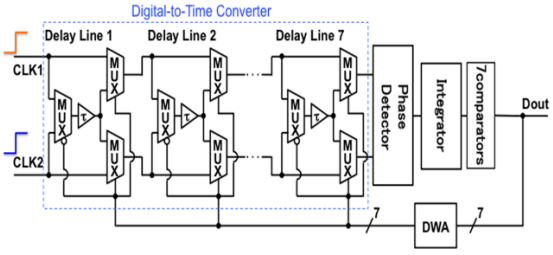


Fig.2. Architecture of a 3-bit ΔΣ TDC

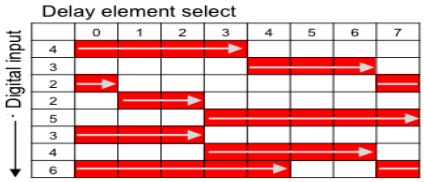


Fig.3. Delay cell selection with DWA

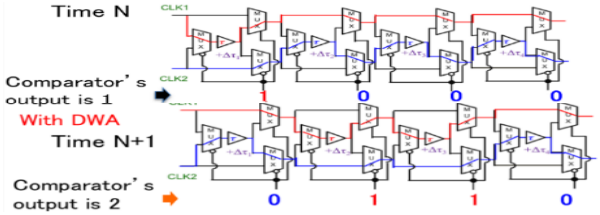


Fig.4. DWA circuit implementation

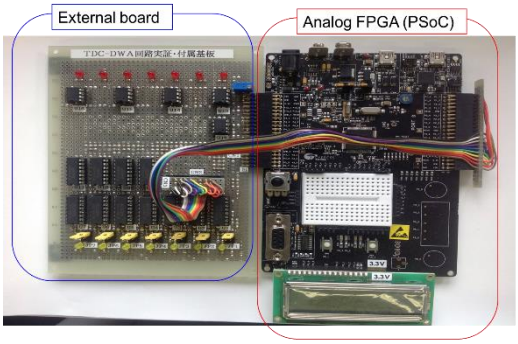
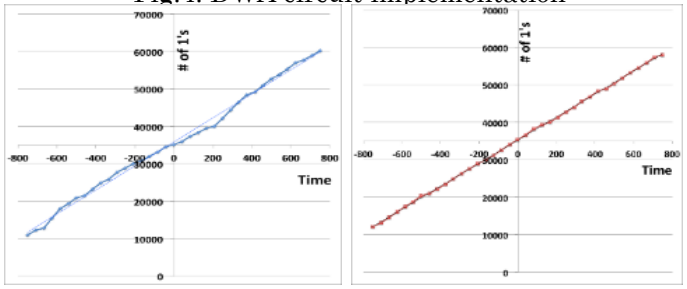


Fig.5 Analog FPGA Implementation



(a)Without DWA (b) With DWA

Fig.6.Measurement results for the 3-bit ΔΣ TDC

[1] S. Uemori, M. Ishii, H. Kobayashi, et. al.,"Multi-bit Sigma-Delta TDC Architecture with Improved Linearity," J. of Electronic Testing, Springer, vo. 29, no. 6, pp.879-892 (Dec. 2013).