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Research on Gate Voltage Dependent 1/f Noise Variance Modeling for n-Channel MOSFETs

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This paper presents 1/f noise variance model in MOSFETs for SPICE3 analog circuit simulators. We derived novel 1/f noise model based on SPICE2 type model and implemented in BSIM4 model on a SPICE3 based circuit simulator (MDW-SPICE).

1/f noise in MOSFET is one of the important characteristics for analog/RF circuit design. For example, 1/f noise is up-converted in frequency domain and degrades phase noise performance of oscillators in wireless transceiver circuits. Fig. 1 shows the tunneling transitions from the Si to the gate oxide and between interface traps. 1/f noise is caused by these traps in energy.

Since existing 1/f noise models are useful only for nominal simulations, we have developed a new model which can simulate noise variance dependent on the gate voltage of a MOSFET.

SPICE2 type 1/f noise model uses eq. (1).

$$S_{I_D}(f) = \frac{KF \cdot {I_D}^{AF}}{C_{OX} \cdot {L_{eff}}^2 \cdot f^{EF}}. \tag{1}$$

Hooge showed 1/f noise generation model in eq. (2), which are considered as mobility fluctuations.

$$S_{I_D}(f) = \frac{\alpha_H \cdot \mu_{eff} \cdot 2KT \cdot I_D}{f \cdot {L_{eff}}^2}. \tag{2}$$

We compared eq. (1) and eq. (2) models and obtained eq. (3).

$$KF = C_{OX} \cdot \mu_{eff} \cdot 2KT \cdot \alpha_{H_{nominal}} \cdot D \cdot e^{-(V_{gs}-V_{th})} \tag{3}$$

1/f noise variability is caused by the device process variation, which we use D as Gaussian Normalized Random Number. α_H is a coefficient caused by phonon scattering and related mobility fluctuation. It decreases with a function of the effective gate to source voltage, so we used exponent. Then our model includes variability model incorporated in mobility fluctuation.

Proposed model has been implemented in BSIM4 model with MDW-SPICE. Parameters of the model are extracted with 1/f noise measurements for simulation verifications. Fig.2 shows simulation and measurement results. We see that the center simulation curves of both gate voltages, which are nominal simulations, agree with measured results accurately. Also for 1/f noise variability with gate voltage, the variance is decreased with increasing gate voltage. Proposed model can accurately simulate the 1/f noise voltage density characterization.

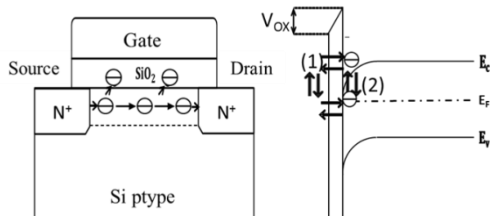

Fig. 1. Schematic illustration and the energy band diagram represent the tunneling transition of electrons between the conduction band and traps in the gate oxide, (1) related to direct tunneling and (2) to indirect tunneling through interface traps.

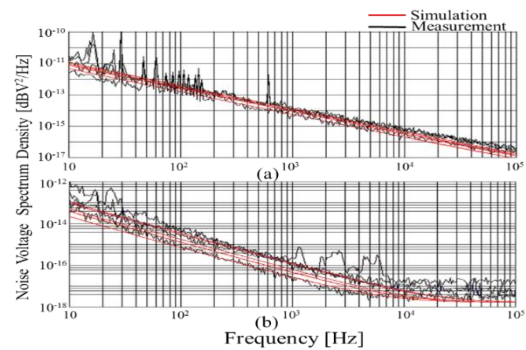

Fig. 2. Simulation and measurement results of drain output 1/f noise voltage density in linear region with (a) V_{gs} = 1.41 V and (b) V_{gs} = 0.45 V. V_{DS} was set to 1.0 V for (a) and (b).