

Segmented DAC Linearity Improvement With Layout Technique Using Magic Square

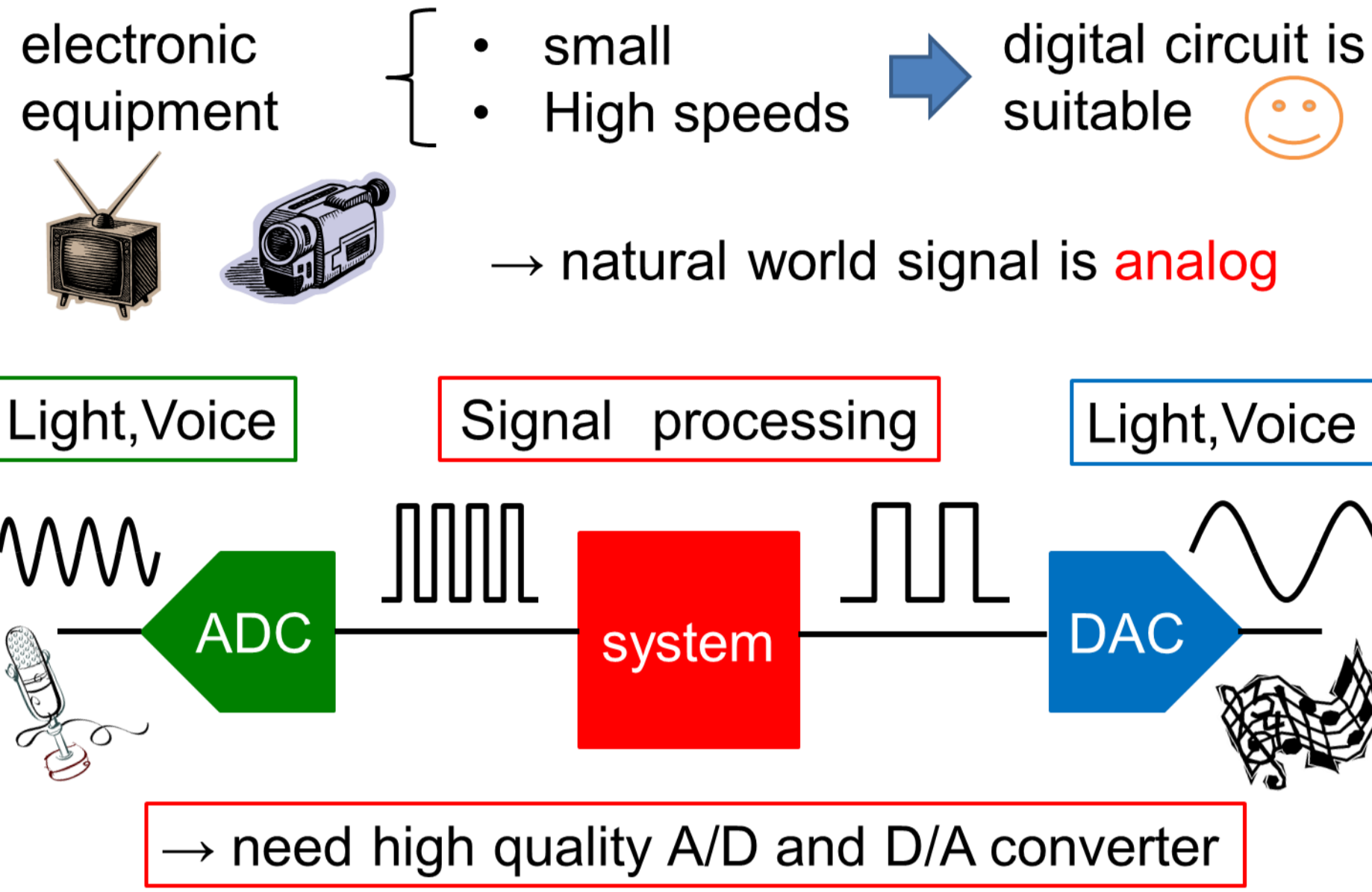
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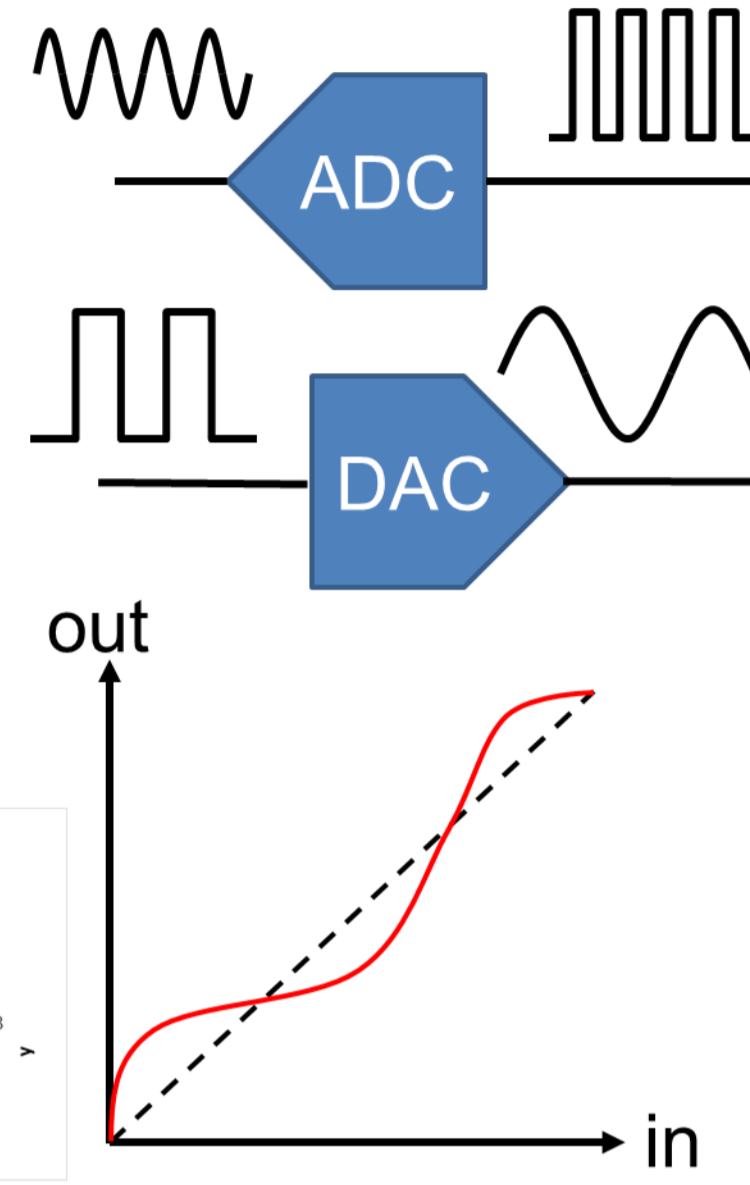
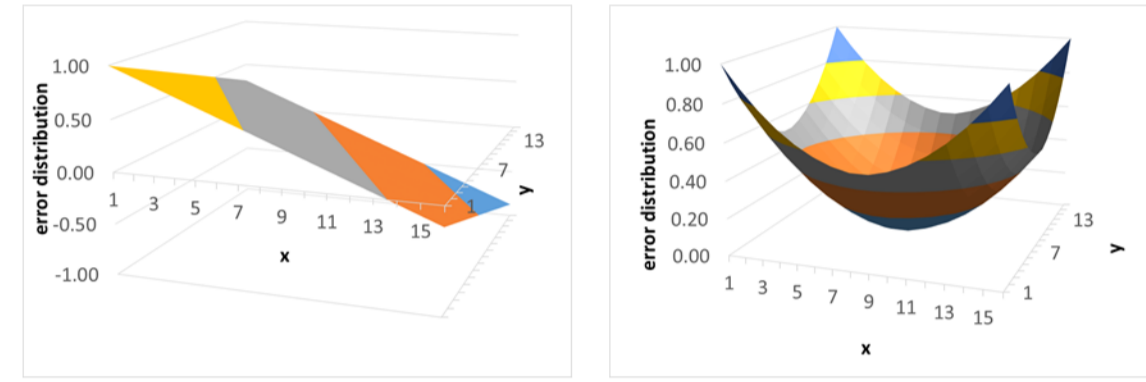
Introduction



Si wafer have mismatch → caused by non-linear ex) MOSFET, resistance, capacitance

Kind of mismatch

- Systematic
- Random

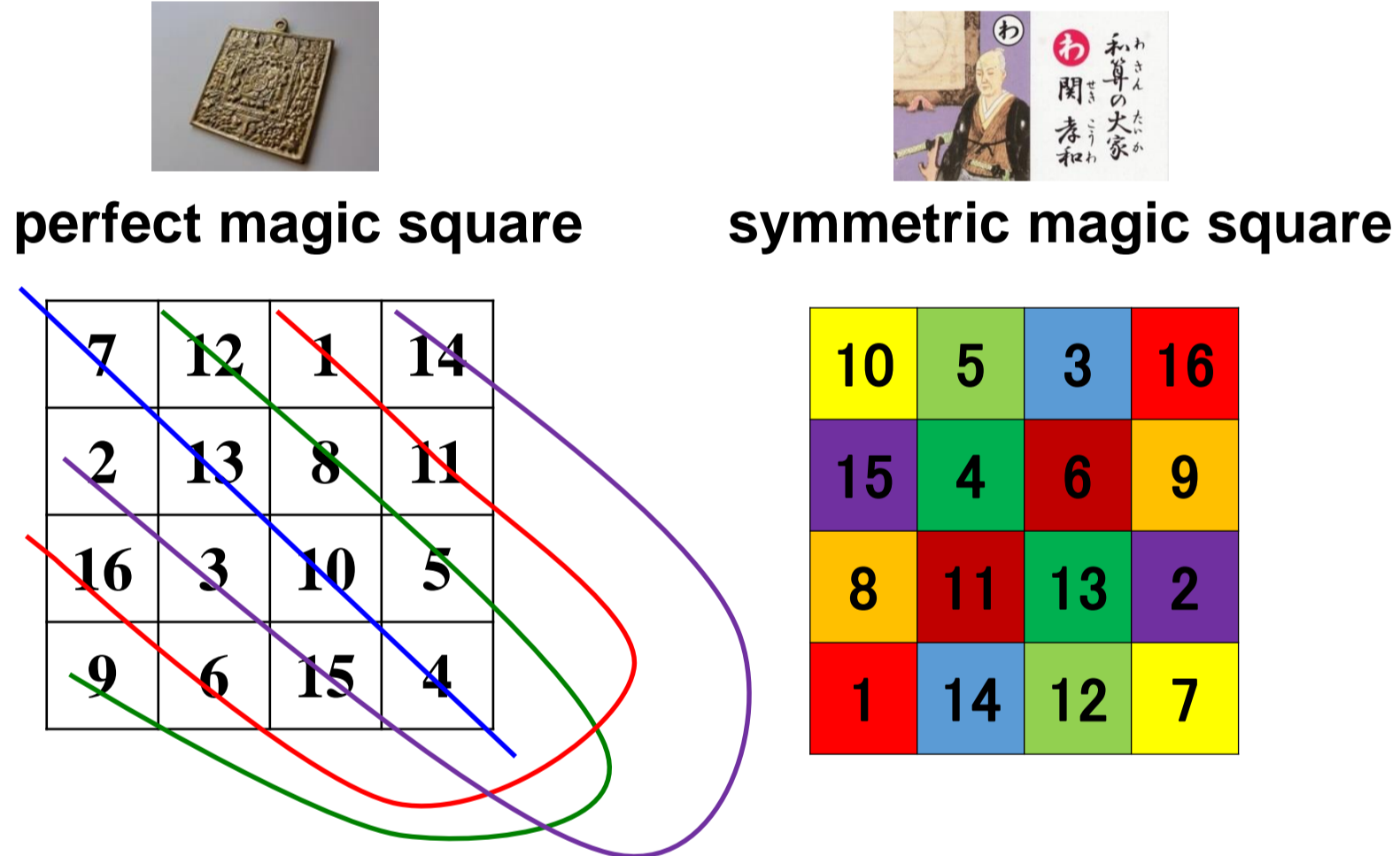


- Systematic mismatch
 - Systematic
 - Random
 - Kind of mismatch
 - Voltage drop
 - Oxide thickness
 - Doping
 - Stress
 - Temperature distribution
 - Wafer
- Linear Error
- Quadratic Error

What's "Magic Square"

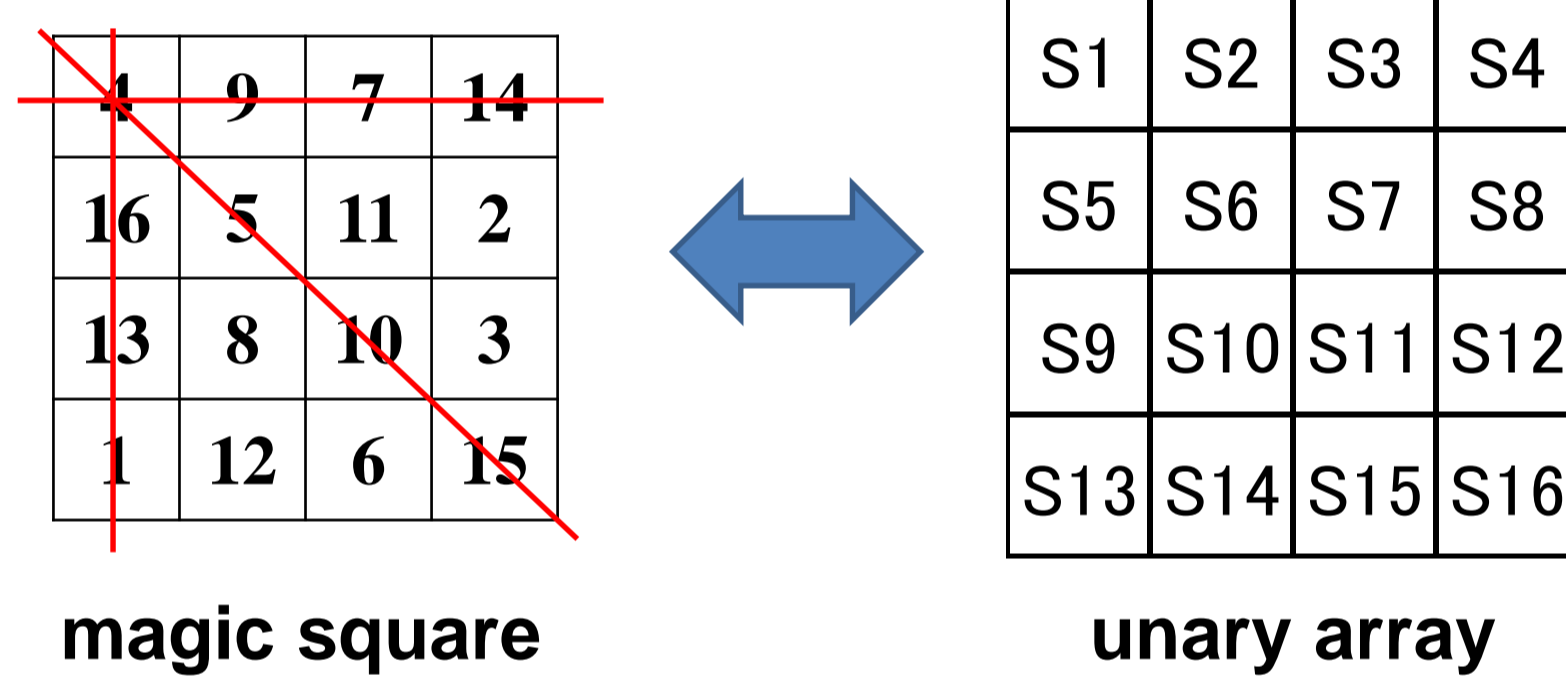
Magic square characteristic

- constant sum of each row, column, diagonal column
- Many kind of magic square



Approach

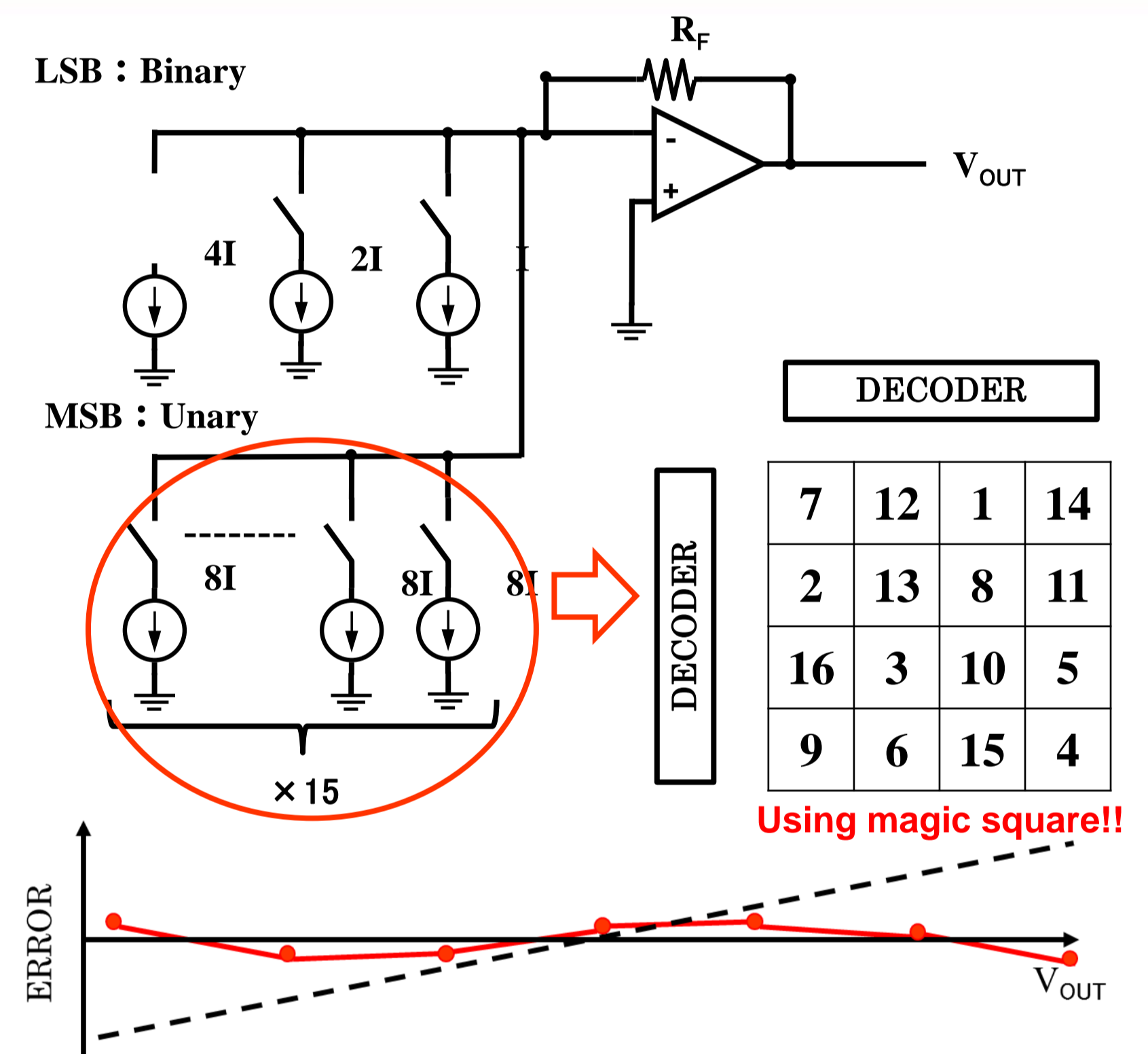
Layout technique using magic square



Characteristic constant sum

→ good balance of current source array layout ☺

Proposal DAC



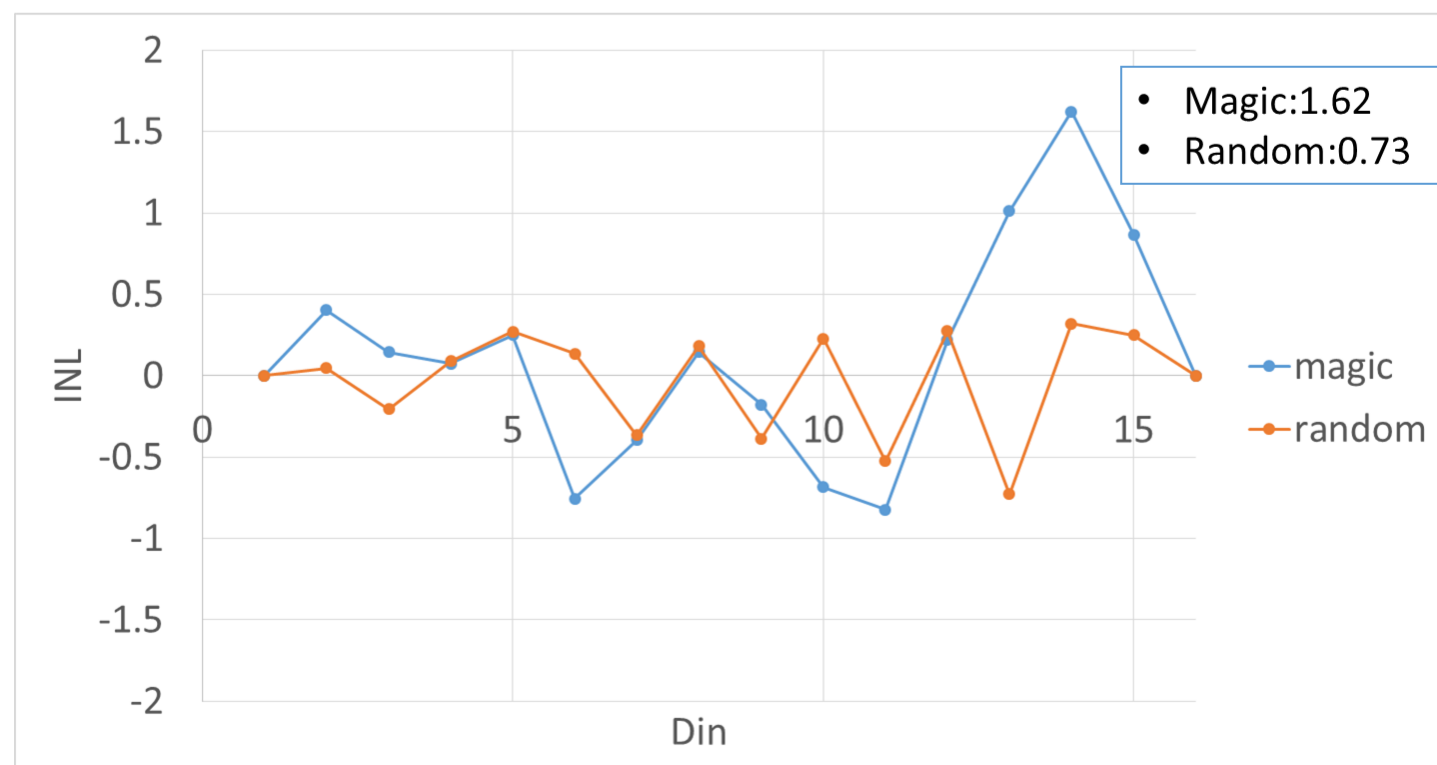
Simulation Result

4bit DAC unary

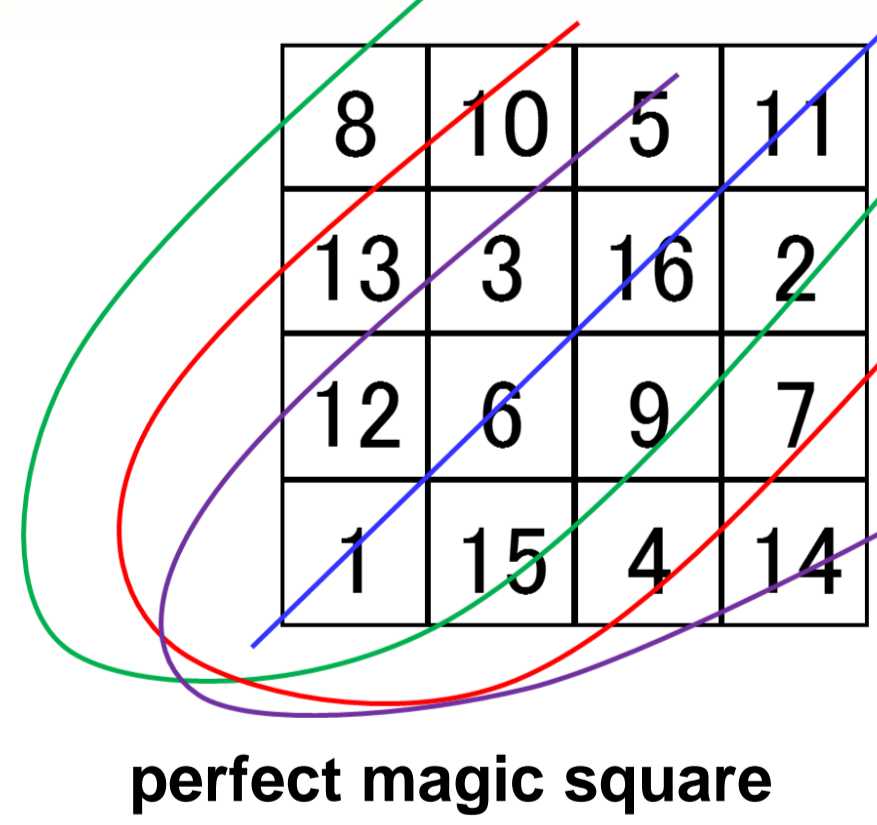
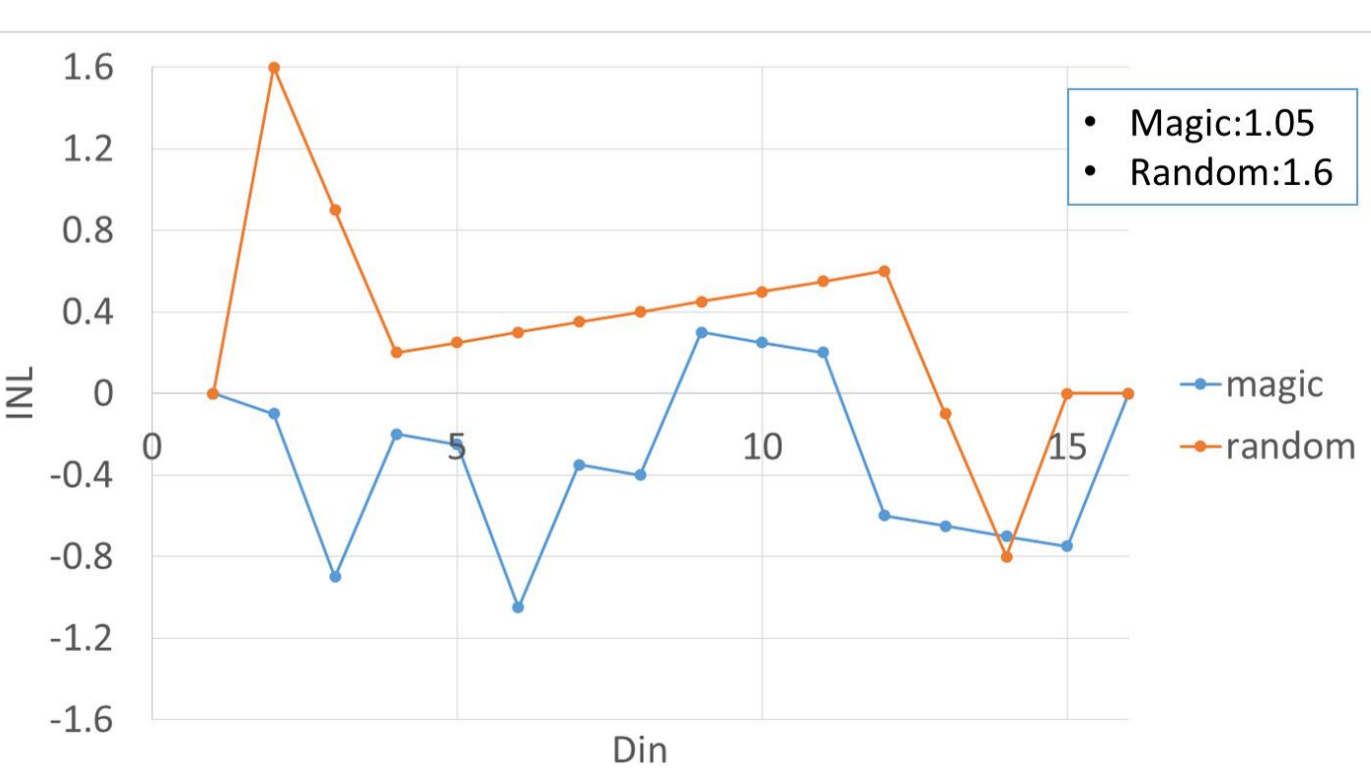
Algorithm using pandiagonal constant sum

→ Linear DAC characteristics

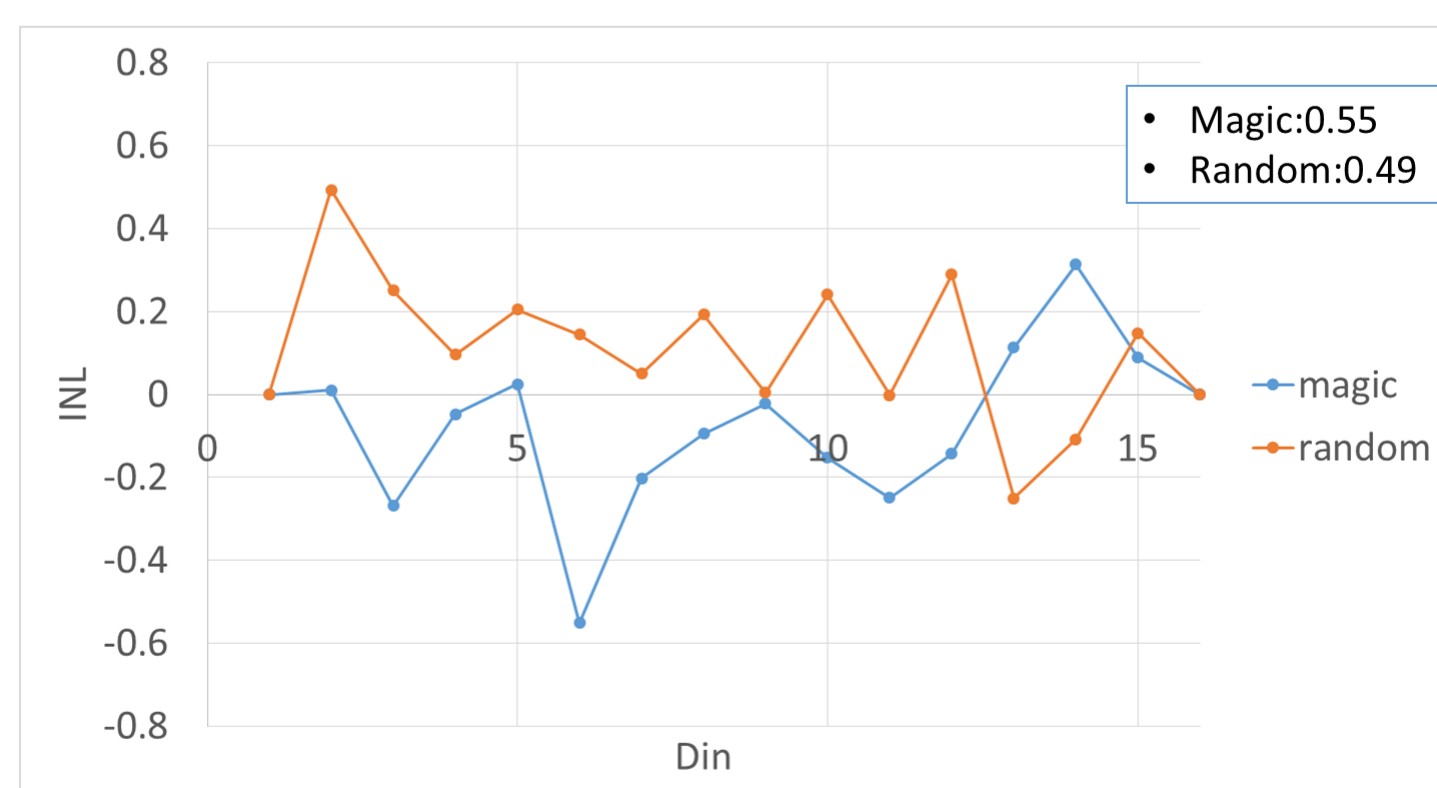
Linear error result



Quadratic error result



Joint error result

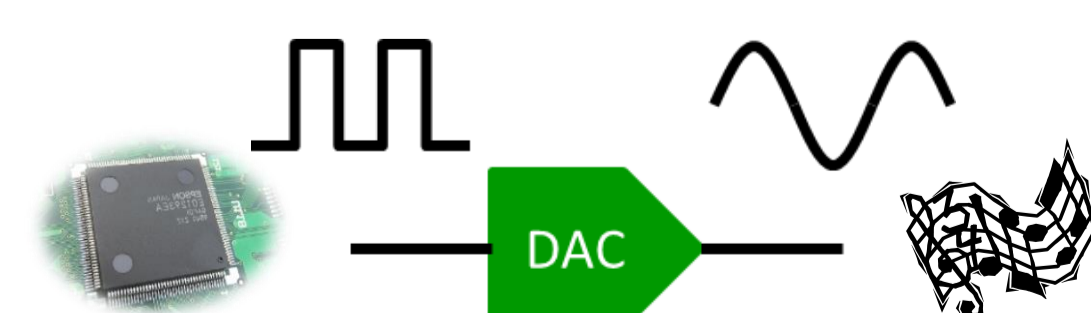


- Linear error ☹
 - Quadratic error ☹
 - Joint error ☹
- Improve linearity : 1.6 → 1.05

Conclusion

- We have proposed a method to reduce the nonlinearity of unary array DAC
 - We have implemented proposed DAC using "magic square" algorithm
 - We compared among magic square, random walk algorithm
 - The proposed algorithm DAC can cancel quadratic error
- INL : 1.60 → 1.05

High Quality DAC!!



Innovation by the classic mathematics

8	10	5	11
13	3	16	2
12	6	9	7
1	15	4	14

