Efficiency Improvement for Switching Power Supply at Light Load Using DSP Control

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With a rising consideration toward “Green IT”, it is becoming important to improve the energy efficiency of electrical systems especially the server power supply. In this paper we mainly attempt to improve the efficiency of power supplies at half-load and light load under 20% using digital control.

The server power supply is mainly made up of two parts: an AC/DC part with PFC (Power Factor Correction), and a DC/DC part to achieve a desired DC output voltage. Although PFC improves the power factor to approach 1, it also brings a output voltage much higher than its input voltage. Actually, despite of the possible range of input voltage, the output voltage is fixed at the peak value of \(265\times\sqrt{2}=390\text{V}\), which is unnecessary high. At the same time, other factors for the losses lie in the other components in the circuits mainly include diode loss and MOSFET loss\textsuperscript{[1]} which mainly happen during the moment of switching. Diode loss occurs when turning off the diode, which is called the recovery loss. As for the MOSFET, losses occur because of the current that may flow during the transition time. As a result, we will also discuss the switching frequency in the circuits to see if these losses can be alleviated.

The experimental environment we adopt is by using a development tool named CCS and two experiment boards shown below:

\begin{itemize}
\item CCS v5 is an integrated development environment for embedded processor provided by TI.
\item BL-PFC (Bridgeless PFC) AC/DC kit: the output voltage (link voltage) is fixed at the value of 400V. the PWM frequency is fixed at the value of 200kHz.
\item PSFB (Phase shifted Full Bridge) DC/DC kit: the PWM frequency is fixed at the value of 100kHz.
\end{itemize}

The experiment is conducted in three steps: first we attempt to change the link voltage of the AC/DC part, and then we deal with the PWM frequency of both parts.

From Fig. 1, it can be seen that the PFC efficiency gradually rises when the link voltage decreases. So by the link voltage the efficiency can be improved if appropriate (lower) boost ratio is chosen. In Fig. 2, instead of a steady frequency covering all the load rate, we find appropriate frequency corresponding to each load range. For example, if the load rate is between 5 and 10%, the efficiency of 150kHz is about 2% better than 200kHz. And when the load rate reaches 20%, the frequency is set back to 200kHz. In Fig. 3, we can see that 70kHz performs better than the conventional 100kHz. The efficiency is promoted by about 3%.

\textsuperscript{[1]}Hata Naotaka, Takahiko Shimada, time “Loss calculation of power converter circuit and an inductor in DC/DC, Technical Report 2009, No. 21