Phase Noise Measurement Technique Using Delta-Sigma TDC Without Reference Clock

Yusuke Osawa, Daiki Hirabayashi, Naohiro Harigai, Haruo Kobayashi

Osamu Kobayashi †, Kiichi Niitsu ‡,

Division of Electronics and Informatics, Gunma University, Kiryu 376-8515 Japan email: k_haruo@el.gunma-u.ac.jp
† Semiconductor Technology Academic Research Center (STARC) , Yokohama 222-0033 Japan
‡ Graduate School of Engineering, Nagoya University, Nagoya 464-8603 Japan

Background

Conventional Phase Noise Measurement

- Expensive spectrum analyzer
- Long measurement time (~10seconds)
- LSI mass production test

Significant test cost

Research Objective

Measurement the phase noise without using a spectrum analyzer

Low Cost & High Quality Test

Phase Noise

Ideal Phase-Locked Loop (PLL)

Actual Phase-Locked Loop (PLL)

Phase Noise = Various frequencies

cause an error in the system

It is necessary to measure the noise amount

Block Diagram of Delta-Sigma TDC

Principle of Phase Noise Measurement With Reference Clock

Phase Noise Measurement Technique Without Reference Clock

Analytical Discussion

MATLAB Simulation

Simulation Results ( I & II )

Simulation Result ( III )

Comparison of Simulation Results and Theory

Simulation Result ( IV )

Delay BT = 0.95T (Error -5%)

Delay BT = 1.05T (Error +5%)

Simulation Conditions

Case

Delay of ΔΣTDC [ps]
Input frequency [MHz]
The number of ΔΣTDC data
Phase variation of CUT

Delay of ΔΣTDC [ps]
Input frequency [MHz]
The number of ΔΣTDC data
Phase variation of CUT

Simulation

Power [dB]

Frequency [kHz]

Simulation

Power [dB]

Frequency [kHz]

Conclusion

Proposal of phase noise measurement techniques using ΔΣTDC without reference clock

- Low cost testing without spectrum analyzer
- On-chip high precision phase noise measurement
- Fine time resolution measurement with ΔΣTDC
- Power spectrum obtained by FFT of ΔΣTDC digital output

Their MATLAB simulation verification

- Superposition of several sinusoidal phase variation components
- Comparison with theoretical analysis and simulation results
- Measurement method with several delay β values

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