P087 Reliability Modeling on 90 nm n-channel MOSFETs with BSIM4 Dedicated to HCI Mechanisms

Takuya Totsuka¹⁾, Hitoshi Aoki¹⁾, Fumitaka Abe¹⁾, Khatami Ramin¹⁾, Yukiko Arai¹⁾,

Shunichiro Todoroki¹⁾, Masaki Kazumi¹⁾, Wang Taifeng¹⁾, Haruo Kobayashi¹⁾,

¹⁾ Gunma University 1-5-1 Tenjin-cho, Kiryu 376-8515, Japan

Research Goal

Background

Generation Principle of 1/f noise

Dominant in the low frequency

Electrons are trapped in the channel

Developed MOSFET model

HCI induced DC degradation model

Show degradation **DC** characteristics

1/f noise model

Show deterioration 1/f noise at DC





- Manufacturing Variations
- **Degradations of Circuit Performance**



Large \Rightarrow Small

Hot Carrier Injection (HCI)

Reaction-Diffusion model (RD model)

- Modeled hot carrier effect



Due to Time and Temperature

Id-Vg Characterizations

Degradation

vg[V]



Conditions for Our Experiments

90 nm process n-channel MOSFET Large Channel Width 10.0µm Channel Length 10.0µm



Measurement and Simulation Environment

Short Channel Width **10.0µm** Channel Length 0.1µm

Stress condition

Degradation parameter is based on 65nm process device's, whereas our device is fabricated with 90nm process

 Temperature 300.15 [K] • Time **1,000** [hours]

> **Measurement and Simulation of Drain Output 1/f Noise Density**





Summary

- •HCI degradation model was studied and implemented in BSIM4 of our MDW-SPICE simulator
- BSIM4 and degradation model parameters were extracted with measurements of 90nm n-channel MOSFETs
- Simulation verifications of DC drain currents were performed with and without bias stresses
- 1/f noise model parameters

were extracted with measurements

- Simulation verifications of drain output 1/f noise density
- were performed with and without bias stresses

[1] S. Todoroki, H. Aoki, F. Abe, K. Ramin, Y. Arai, M. Kazumi, T. Totsuka, H. Kobayashi, "1/f Noise Variance Modeling of Gate idence with n-channel MOSFETs," Institute of Electrical Engineers Japan (IEEJ). ECT-14-010 Kanazawa (Jan, 2014)

[2] H. Aoki, M. Shimasue, Y. Kawahara, CMOS Modeling Technology, Maruzen Publishing, (2006).

[3]H. Aoki, "Bias and Geometry Dependent Flicker Noise Characterization for n-MOSFETs," IEICE Trans. Electronics, vol. E85-C, no.2 pp.408-414(2002).

[4] Information on http://www-device.eecs. berkeley.edu/bsim/

[5] C. Hu, et al. "Hot-electron induced MOSFET degradation model, monitor, and improvement," Trans. Electron Devices, 32(2), 375-385, 1985,

[6] E. Maricau and G. Gielen, Analog IC Reliability in Nanometer CMOS, Springer Science Business Media New York, 2013.

[7] H. Kufluoglu and M. A. Alam, "A unified modeling of NBTI and hot carrier injection for MOSFET reliability," 10th International Workshop on Computational Electronics, pp. 28-29, Oct. 2004.

[8] H. Aoki and M. Shimasue, "Noise Characterization of MOSFETs for RF Oscillator Design," Proc. 1999 IEEE MTT-S International Microwave Symposium, Anaheim CA, (Jun. 1999).