Digital Calibration Algorithm for Half-Unary Current-Steering DAC for Linearity Improvement

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Abstract

This paper introduces an algorithm called 3-stage current sorting (3S-CS) in half-unary weighted current cells to improve the linearity of a current-steering digital-to-analog converter (DAC). Based our statistical analysis and simulation results, the proposed algorithm improves the DAC static linearity as well as its dynamic performance.

Keywords- current-steering DAC, current source mismatch, linearity, current sorting, half-unary weighted

Introduction

The random error among current sources is one of fundamental problems in current-steering DACs. Its effect is deteriorating both static and dynamic DAC performance. Reduction of the current source mismatch effects is becoming important. Most of previous works have shown that the effect of these errors can be reduced by proper mapping or/and calibration techniques [1]. In this paper, we propose a half-unary current steering DAC with a 3S-CS algorithm as calibration technique to deal with this problem. Our MATLAB simulation shows that our proposed algorithm reduces both integral and differential non-linearity errors, and as a result, better spurious free dynamic range (SFDR) is achieved. The comparison has been done with a conventional unary, a unary and half-unary with 2-stage current sorting (2S-CS) in case that the static current source mismatches are considered.

DAC architecture

A unary weighted architecture of the current-steering DAC is introduced to overcome the binary-weighted disadvantages of large glitch energy and non-monotonicity. However, since the unary weighted structure has 2^N-1 unit current sources with identical weight for N-bit resolution, it suffers from low sampling speed and consumes large silicon area due to its decoding circuit. However, to increases intrinsic accuracy of this DAC architecture, we propose here another architecture called a half-unary weighted of the current steering DAC which is doubled in number of current source cells with halved weight compared to the conventional unary. This architecture offers better in term of glitch energy and redundancy than the conventional unary structure. However, since its number of current sources is double, the consumed silicon area and complexity in terms of decoder and routing is remained. Therefore, by manipulating its advantages and taking care of its weakness, we assume the combined architecture, but for SFDR improvement, the segmented part for the higher bits which more important and hence our discussion here focuses on the half-unary structure.

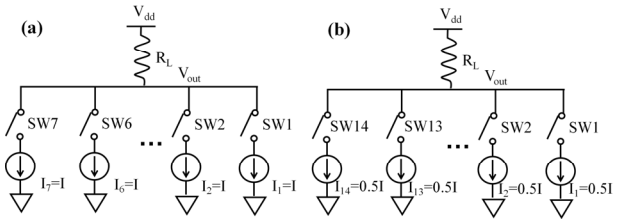

Fig. 1 A 3-bit DAC architecture. (a) Unary. (b) Proposed half-unary.

DAC nonlinearity

A. Current source mismatch

In actual CMOS technologies, the current source mismatches are influenced either by the threshold matching, ΔV_{th} or by the slope mismatch, $\frac{\Delta\beta}{\beta}$. Since both are dependent on devices size ($\sqrt{WL}$), it is possible to alleviate them by changing the device size. However, without proper matching due to their limited variations, they will increase the device capacitances, which require more biasing current and thus power. So, we consider to reduce these effects after fabrication process.

Proposed algorithm

A. 3-stages current sorting

Current sorting algorithms have been used in several published works in order to reduce the effect of random static errors [2, 3]. These algorithms intend to optimize the switching selection [2]. In [3], this kind of algorithm is used to form binary weighted current cell from a group of unary current cells. In our work, we have merged these two methods, called as a 3-stage current sorting (3S-CS) algorithm. It is divided into two main stages: combine and rearrange. Fig. 2 shows an example of 3-bit of half-unary weighted current cells. Firstly, the 14 available current source cells (doubled number of conventional unary weighted structures) will be sorted by their current values. Then, by associating the smallest and the largest values (in this case, I_3 and I_7) to form a virtual unary weighted cell during conversion. Followed by the second smaller, I_{14} is combined with the second larger value, I_{10}. Next, the third weighted cells have their own pairs. The second and third stage, smaller, I_{11} and the third larger, I_4 and so on until all half-unary sequence determination. This kind of procedure is benefited for reducing the integral nonlinearity (INL) and differential

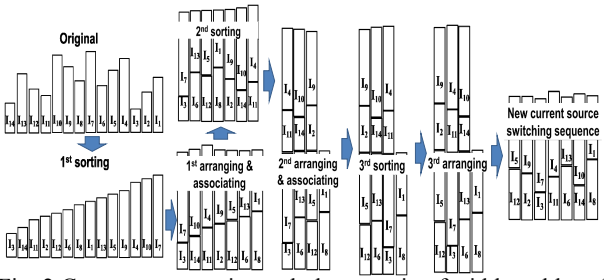

Fig. 2 Current source mismatch due to ratio of width and length of MOSFET transistor

nonlinearity (DNL) errors. Thus, a better linearity performance can be achieved.

B. Calibration

The calibration with error measurement approach is chosen to meet with our proposed techniques. Through foreground calibration mode, the overall calibration flow is shown as in Fig. 3 (left). A ring oscillator based measurement circuit located in the center of the current source is used to perform current measurement (Fig. 3 (right)). However, the accuracy of this measurement circuit becomes a trade-off with the overall area and DAC performance itself. Since, this current measurement circuit is fully digitalized implementation, it can be small size and low power consumption. After measurements, all measured values are stored in memory which later will be fed to digital calibration circuit to perform current cell sorting and switching rearrangement. The optimized switching sequence will be stored in memory and used during conversion. A look-up table (LUT) based decoder is used to decode binary code to the address of memory that contains the switch code. So, the switches will be configured as loaded codes. This process continues for all digital input. In order to reduce routing complexity and parasitic effects, a clock tree like (equal routing distance) layout has been taken place (Fig. 3 (right)). As a result, the overall dynamic performance of the proposed DAC is also improved. Fig. 3 (right) also illustrates floor plan of our proposed DAC architecture.

Results

Half-unary current-steering DACs with 8 to 12-bit has been simulated using Matlab where only static current source mismatches are considered and glitch effects are not. Fig. 4(a) and Fig. 4(b) show the static characteristics of INL and DNL which obtain better integral and differential linearity after calibration. Fig. 4(c) and Fig. 4(d) show that the SFDR performance obtains more than 15 dB while second and third harmonic distortions are significantly suppressed at condition

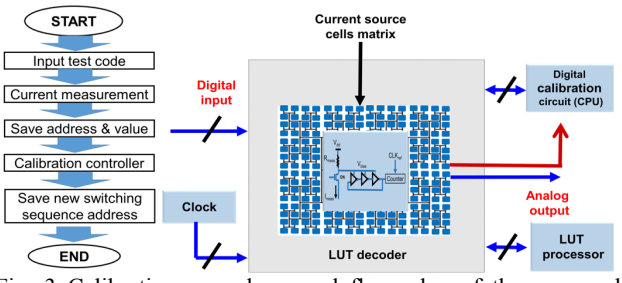

Fig. 3 Calibration procedures and floor plan of the proposed DAC.

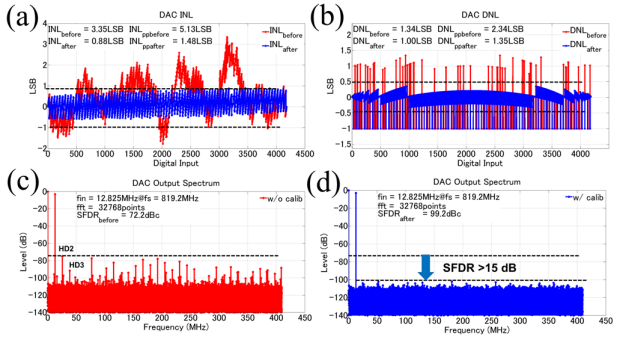

Fig. 4 A 12 bit DAC. (a) INL. (b) DNL. (c) Output spectrum before calibration. (d) Output spectrum after calibration

TABLE I
SUMMARY OF 12 BIT DAC PERFORMANCE

Architecture		Unary		**This work**	
Switching scheme		TC	2S-CS	2S-CS	3S-CS
Static	INL	3.99	1.06	1.01	0.93
	DNL	1.34	1.34	1.13	1.13
Dynamic	SFDR, dBc	66.6	85.8	86.3	91.6
	HD2, dB	-71.1	-88.6	-88.2	-94.6
	HD3, dB	-74.6	-96.1	-94.7	-102.0

of frequency input 12.8 MHz and sampling frequency of 819.2MHz with 0.075A of standard deviation error after calibration. For comparison, the conventional unary with thermometer-coded (TC) switching scheme, unary and half-unary with 2S-CS are also simulated. All simulation results in the same conditions are summarized in Table I. Both INL and DNL are improved compared to conventional unary and unary with 2S-CS. While, 3S-CS shows further INL improvement compared to 2-stages. The dynamic performance also improved using the proposed architecture.

Conclusion

We have proposed a 3-stage current sorting algorithm for a current steering DAC linearity improvement as well as its dynamic performance. By implementing this technique with MATLAB simulation, we have obtained SFDR of more than 15 dB compared to conventional unary with thermometer-coded switching scheme. The third of the harmonic distortion is also successfully suppressed.

Our proposed technique is simple and can be digitally implemented. The accuracy measurement circuit in this work is the key of the overall DAC performance.

Acknowledge

We would like to thank Semiconductor Technology Academic Research Center (STARC) for their valuable support on this project.

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