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群馬大学
GUNMA UNIVERSITY

# Digital Calibration Algorithm for Current-Steering DAC Linearity Improvement

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**November 5, 2014**

# Outline

- Introduction
- Problem Statement
- Proposed Techniques
  - Half-Unary Current-Steering DAC
  - Current Source Sorting
  - Circuit & Layout
- Simulation Result
- Conclusion

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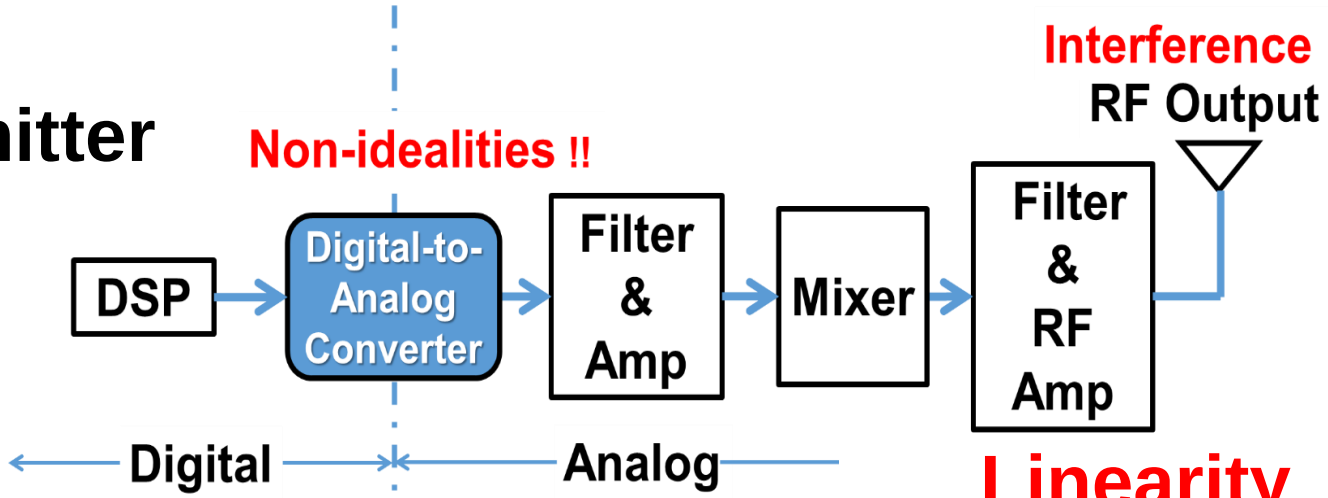
# Introduction

- **Background**
  - **Telecommunication devices**
    - **Mobile phones, wireless modems & avionics**
    - **High-speed, high-accuracy digital-to-analog converter (DAC)**

- **Problem**
  - **Transmitter**


**Linearity degradation!!!** ☹

# Objective & Investigated Method

- **Objective**
  - **High SFDR current-steering DAC for communication**
- **Proposed method**
  - **Current source mismatch effect reduction**
    - **① Half-unary DAC architecture**
    - **② Current source sorting algorithm**
      - **➔ Static linearity improvement**
  - **Layout strategy**
    - **① Clock-tree-like layout of current sources & switches**
      - **➔ Dynamic linearity improvement**

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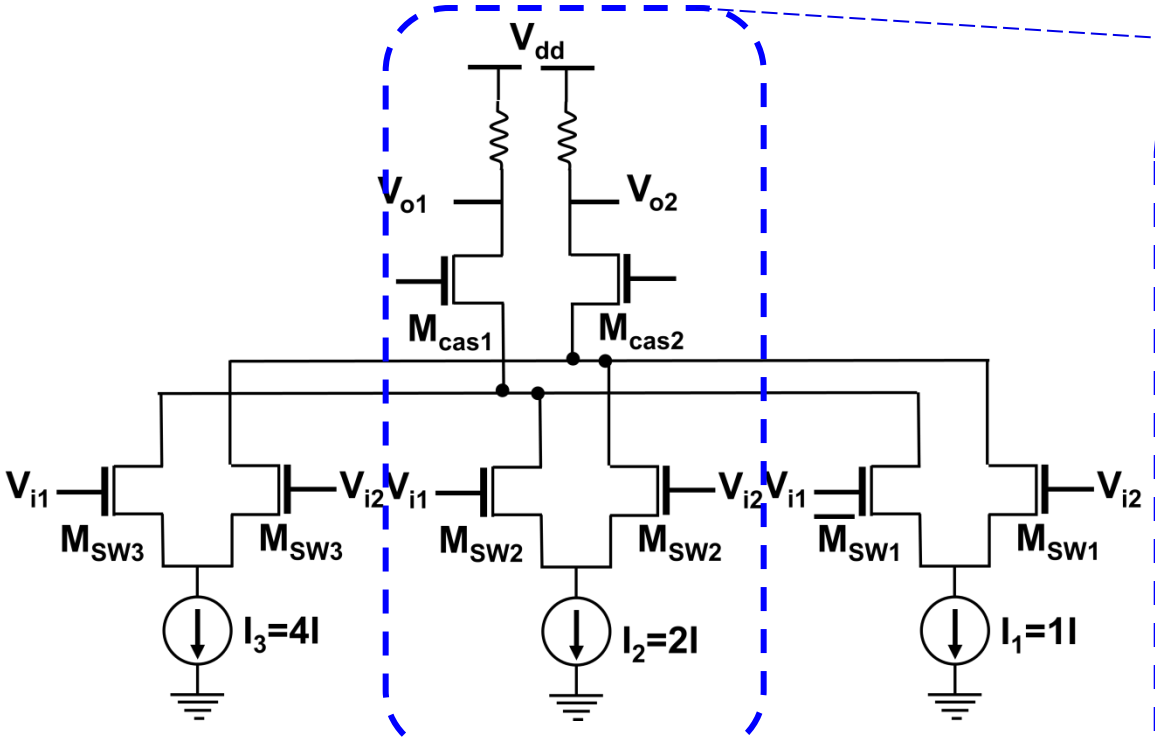
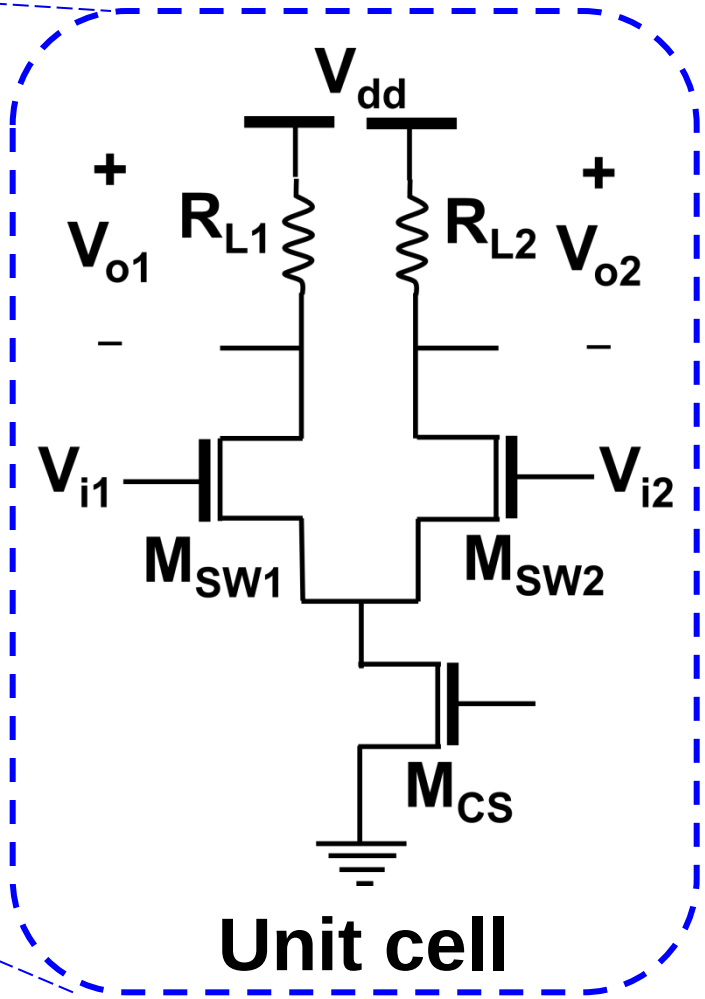
# Current-Steering DAC

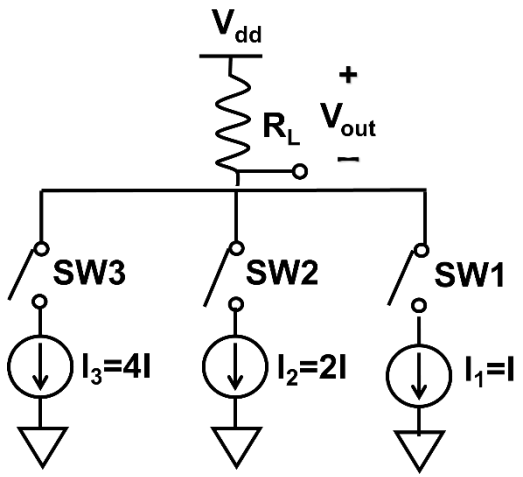


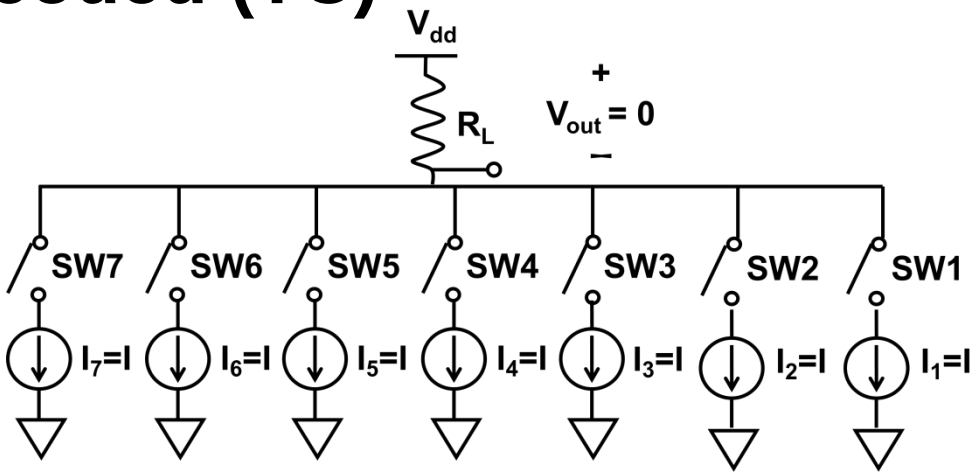

- High speed
- High resolution
- Small chip area

# Binary versus Unary CS DAC

- **Binary**
  - Small silicon area ☺
  - High speed ☺
  - Large glitch energy ☹




- **Unary / Thermometer-coded (TC)**
  - Small glitch energy ☺
  - Redundancy ☺
  - Low speed ☹
  - Large silicon area ☹



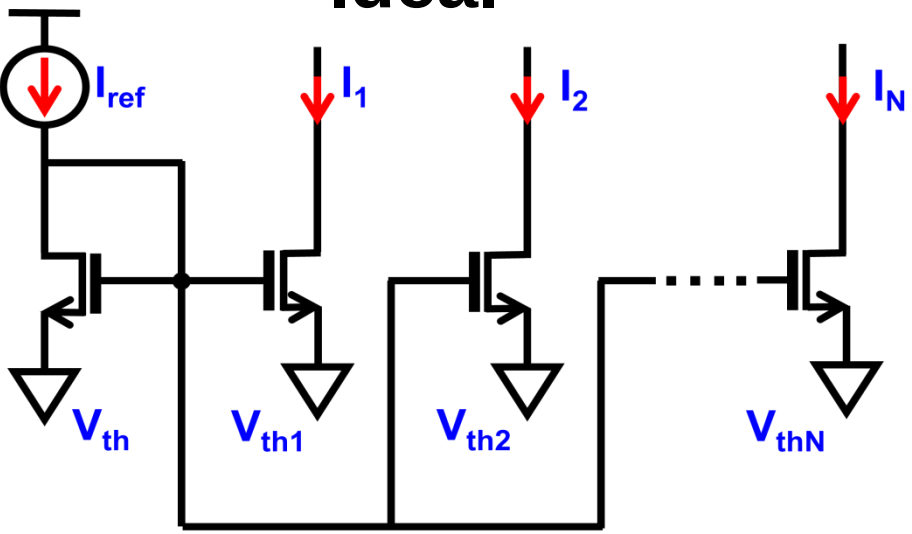

➔ **Segmented for balanced performance !!! 😐**

# Current-steering DAC Limitation

- **Transistor matching error**
  - **– Amplitude errors - current sources**
    - **Dominant at low input frequency**
  - **– Timing errors (delay, duty cycle) – switches**
    - **Dominant at high input frequency**
  - **➔ DAC static & dynamic non-linearity**
- **Better transistor matching**
  - **– Large size ➔ Power loss ☹**
  - **– Laid out close to each other ➔ Complicated ☹**

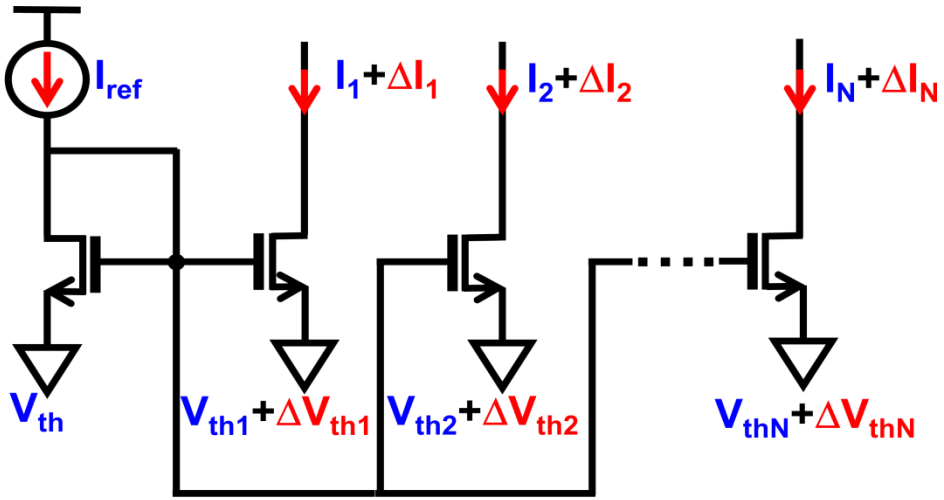
# Current Source Mismatch

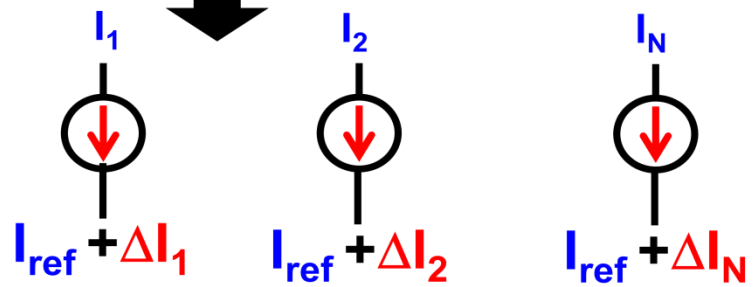
## Ideal




$$V_{th} = V_{th1} = V_{th2} = \ldots = V_{th2}$$
$$\rightarrow I_{ref} = I_1 = I_2 = \ldots = I_2$$

## Mismatch




$$V_{th} \neq V_{th1} \neq V_{th2} \ldots \neq V_{thN}$$
$$\rightarrow I_{ref} \neq I_1 \neq I_2 \neq \ldots \neq I_N$$

- **Threshold voltage mismatch**
- **Mirrored current source structure**

**Current source mismatch!!!** ☹

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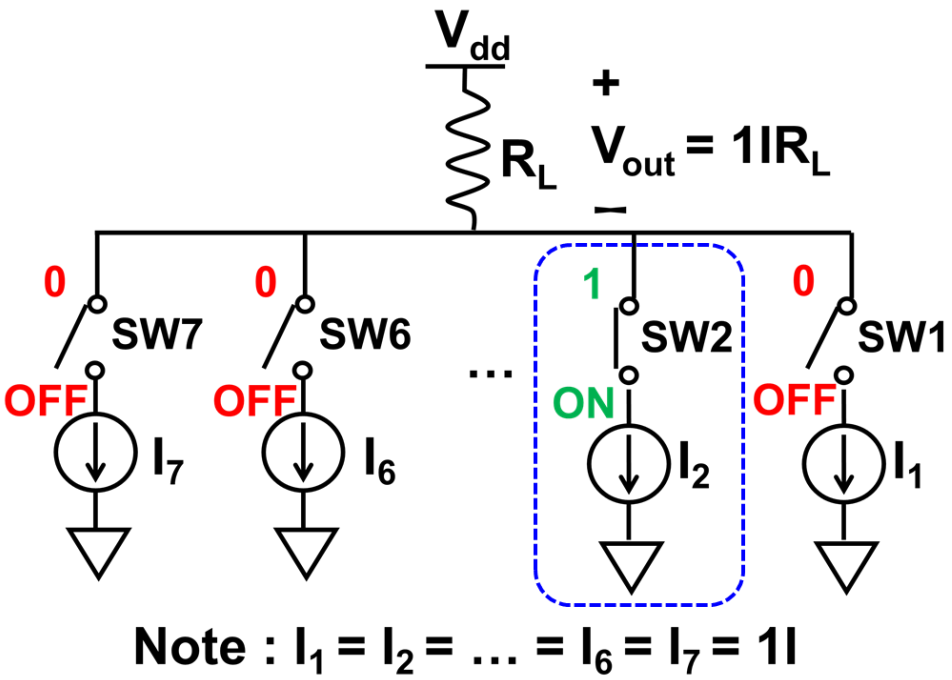
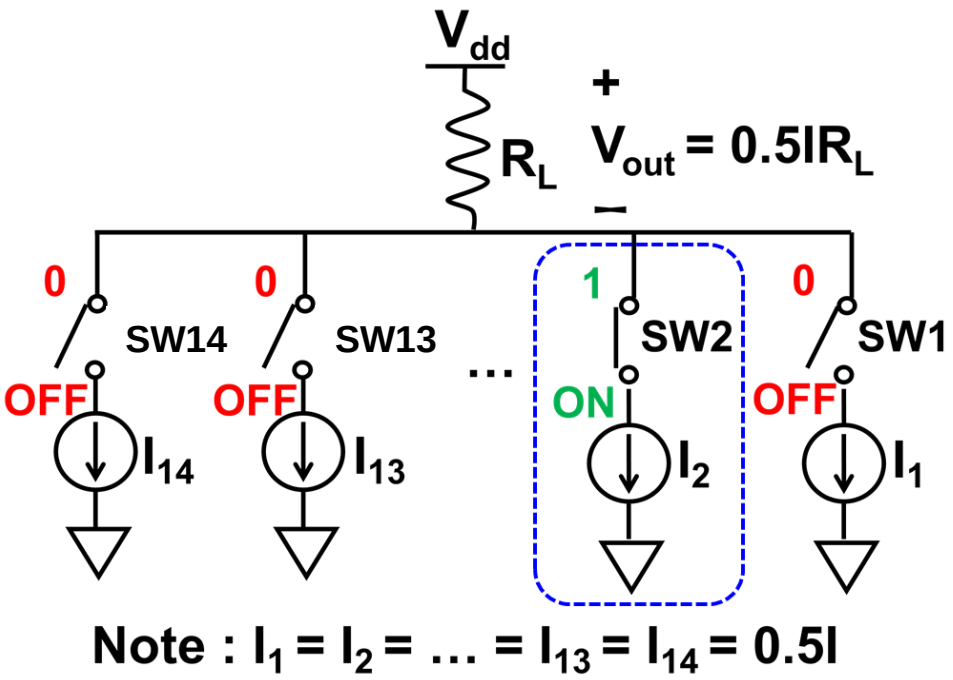
# Why half-unary?




Note : $I_1 = I_2 = \ldots = I_6 = I_7 = 1I$




Note : $I_1 = I_2 = \ldots = I_{13} = I_{14} = 0.5I$

| | Unary | Half-unary |
|---|---|---|
| Number of CS | $2^N-1$ | $2(2^N-1)$ |
| Current value | I | 0.5I |

N : number of bit

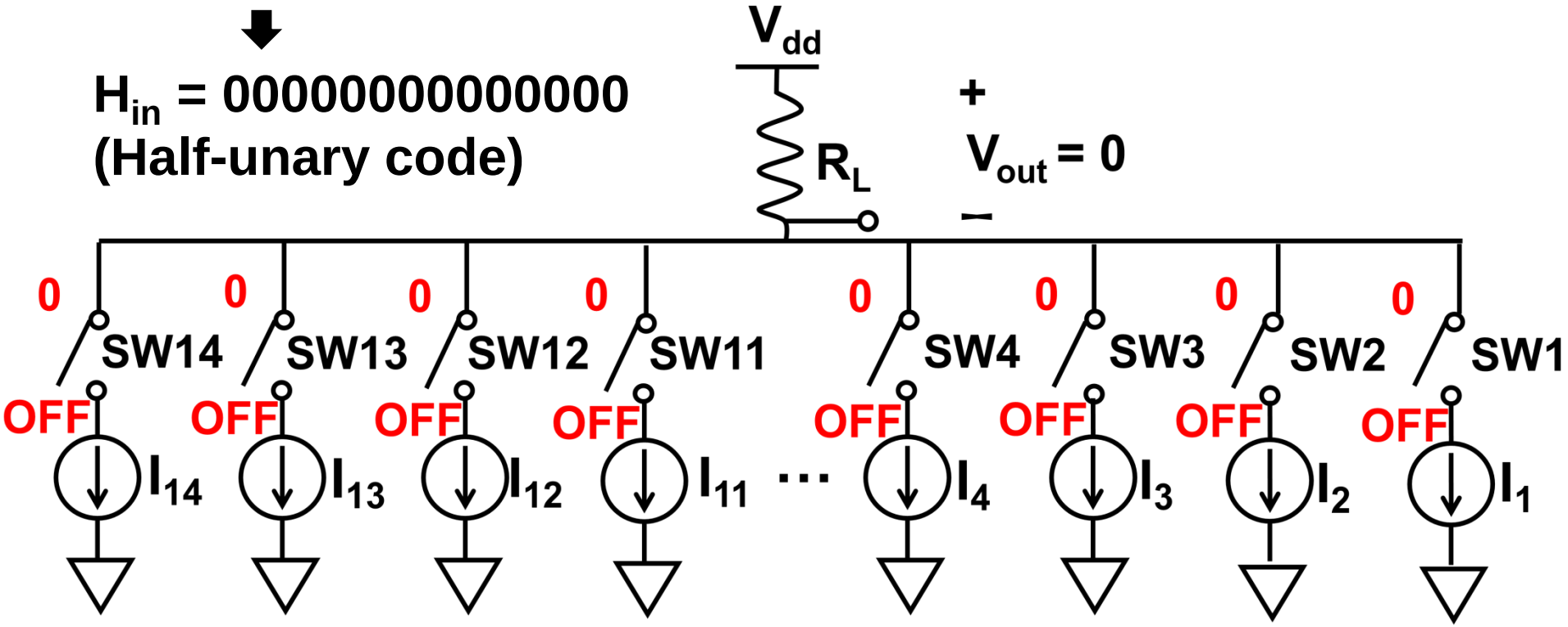
# How half-unary works?

**Initial condition:**

$B_{in}$ = 000 (Binary code)

⬇

$H_{in}$ = 00000000000000
(Half-unary code)



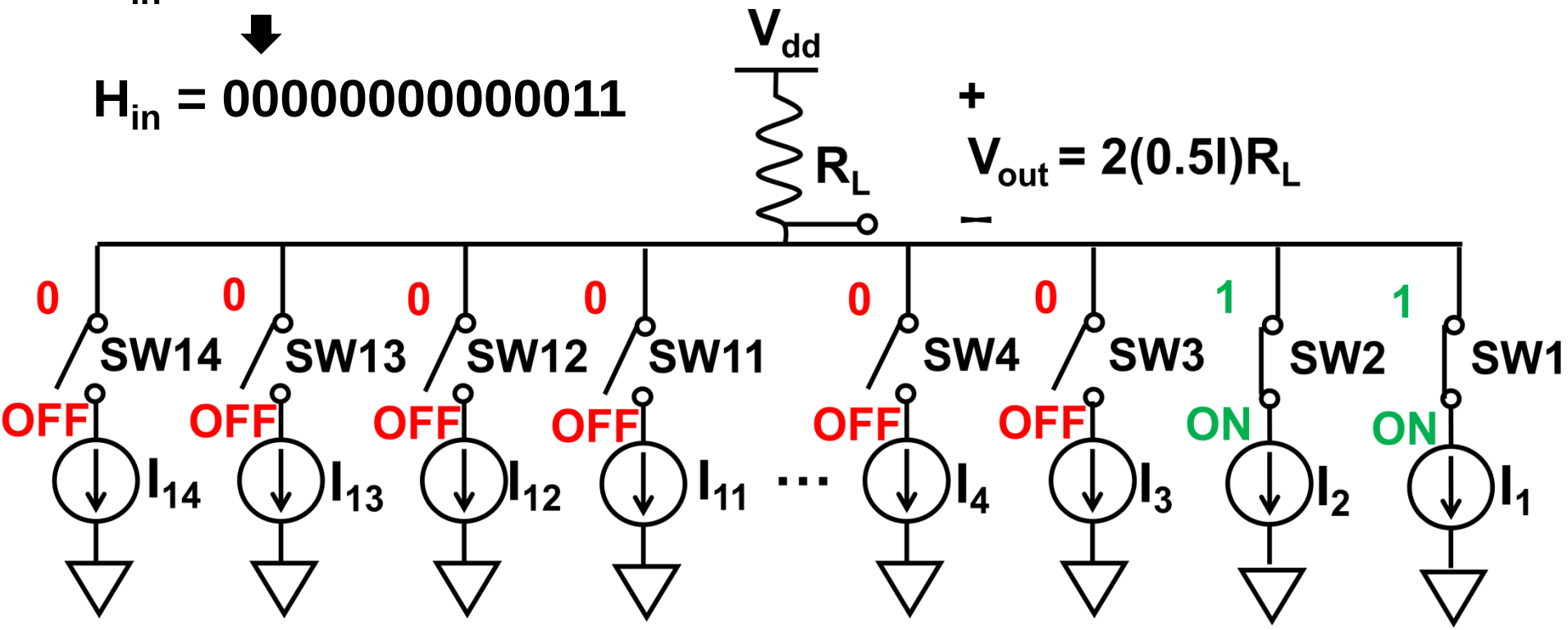

Note : $I_1 = I_2 = \ldots = I_{13} = I_{14} = 0.5I$

# How half-unary works?

**Clock 1:**

$B_{in}$ = 001

$H_{in}$ = 00000000000011



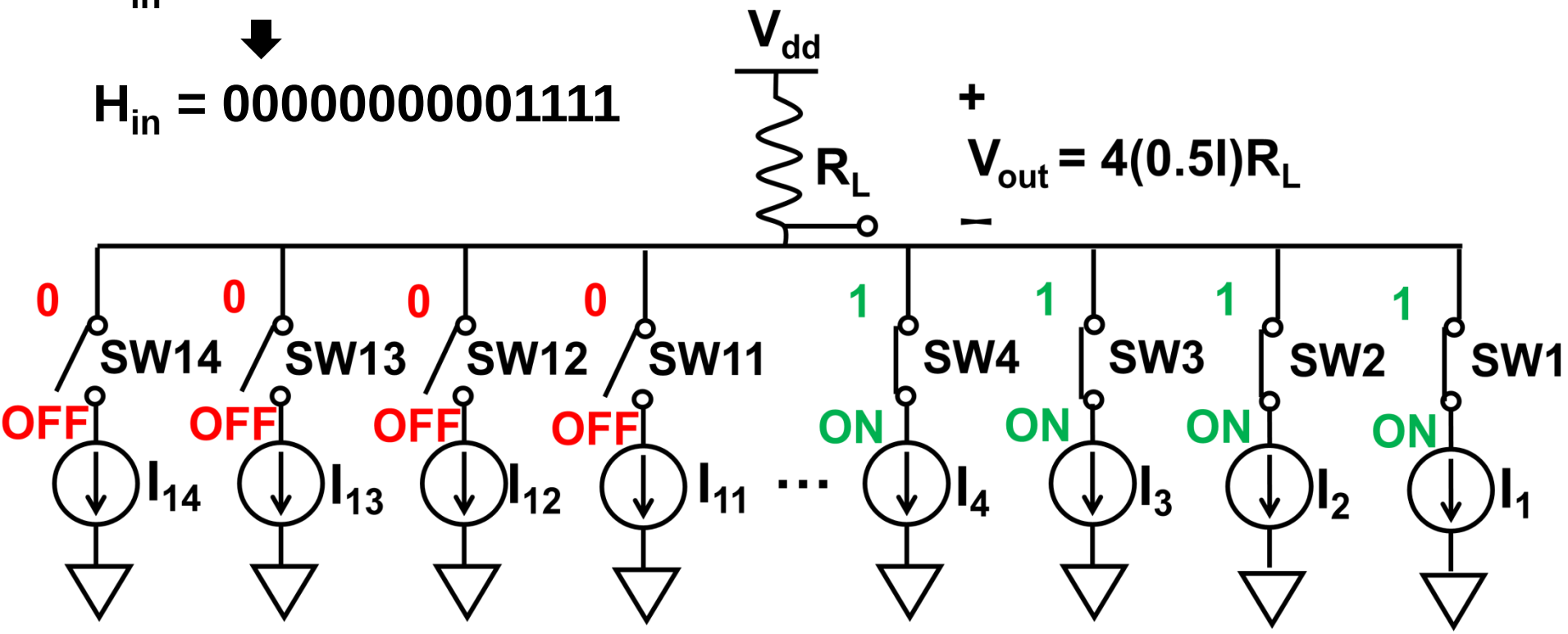

Note : $I_1 = I_2 = \ldots = I_{13} = I_{14} = 0.5I$

# How half-unary works?

**Clock 2:**

$B_{in}$ = 010

$H_{in}$ = 00000000001111



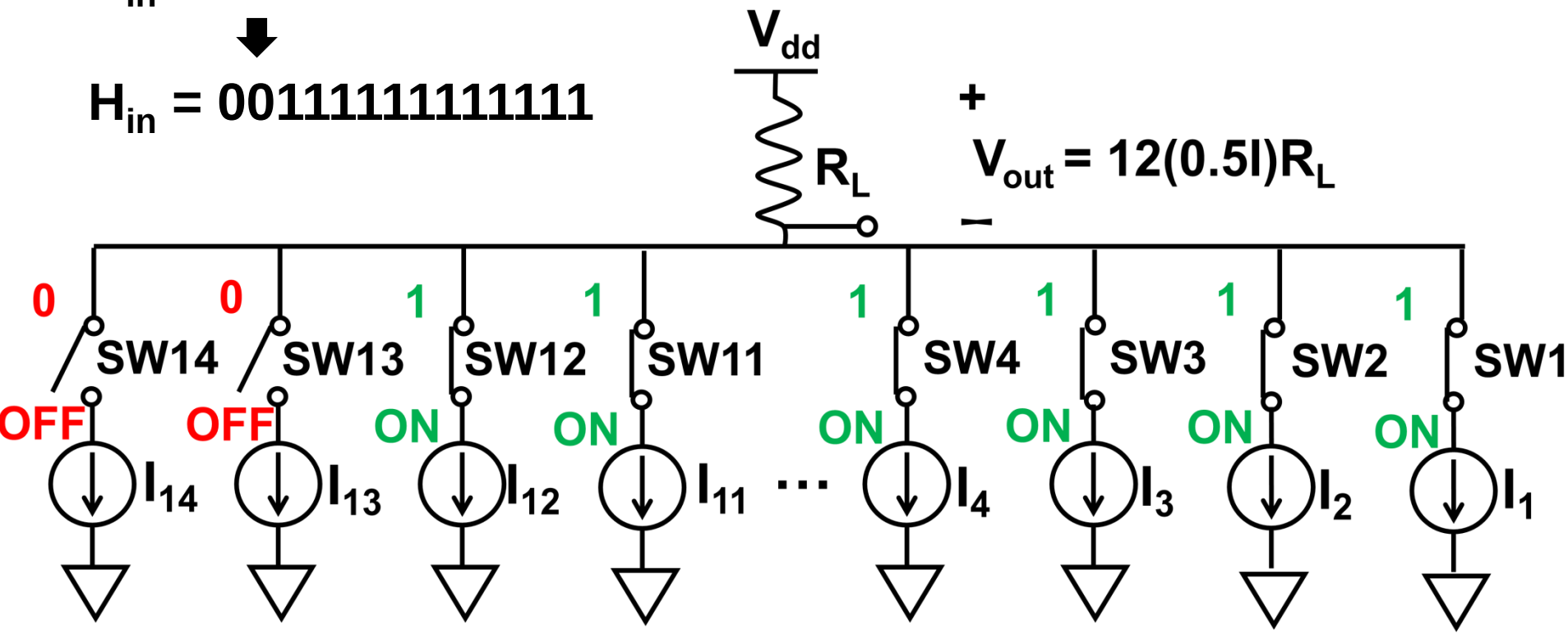

Note : $I_1 = I_2 = \ldots = I_{13} = I_{14} = 0.5I$

# How half-unary works?

**Clock 6:**

$B_{in}$ = 110

$H_{in}$ = 00111111111111




Note : $I_1 = I_2 = \ldots = I_{13} = I_{14} = 0.5I$

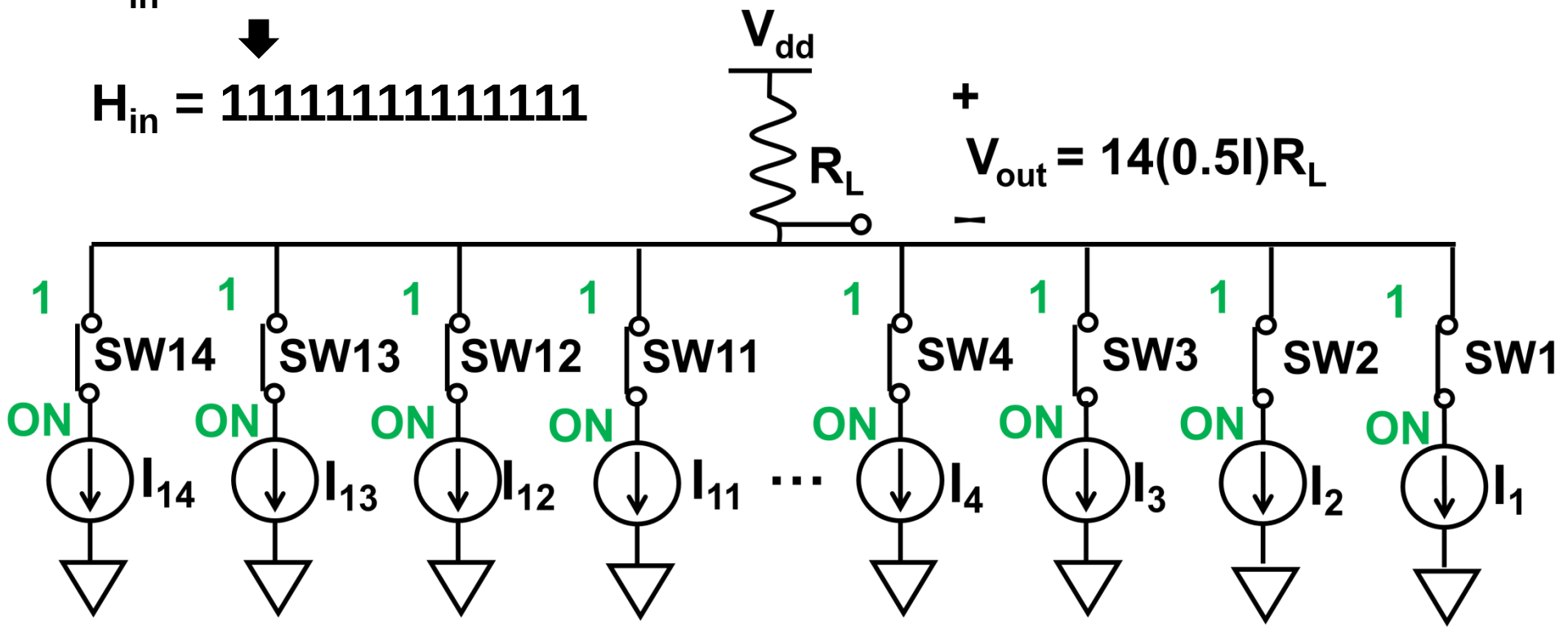
# How half-unary works?

**Clock 7:**

$B_{in}$ = 111

⬇

$H_{in}$ = 11111111111111




Note : $I_1 = I_2 = \ldots = I_{13} = I_{14} = 0.5I$

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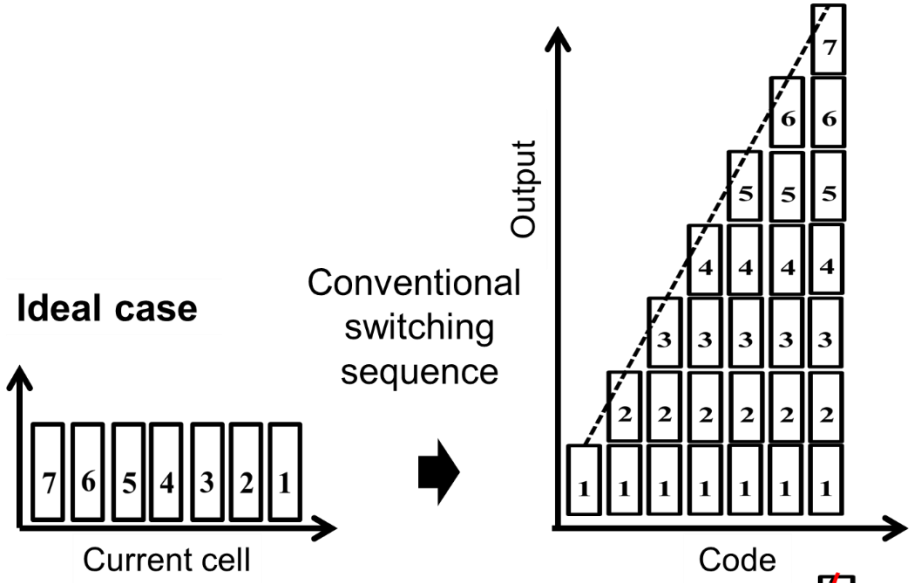
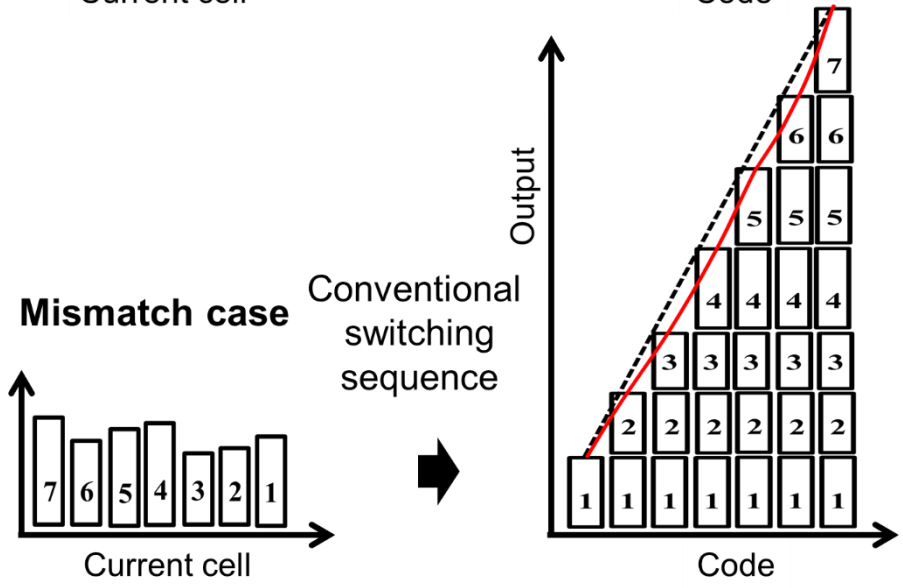
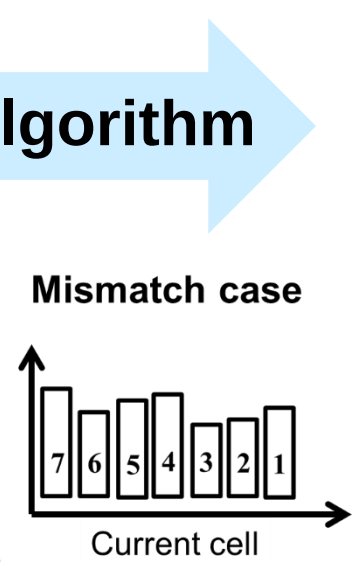
# Switching Sequence



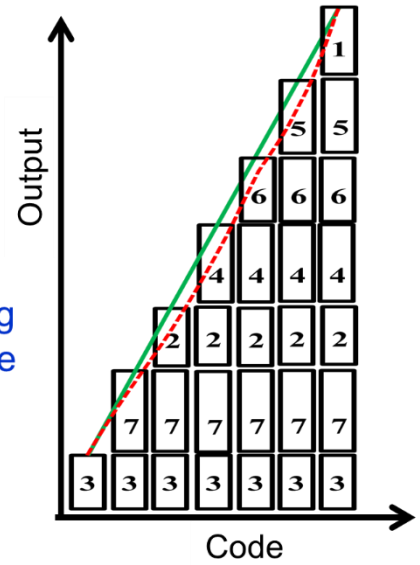

- **New switching sequence**
- **INL improvement**




**Algorithm**

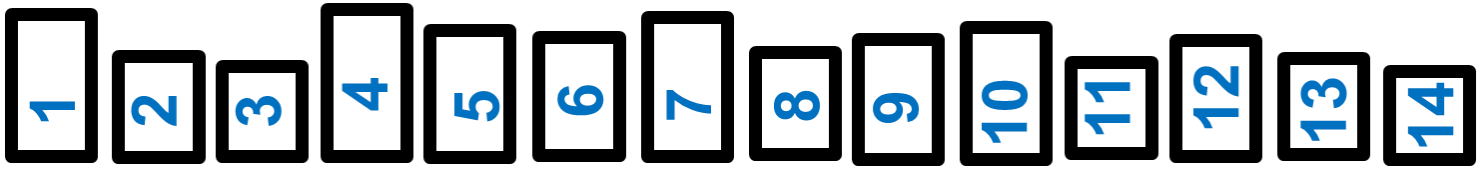



New Switching sequence

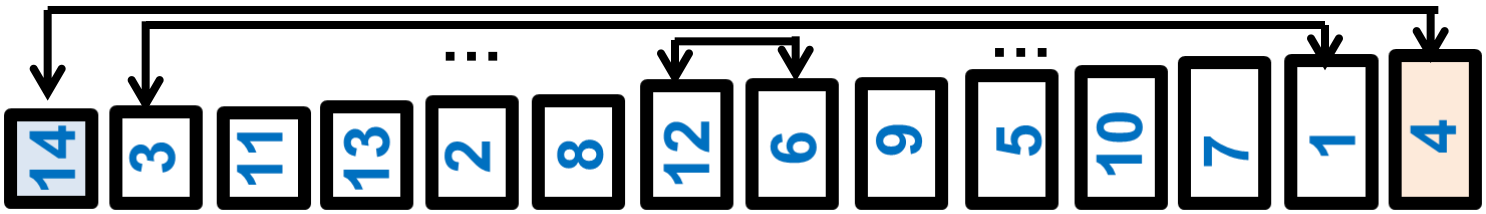


# 3-Stages Current Sorting (3S-CS)

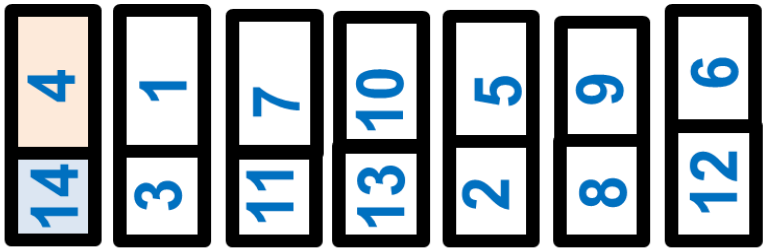
- Original




- 1st Stage Sorting

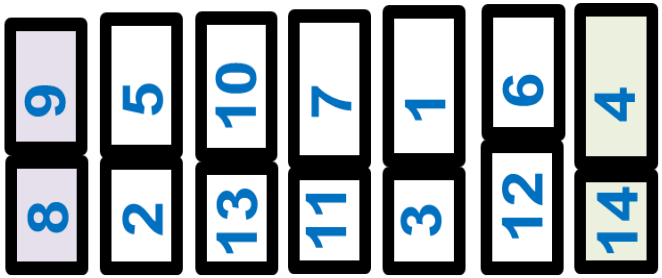



- 1st Stage Pairing → Virtual Unary

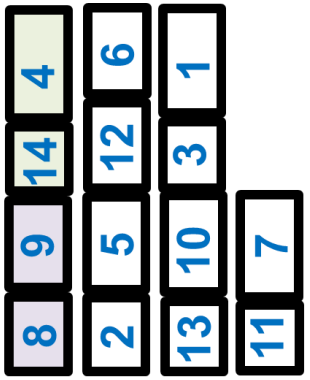


# 3-Stages Current Sorting (3S-CS)

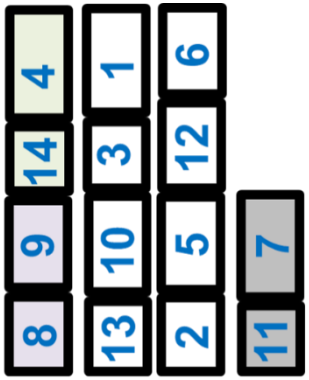
- 2nd Stage Sorting



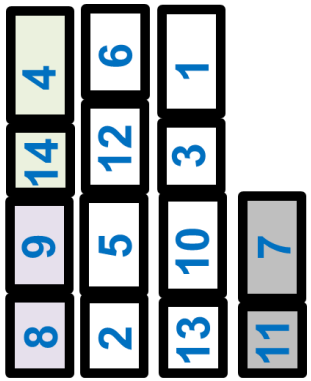

- 2nd Stage Grouping




- 3rd Stage Sorting

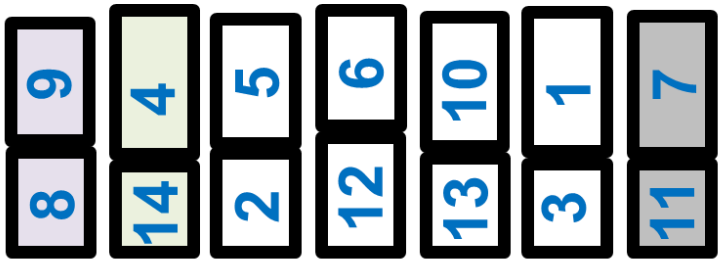



- 3rd Stage Grouping




- Disassociating

➔New switching sequence



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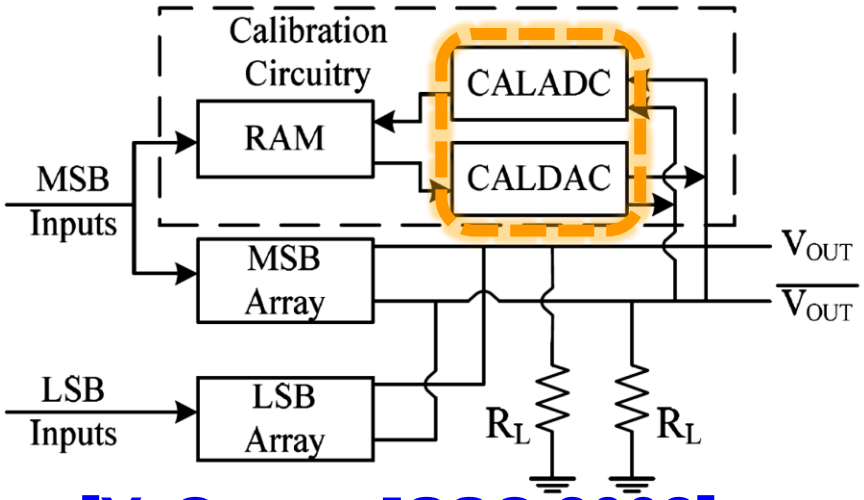
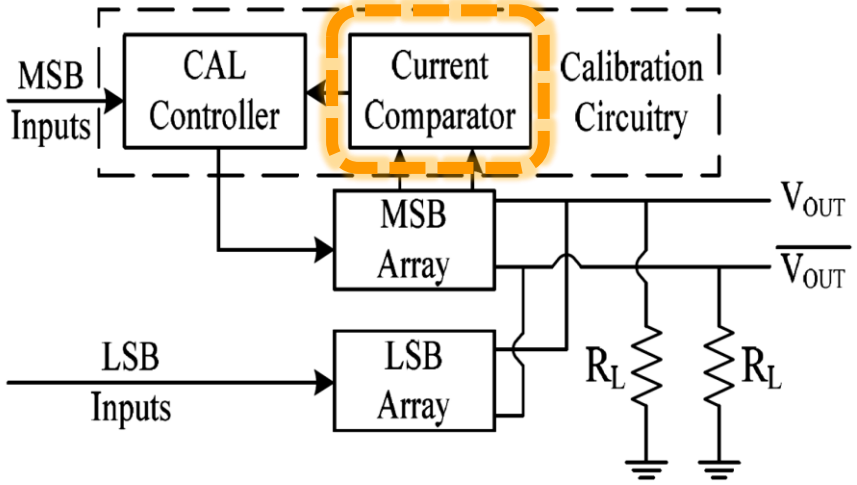
# Previous Calibration Circuits

**Extra calibration ADC/DAC**



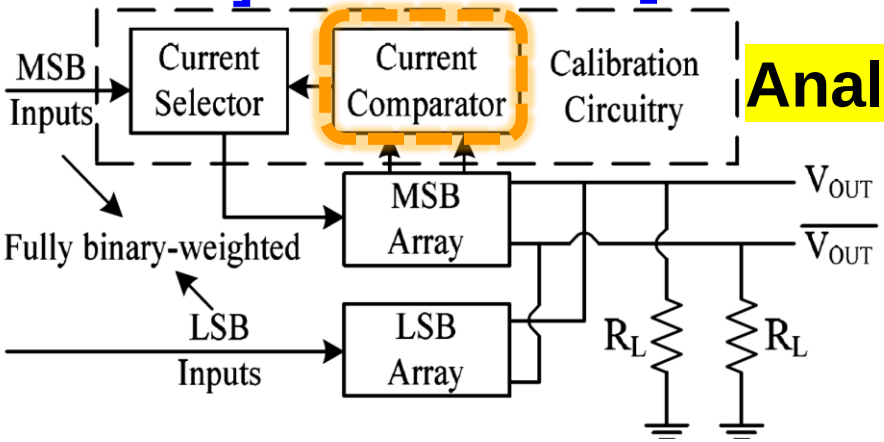

[Y. Cong, JSSC 2003]

**Analog centric**




[T. Chen, JSSC 2007]

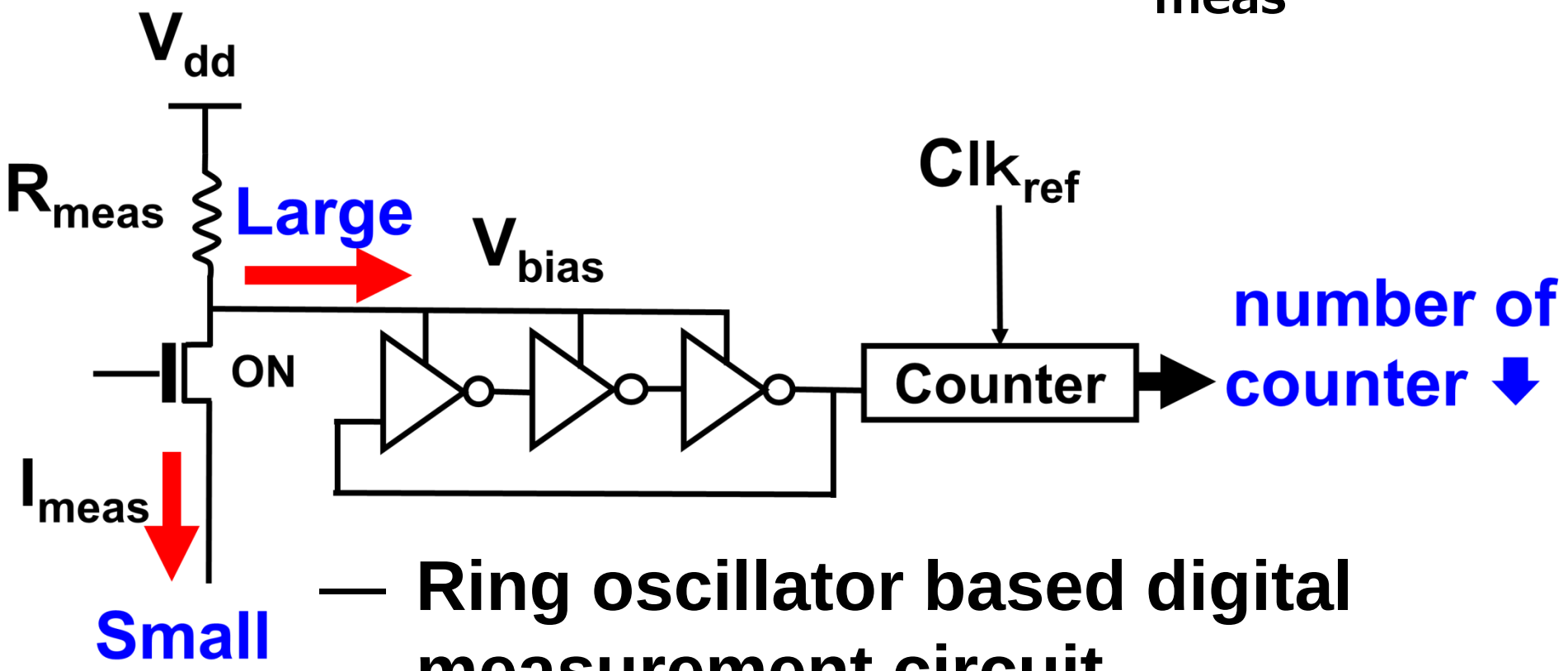
**Analog centric**




[T. Zeng, ISCAS 2010]

# Current Measurement Circuit

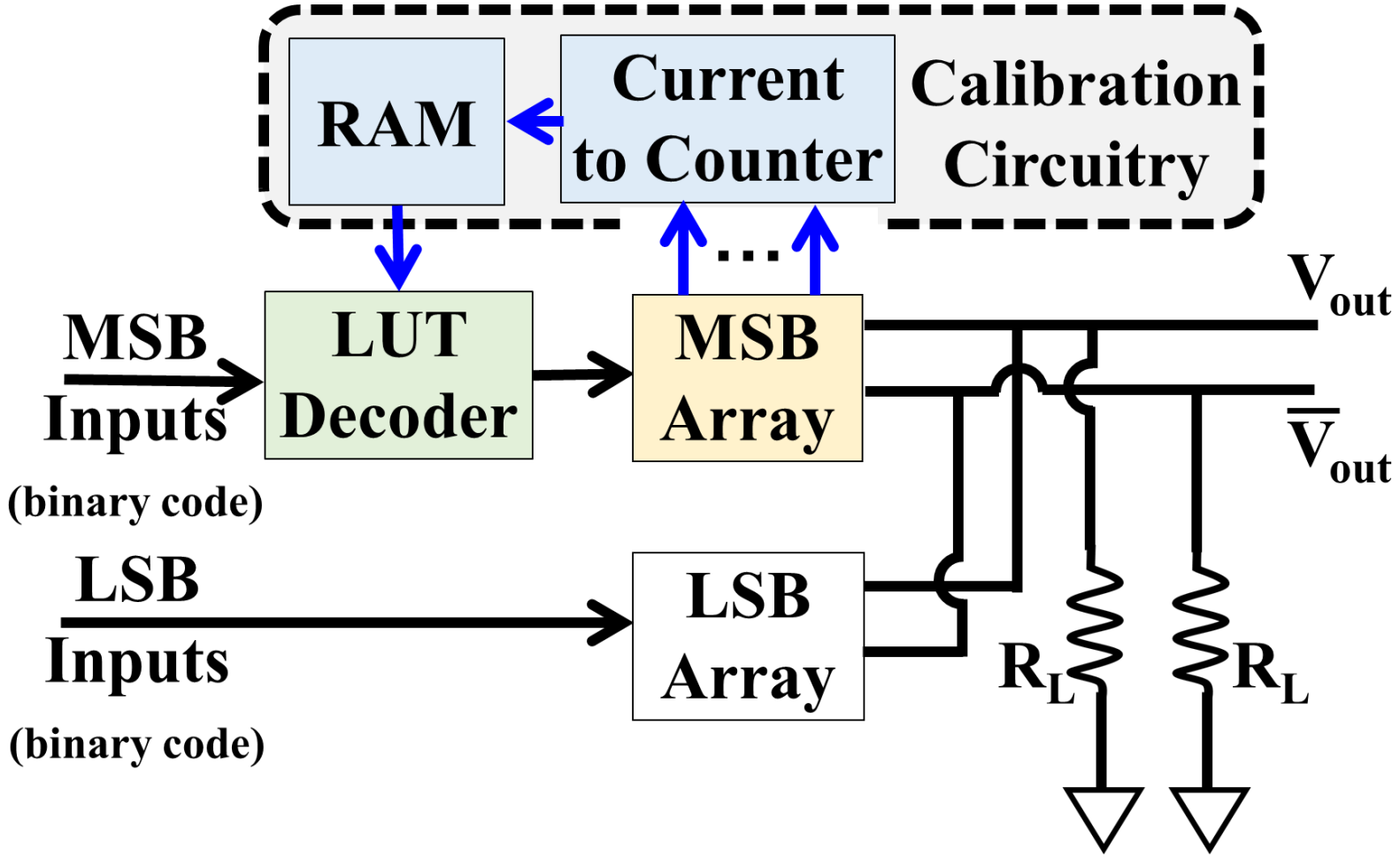
Number of counter ∝ $I_{meas}$




— Ring oscillator based digital measurement circuit

— Digital implementation ☺

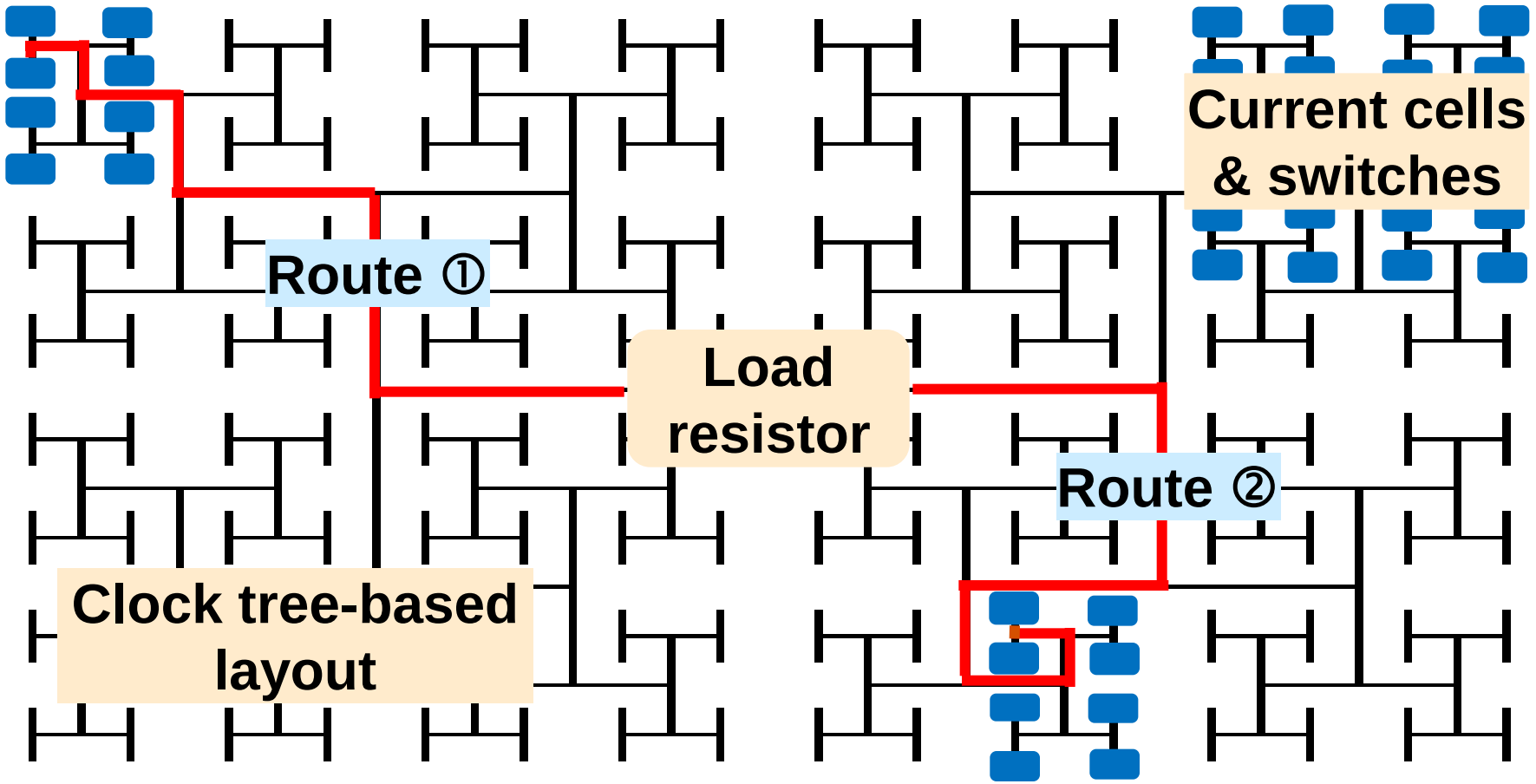
# Proposed Calibration Technique




— No additional analog circuit (switches or routing).

— Only add digital circuit for switch control

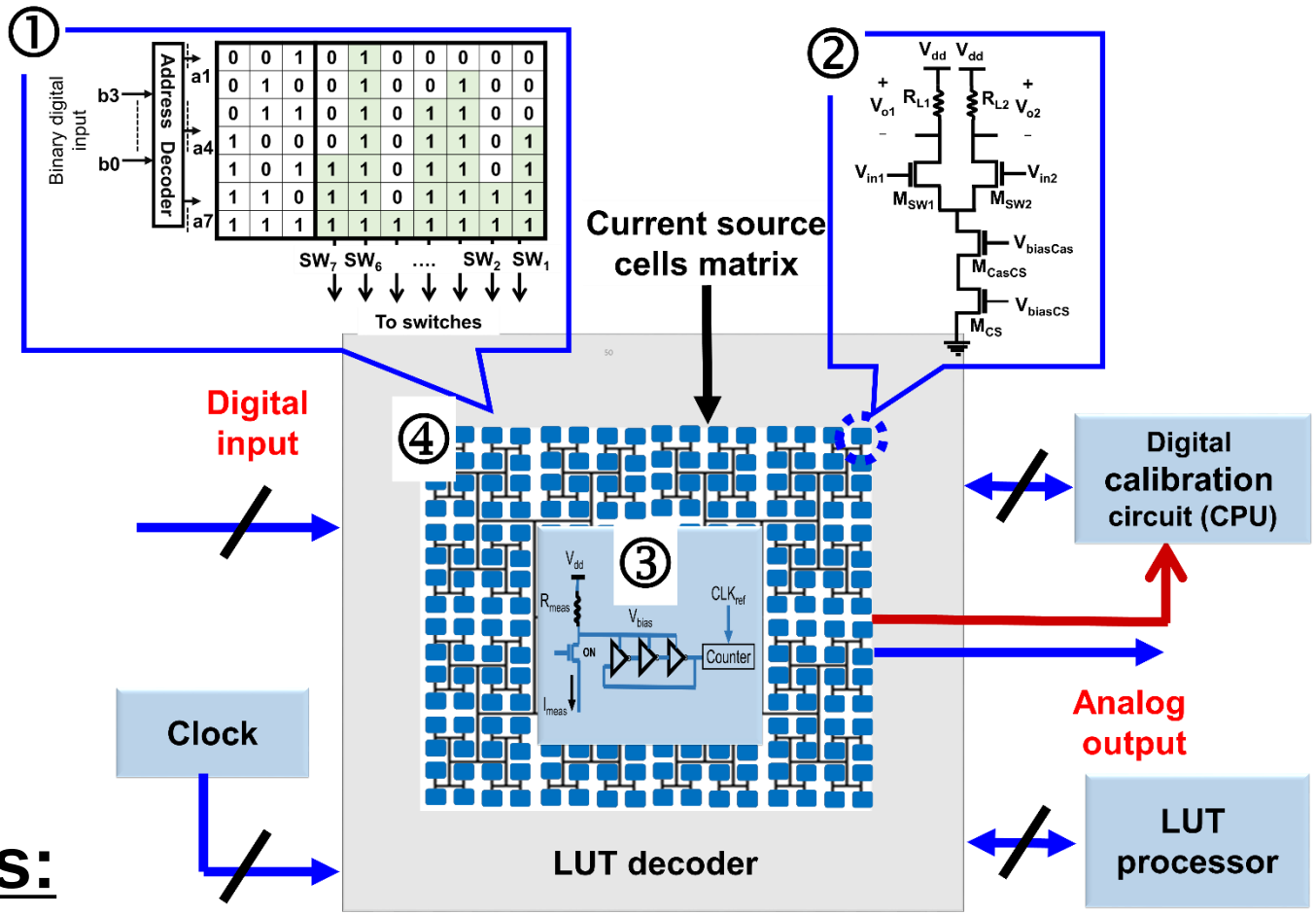
# Layout of Current Cells




— Isometric of interconnection to load resistor

➔Minimum timing skew ☺!!!

# Floor Plan of Whole DAC




## Features:

①3S-CS switching scheme

②Cascoded current source

③Digital measurement circuit

④Isometric wiring

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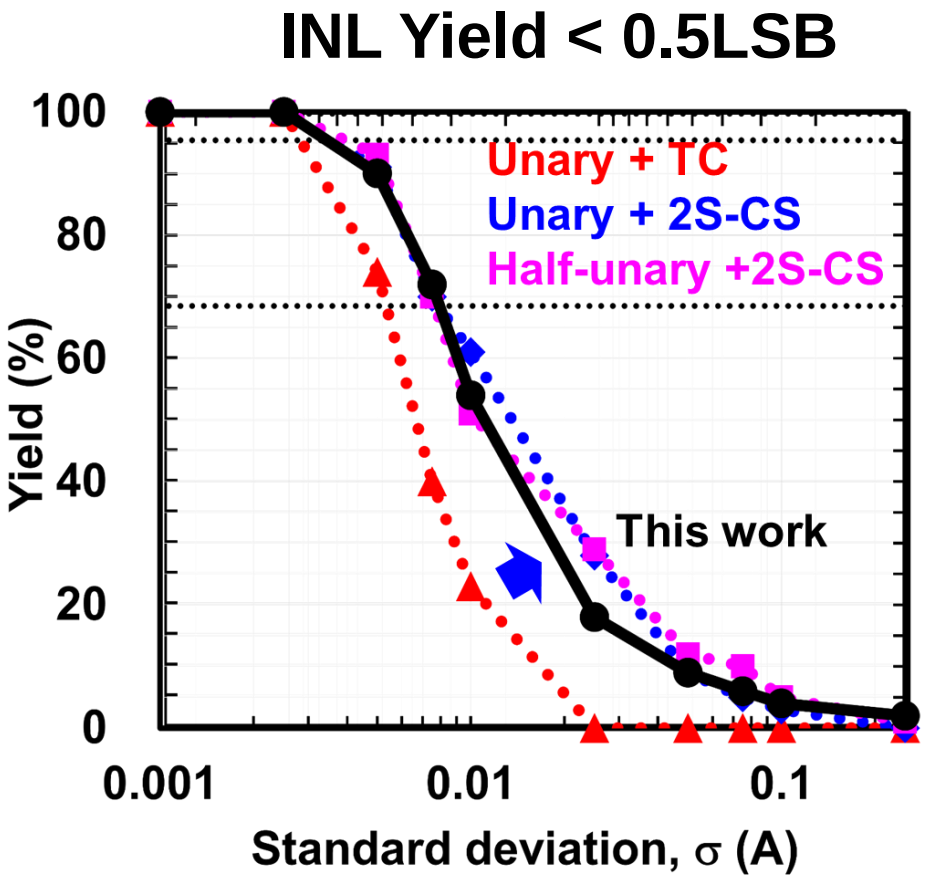
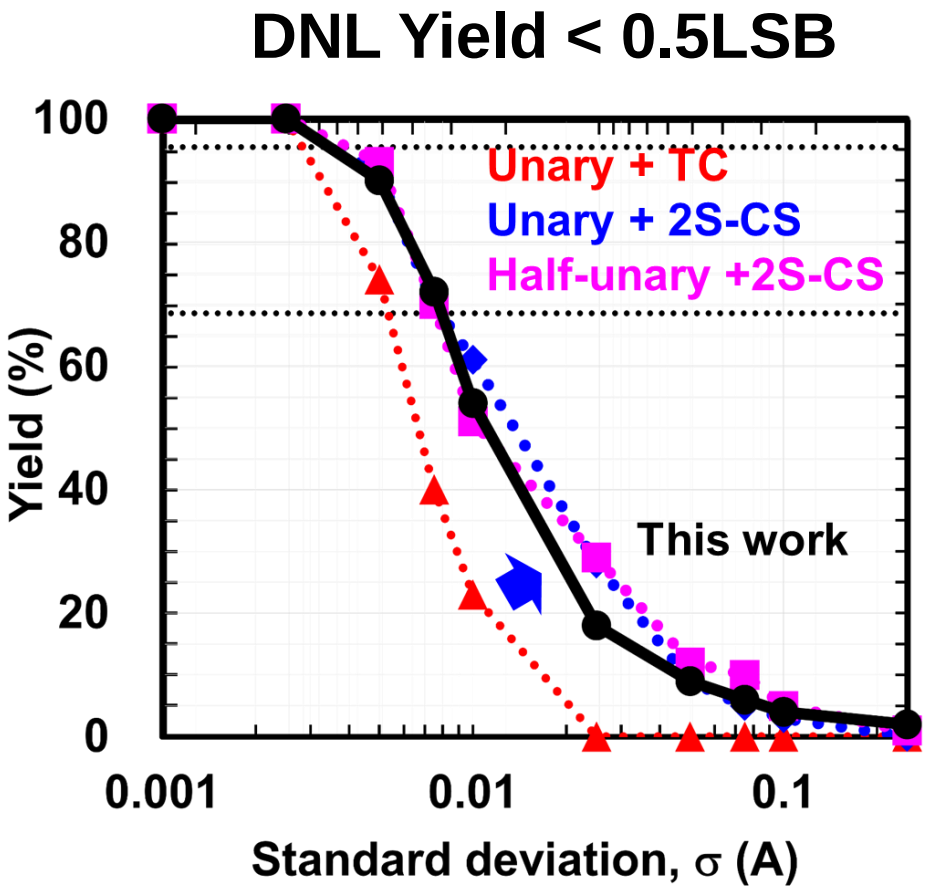
# Simulation condition

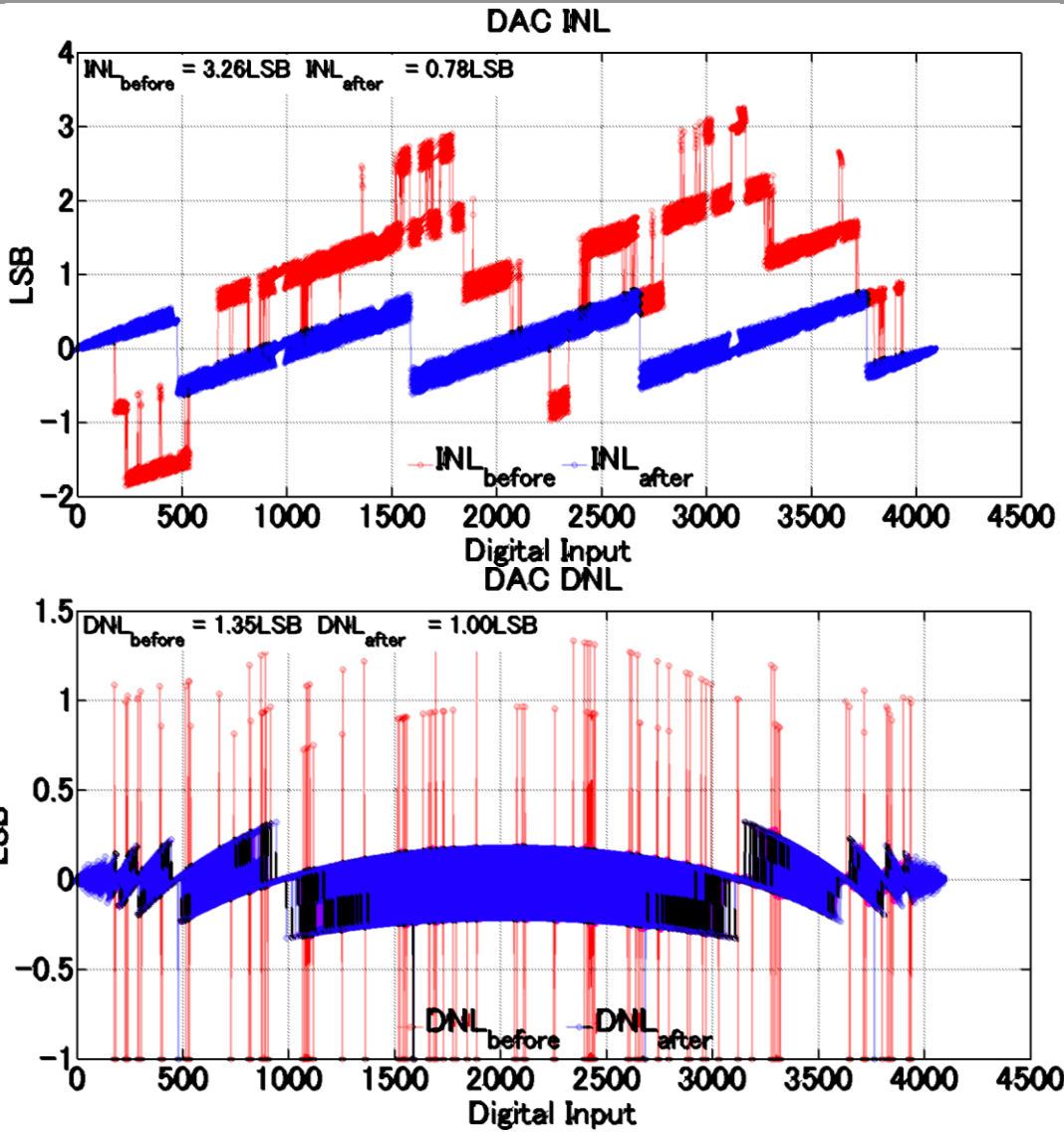
| | |
|---|---|
| **Resolution** | **12-bit** |
| **Input frequency** | **12.8 MHz** |
| **Sampling frequency** | **819.2 MS/s** |
| **Simulation iteration** | **100 times** |
| **Distribution type** | **Gaussian normal distribution, $N(0,\sigma)$,($\sigma$ = 0.001 ~ 0.25 A)** |
| **Switching scheme** | **1. Thermometer code (Unary)**<br>**2. 2-Stages CS(Unary)**<br>**3. 2-Stages CS (H-Unary)**<br>**4. 3-Stages CS (H-Unary) This work** |

# INL & DNL Yields



# Example: INL & DNL (σ = 0.05)




**INL:**

**3.26 LSB**

⬇

**0.78 LSB**

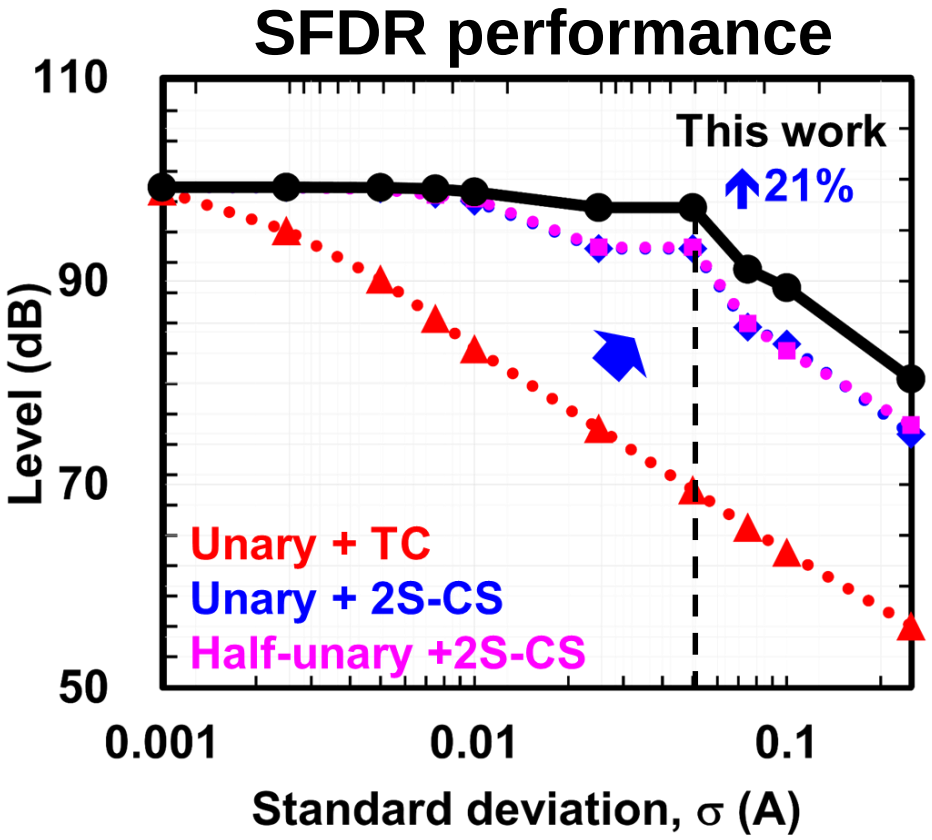
**DNL:**

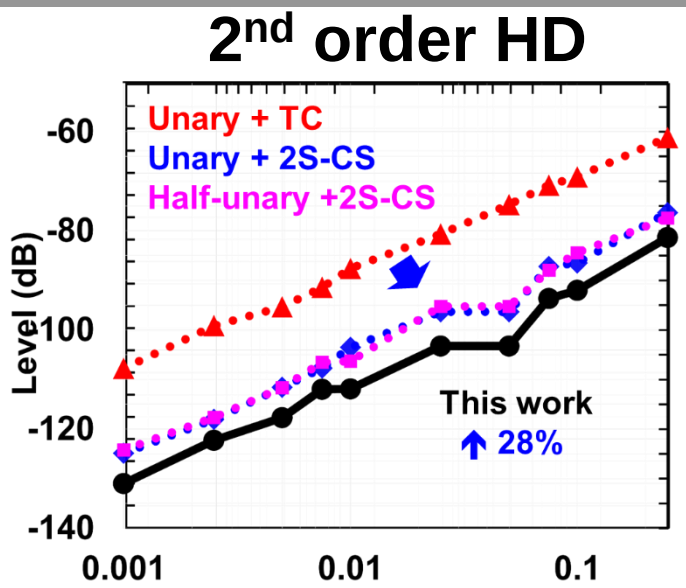
**1.35 LSB**

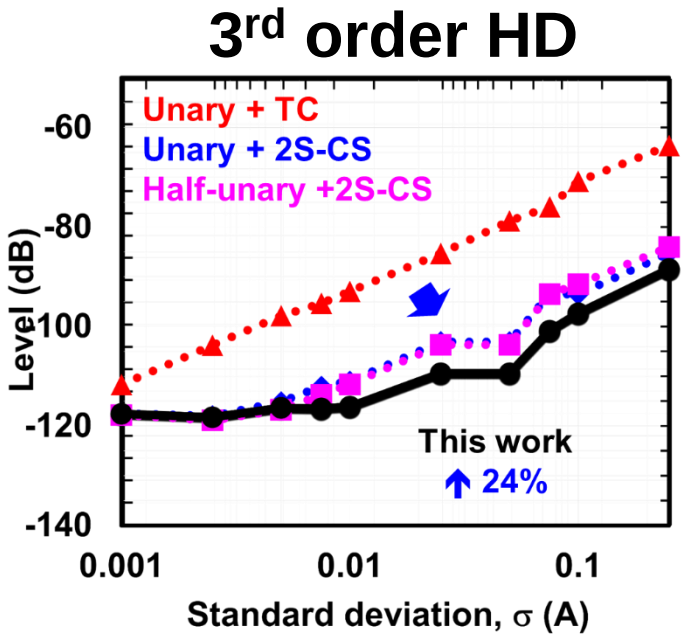
⬇

**1.00 LSB**

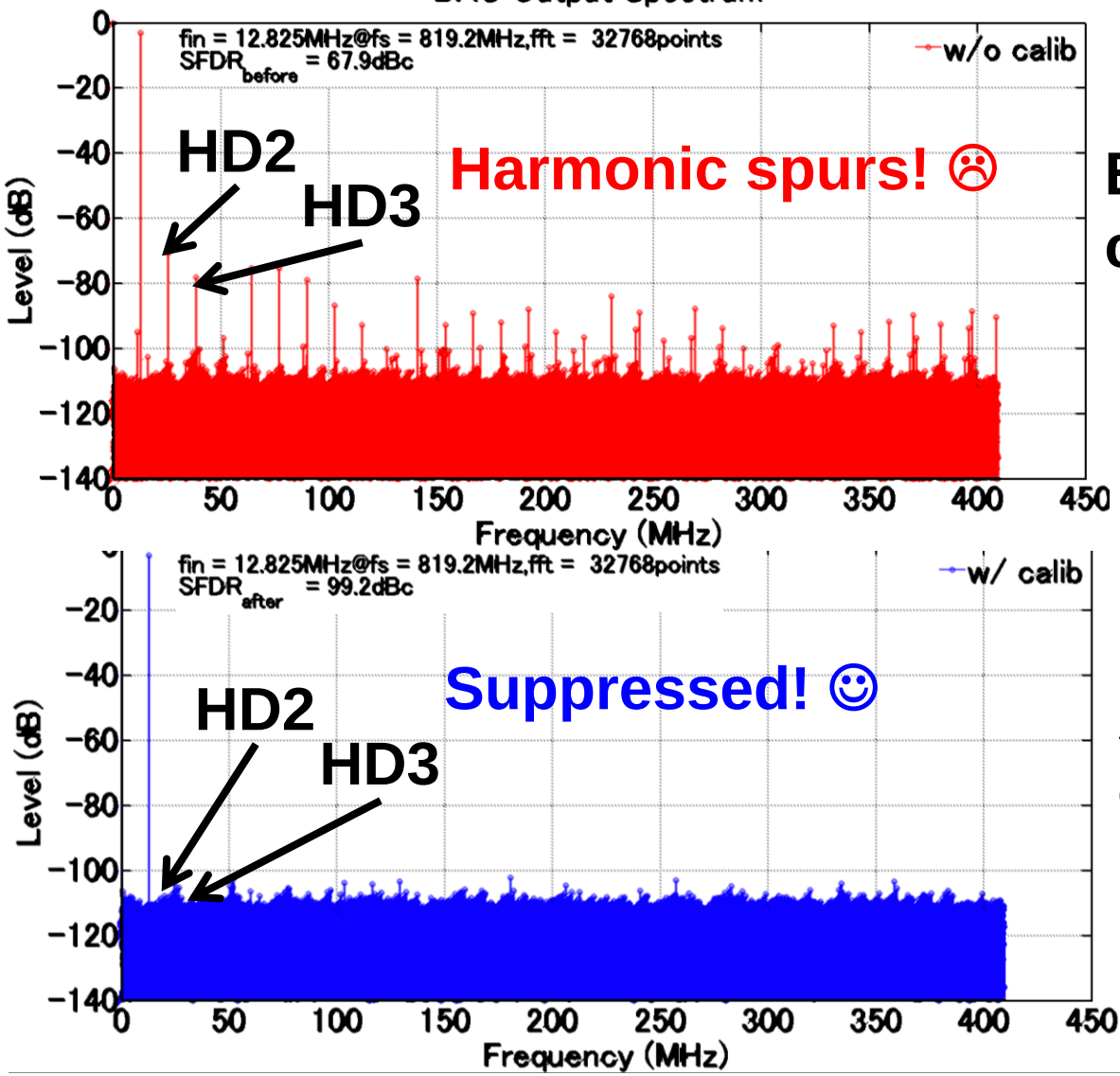
# SFDR & Harmonic Distortions



# SFDR Performance (σ = 0.05)




Before calibration

**SFDR:**

67.9 dB

⬇

99.2 dB

After calibration

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# Conclusion

- **High SFDR CS DAC for fine CMOS**
- **Static linearity improvement**

  **① Half-unary DAC architecture**

  **② 3-stage current sorting algorithm (calibration)**

  **➔ Performed MATLAB simulation with different switching schemes**

  **— Better INL & DNL yields ☺**

  **— Better SFDR, $2^{nd}$ & $3^{rd}$ HDs level ☺**
- **Dynamic linearity improvement**

  **① Well-balanced layout of current cells for interconnection R, C skew minimization.**

**Thank you very much**
**for your kindly attention**

**We acknowledge STARC for kind support.**

# Question

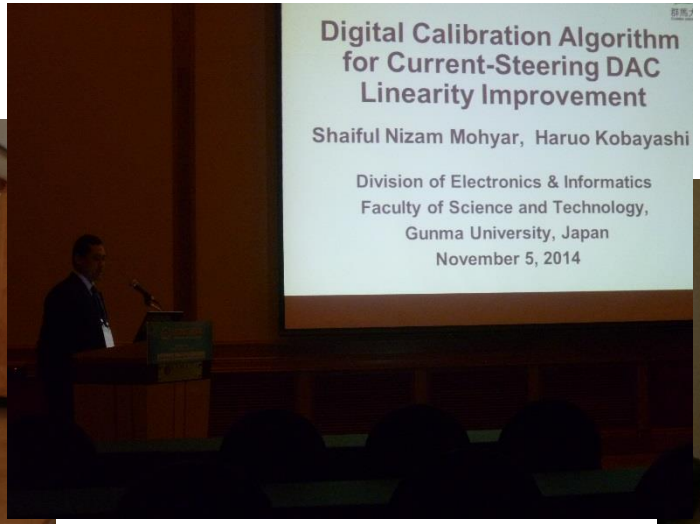
**Q1: How many cycles did you require in order to sort your proposed algorithm?**

**Q2: Let say the optimal number of cycles is six cycles, where one cycle is equal to 20ns, how can you claim the conversion rate of your DAC is 819.2 MS/s?**

**Q3: What is the range of your input voltage?**

# ISOCC2014


ISOCC
ISOCC 2014
International SoC Design Conference
November 3-6, 2014
RAMADA PLAZA JEJU Hotel,
Jeju Korea
2F


Digital Calibration Algorithm for Current-Steering DAC Linearity Improvement
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• Objective
– High SFDR current-steering DAC for communication
• Proposed method
– Current source mismatch effect reduction
1. Half-unary DAC architecture
2. Current source sorting algorithm
→ Static linearity improvement
– Layout strategy
1. Clock-tree-like layout
of current sources & switches
→ Dynamic linearity improvement


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