電流源３段階並び替えによる電流型 DA 変換器の線形性向上

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3-Stage Current Source Sorting Algorithm for Current-Steering DAC Linearity Improvement

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This paper introduces an algorithm called 3-stage current source sorting (3S-CS) in half-unary weighted current cells to improve the linearity of a current-steering digital-to-analog converter (DAC). We show that based on our statistical analysis and simulation results, the proposed algorithm improves the DAC static linearity as well as its dynamic performance.

Keywords: current-steering DAC, current source mismatch, linearity, current-sorting, half-unary structure

1. Introduction

Recently, the emerging market of telecommunication devices such mobile phones, wireless modems and avionics raises the demands for high-speed, high accuracy digital-to-analog converters (DACs). Especially, in the field of wireless communication, the accuracy of the DAC is very important to ensure no noise leakage during transmission. As society needs faster, cheaper, and more reliable communication, this block design becomes more complicated, although the digital electronics actually have benefits from the advancements of CMOS technology. But again, there are still requirements in solving the fundamental physical constraints, such as noise, component matching and fabrication process parasitic. Therefore, the DAC linearity must be sufficient enough to accommodate with such requirements. For the DAC with resolution less than 10 bits, this problem may not be so significant but the one with equal to or more than 10 bits, the current source mismatch and timing error effects become serious [(1)].

In this paper we propose a half-unary current steering DAC to aim the improvement of the DAC linearity both integral nonlinearity (INL) and differential nonlinearity (DNL). Therefore, not only the static performance but the dynamic performance as well is important [(2)].

Here we are only focusing on suppressing the current source mismatch effect rather than timing error; we consider here a segmented DAC architecture which has relatively small glitch. We propose here called a 3-stage current sorting algorithm to reduce the current source mismatch effects to DAC nonlinearity. This technique is divided into three stages.

(1) The first stage is to find out the optimized combination of two half-unary weighted current sources, and then form as a unary weighted current source. At this stage, the error between these two current cells is cancelled by each other.

(2) In the second stages, each formed current source pair will be rearranged to optimize the switching selection. Thus, without any special layout and switching scheme technique, we can automatically reduce the current source mismatch effect and its switching sequence selection once.

By adopting this technique in the segmented part, the current source mismatch effects are expected to be suppressed. Hence, a sufficient spurious free dynamic range (SFDR) can be obtained. By performing this algorithm as a foreground calibration that totally operates in digital domain, this technique is matched with the VLSI technology advancement trend. Our MATLAB simulation results show that our proposed algorithm achieves better SFDR results compared to a conventional unary weighted DAC with thermometer-coded switching scheme in case that the static current source mismatches are considered.

This paper consists of six sections. Section 2

describes present current-steering DAC architectures; binary-weighted, unary-weighted, segmented and our proposed half-unary weighted. Section 3 explains DAC nonlinearity due to current source mismatches. Section 4 discusses proposed techniques that are used to reduce the targeted errors. Section 5 discusses simulation results, and conclusion is provided in Section 6.

2. DAC architecture

2·1 Current-steering DAC

Current steering DAC is one of the common DAC architectures. This architecture is selected due to its suitability in producing such high speed, more linear, easy to integrate with digital circuit, and low cost (small chip area), though it is a little bit power hungry.

The simple structure of this architecture is a binary weighted structure, where its current source values use binary weights (I_1 = I, I_2 = 2I, I_3 = 4I) (Fig. 1). Its operation depends on the digital input which controls the switches between V_{out} and current source cells. For example, when the digital input is 4, then SW_3 turn on, and SW_1, SW_2 turn off and the output voltage V_{out} is obtained. The relationship between input-to-output of this architecture can be explained as in (1).

$$V_{out} = V_{dd} - I_o R_L \quad \text{.....(1)}$$

Here R_L is a load resistor. The binary weighted current-steering DAC has advantages of high speed sampling operation, and small chip area. However, due to its non-identical current weights, it produces the large glitch energy especially at the mid-code transition and the input-output monotonicity characteristics are not guaranteed.

Therefore, a unary weighted current steering DAC has been introduced to overcome the disadvantages of the binary-weighted structure (Fig. 2). Compared to binary weighted structure, a unary weighted structure requires 2^N -1 unit current sources for N -bit resolution where all current source weight is identical expressed in (2).

$$I_1 = I_2 = \cdots = I_6 = I_7 = I \quad \text{.....(2)}$$

For the operational of the unary weighted structure, a binary-to-thermometer code decoder is required. For example, with same resolution as binary weighted, a unary weighted structure requires 7 separated codes to control the switches.

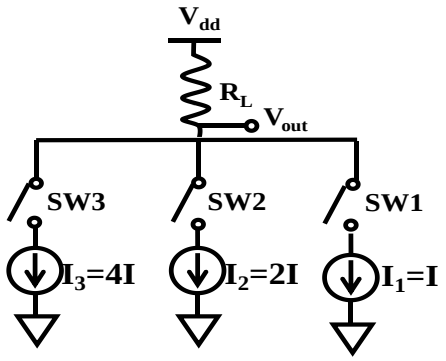

Fig. 1 A binary weighted current-steering DAC.

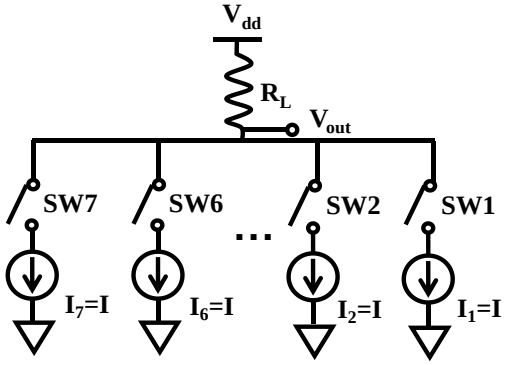

Fig. 2 A unary weighted current-steering DAC.

In case of digital input of 4, SW_1, SW_2, SW_3, and SW_4 will turn on, and SW_5, SW_6, and SW_7 are remained off. So, the output voltage V_{out} that satisfies q. (1) can be obtained. Due to its identical current weight, a smaller glitch energy compared to binary weighted structure is expected while the input-output monotonicity characteristics can be also achieved. In additional, its high intrinsic redundancy has promising more flexibility for output optimization. Nonetheless, this architecture suffers from more logic and decoder circuit requirement which increases the silicon chip area for each bit increment (2^N - (N+1)).

In many cases, their combination (binary and unary weighted structures) is used; for higher bits, the unary-weighted structure is used while for lower bits the binary weighted structure is used. This combined topology can achieve well-balance of chip area [3,4], power, speed and glitch energy [5] .

Another approach for these kinds of error correction is calibration technique. Most popular candidates are self-calibration and switching arrangement scheme [6,7]. However, most calibrations based on the unary weighted structure only improve the INL while the DNL remains

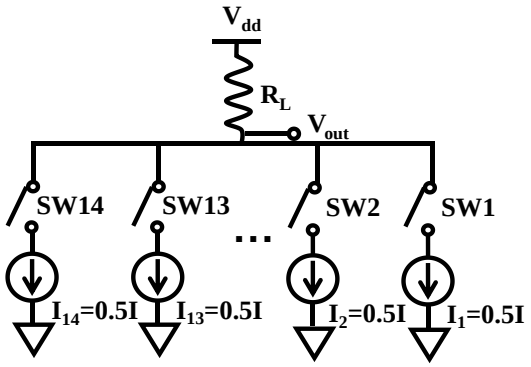

Fig. 3 Proposed half-unary current-steering DAC.

unchanged.

Therefore, in order to achieve both integral and differential linearity improvement, we propose another structure called a half-unary weighted of number of current source cells with halved weight compared to the conventional unary (Fig. 3). This structure offers a better glitch energy compared to binary and unary structure. However, since its number of current sources is double, the consumed silicon chip area and complexity circuit and routing of its decoder are still remained. Therefore, by manipulating its advantages and taking care of its weakness, we focus on the segmented part for the higher bits with half-unary structure.

3. DAC nonlinearity

3·1 Current source mismatch

In practical CMOS technologies, the current source mismatch influenced by the threshold matching, ΔV_{th} or by the slope mismatch, $\frac{\Delta\beta}{\beta}$ (Fig.4). With the MOS devices in saturation, then its drain current, I_{d} is given by:

$$I_{d,1} = \frac{\beta}{2}(V_{gs} - V_{th1})^2 \quad \text{.....(3)}$$

Here β is the gain of the MOS device.

$$\beta = \mu C_{ox}\frac{W}{L} \quad \text{.....(4)}$$

However, due to the small difference between the ideal value, the current mismatches can be calculated by:

$$\frac{\Delta I_{d,1}}{I_{d,1}} = \frac{\Delta\beta}{\beta} + \frac{2\Delta V_{th1}}{V_{gs}-V_{th1}} \quad \text{.....(5)}$$

Generally, in case of small current densities, the current mismatches can be simplified as:

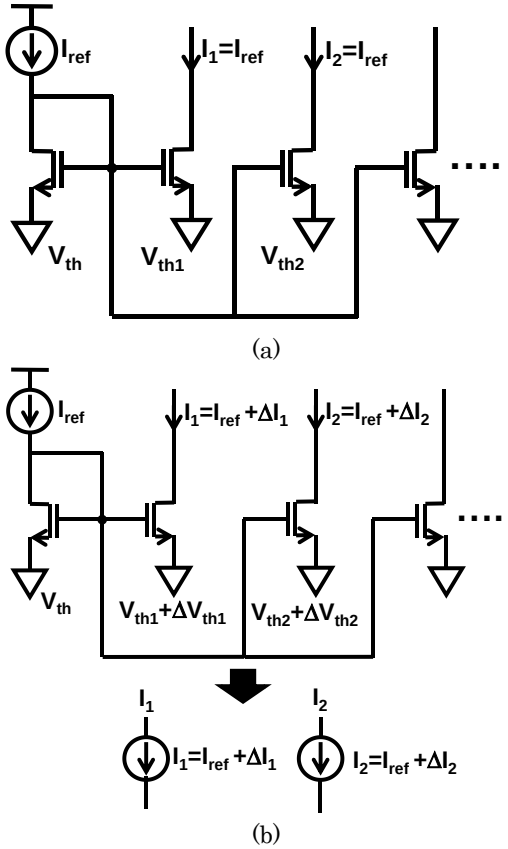

Fig. 4 Current mirror circuit.
(a) Ideal case. (b) Mismatch case.

$$\frac{\Delta I_{d,1}}{I_{d,1}} = \frac{2}{V_{gs1}-V_{th1}}\frac{A_{V_{th}t_{ox}}}{\sqrt{WL}} \quad \text{.....(6)}$$

In case of large current densities, the current mismatches are determined by:

$$\frac{\Delta I_{d,1}}{I_{d,1}} = \frac{\Delta\beta}{\beta}\frac{1}{\sqrt{WL}} \quad \text{.....(7)}$$

From (6) and (7), we see that the current mismatches are dependent on device size.

In CMOS process, the current mismatches can be reduced with thinner gate oxide thickness, where the supply voltage has to be decreased. This reduction will affect the signal-to-noise ratio which requires more bias current. As result, the power may be increased. Another trade-off is between threshold voltage mismatch and device size. By increasing the gate size, the offset is reduced but the device area is increased. Moreover, the capacitance of the devices will also increase. Then, again more biasing current is required. Here, we are considering to reduce the current mismatches due to device size ($\sqrt{WL}$) at post-fabrication process rather than using matching method during pre-fabrication.

4. Proposed digital calibration algorithm

In this section, we manipulate a half-unary structure and a proposed digital algorithm as one calibration technique in a segmented current-steering DAC. With a half-unary weighted structure at higher bits and binary weighted in lower bits, we aim that the new digital algorithm can improve the linearity of the DAC from the effect of the current source mismatches, at the same time, the optimized switching sequence optimization can suppress the distortion especially caused by 2nd and 3rd order harmonics of the input signal for better dynamic performance. This section will discuss the essence of the proposed digital algorithm as well as calibration technique.

4・1 3-stage current source sorting

Sort and group procedure has been used in several published works in order to reduce the effect of static errors [7,8]. Basically, this procedure intends to optimize the switching selection [7]. This kind of procedure also has been used to form a unary current cell to a group of unary current cells with different weights [8]. Applying such procedure ensures the mismatch error can be eliminated or be averaged during conversion. In our work, we have merged these two procedures into one called as a 3-stage current sorting technique (3S-CS). This technique is divided into two main stages; combination and rearrangement (Fig. 5).

An example of 3-bit of half-unary weighted current cells has been used in order to describe this algorithm. The proposed algorithm is explained as the following steps:

1st stage (combination)

① By assuming the initial condition of current source after fabrication.

② Then, the 14 available current source cells (twice number of conventional unary weighted structures) will be sorted by their current values.

③ Then, by associating the smallest and the largest values (in this case, I_3 and I_7) to form virtual a unary weighted cell during conversion. Then, following by the second smaller, I_{14} is combined with the second larger value, I_{10}. Next, the third smaller, I_{11} and the third larger, I_4 and so on until all half-unary weighted cells have their own pairs

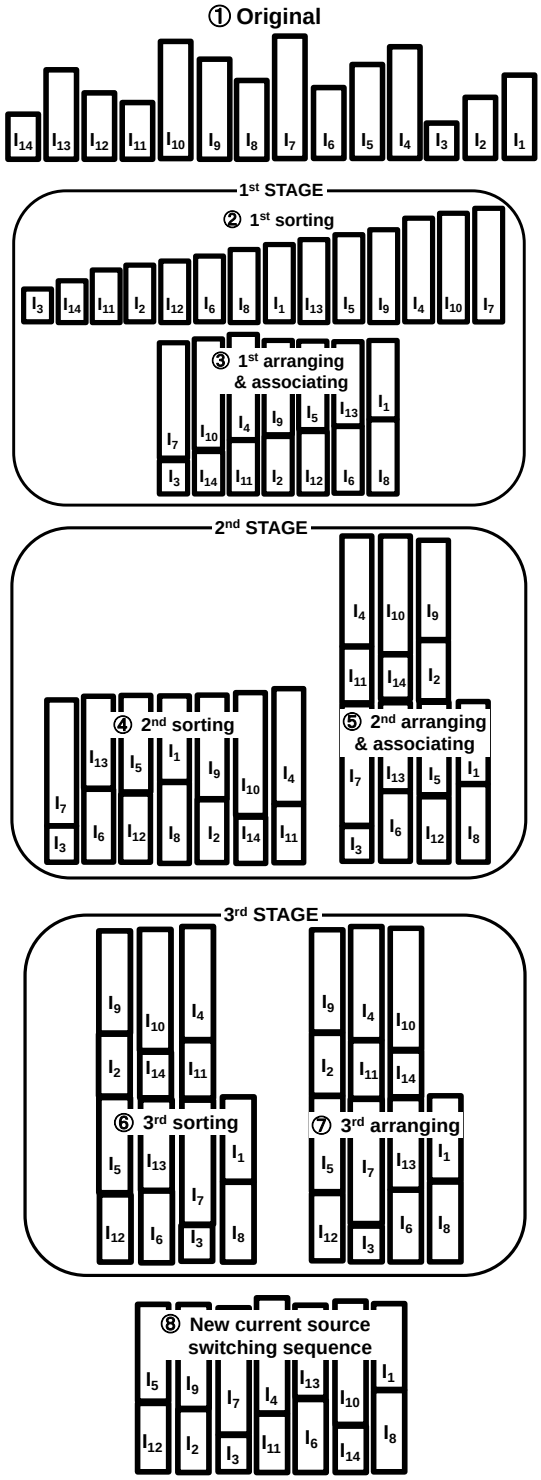

Fig. 5 Proposed current sorting algorithm.

2nd stage and 3rd stage (rearrangement)

④ After all single cells have their own pair as formed as a virtual unary (in this case, 7 pair of unary cells), again all pair will sort by its associated values.

⑤ Then, by repeating step③, in case of 3-bit, 3 pairs from 4 single cells and a single pair with 2 single cells are obtained

⑥ For further cell selection optimizations, 3 pairs with 4 single cells are sorted while the pair with 2 single cells remains as in step⑤.

⑦ Different with step③, the sorted 3 pair positions will be rearranged without need to be associated.

⑧ Finally, the optimized switching selection can be obtained by disassociating the pair in ⑦ down to a pair of two unary cells.

Therefore, during conversion, these two cells will turn on or off together.

This kind of procedure is benefited for improving INL and DNL.

4·2 Calibration

Calibration can be divided into 2 categories; with error measurement or without error measurement. Each category has strength and weakness [7,9-11]. By implementing error measurement, the exact error profile can be obtained, for implementation of either foreground or background. However, its effectiveness relies on the accuracy of the measurement circuit. There is also risk of performance deterioration due to the measurement circuit itself. On the other hand, it can be performed without error knowledge by average operation However, it can only operate in background mode. Thus, it is essentially exposing to the performance deterioration, as well as power and noise increment.

In this work, we are considering the calibration with error measurement approach to meet with our proposed techniques (Fig. 6). Through foreground mode of calibration, the overall calibration steps are as follow:

① Input test code will be inserted by central processing unit (CPU) that control the digital calibration circuit.

② By implementing current measurement circuit, each current source cells are measured.

③ All measured values are stored in memory.

④ Then, these data are fed to digital calibration circuit to perform main calibration process.

⑤ Finally, the optimized switching sequence will be stored in memory.

Finally, the optimized switching sequence will be used during conversion.

For a simple measurement mechanism and realization with fully digital circuit, a ring

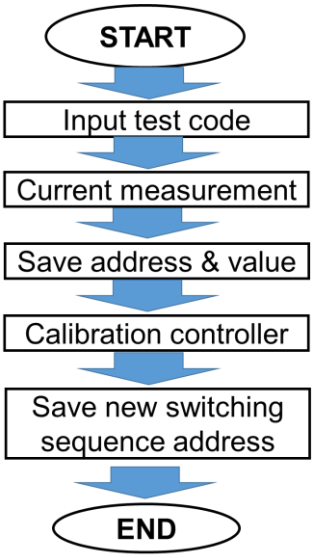

Fig. 6 Calibration procedure.

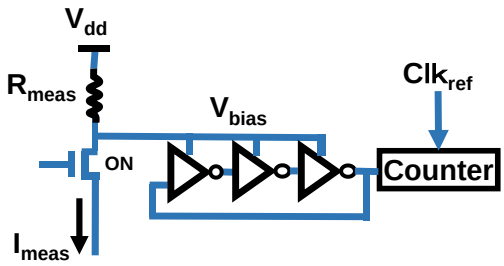

Fig. 7 Measurement circuit.

oscillator-based measurement circuit is adopted during calibration (Fig. 7). However, the accuracy of this measurement circuit becomes a trade-off with the overall area and DAC performance itself. By using this measurement circuit, the amount current is equivalent to the number of clock that has been counted during measurement. The number of counter is inversely proportional to the measured current value. This means that when the high current value is measured, then the number of counter becomes less and vice versa.

For implementation, a look-up table (LUT) based decoder is used to convert the binary digital input code to equivalent thermometer-code (Fig. 8). Conventionally, thermometer-coded (TC) switching scheme are commonly used (Fig. 8 (a)). However, this switching sequence suffers from data-dependent output load which causes more distortion in output signal. Thus, by using the 3S-CS, this effect has been automatically reduced by optimizing the selection of current cell.

Here, we use the LUT decoder to address the location of the optimized switching selection in memory (Fig. 8 (b)). So, the decoder will transform

the binary code into the address that contains the optimization of each corresponding digital input value to be loaded. Hence, the switches will configure as the loaded code. This process continues for all digital input. As a result, a current-steering DAC with LUT decoder and 3S-CS calibration technique is proposed (Fig. 9).

The measurement circuit is purposely located in the center of the current source array to minimize the distance mismatch between measurement circuit and current cells. So, the effect of parasitic resistance and capacitance mismatches during the measurement can be reduced, which improves the measurement accuracy with short time.

4·3 Layout

Conventional current source structure suffers from the crosstalk noise and low output impedance (Fig. 10(a)). In contrast, by adopting cascoded transistor for current source cell structure, more accurate current gain can be obtained (Fig. 10(b)). In additional, better output impedance and the effect of parasitic capacitance reduction between current source and switches also can be achieved. Secondly, due to double the number of current sources, it increases not only the area of logic and decoder circuit, but also the complexity of the layout in term of routing and risk of parasitic

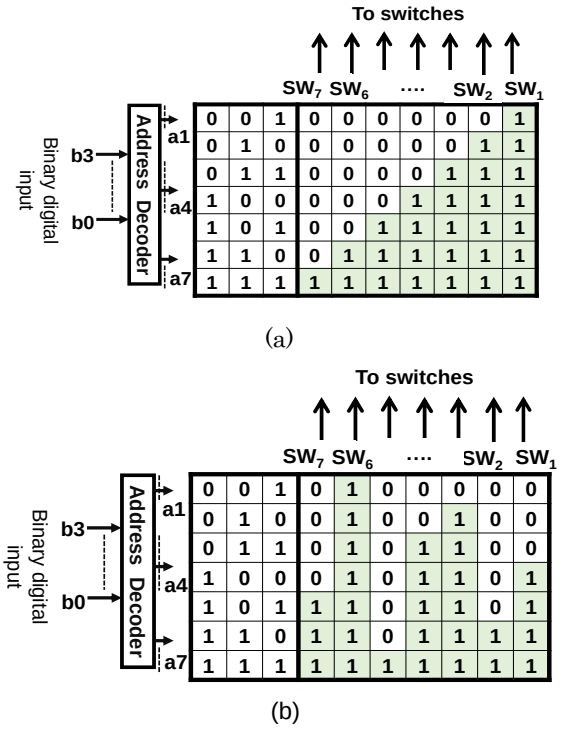

Fig. 8 Look-up table based decoder.
(a) Thermometer-coded. (b) Proposed algorithm.

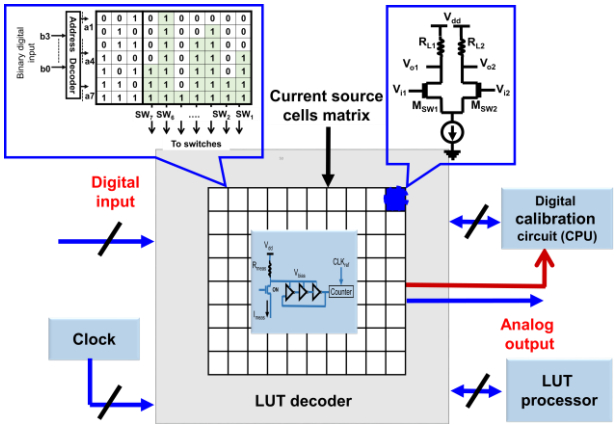

Fig. 9 Whole DAC block diagram.

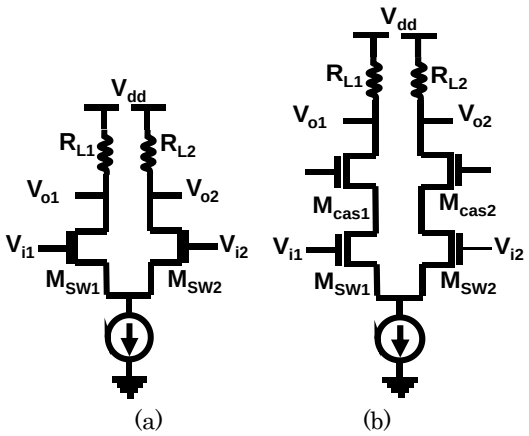

Fig. 10 Current source structure.
(a) Conventional. (b) Cascoded.

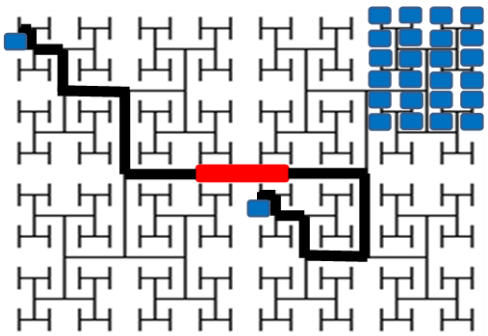

Fig. 11 Clock-tree based layout.

effects. Therefore, clock tree like (equal routing distance) layout has been taken place to reduce such effects. It provides more proper routing and less parasitic effects due to its balanced condition (Fig. 11). As a result, the overall dynamic performance of the proposed DAC is also improved.

Finally, with proposed digital algorithm and layout modification, a better linearity and high dynamic performance can be achieved (Fig. 12).

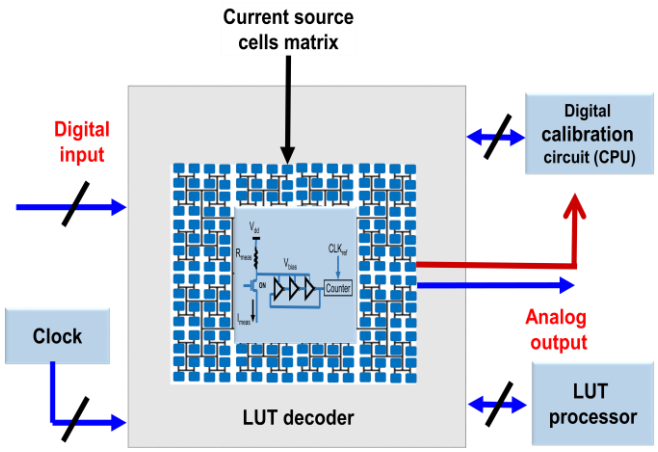

Fig. 12 Floor plan of the proposed DAC.

Table 1 Simulation conditions

Signal		Error	
Input freq fin,(MHz)	12.8	Standard deviation, σ	0.05
Sampling freq. fs, (MHz)	819.2	Mismatch	± 0.25
FFT points	32,768		

5. Simulation results

We have implemented the developed calibration technique to demonstrate a 12 bit half-unary weighted of the current-steering DAC using MATLAB simulation under the certain condition of frequency input 12.8 MHz with 0.05 standard deviation error and 50% mismatch (0.75 to 1.25A), and only current source mismatches are considered (Table 1).

In order to verify the linearity of the proposed DAC, the static performance parameters, INL and DNL have been simulated. The simulation result shows that the INL of 3.35 LSB obtained before calibration has been corrected using the proposed calibration technique. As a result, 0.88 LSB less than 1 LSB is obtained.

The difference between the lowest to the highest value is 1.48 LSB compared to 5.13 LSB before calibration (Fig. 13). At the same time, the DNL performance is also improved from 1.34 LSB to 1.00 LSB, and the peak to peak value is reduced from 2.34 LSB to 1.34 LSB (Fig. 14).

In the frequency domain, the proposed half-unary weighted DAC shows the SFDR performance of a 12-bit half-unary weighted DAC before calibration obtains 72.2 dBc (Fig. 15). After calibration, the same converter which obtains 99.2 dBc, which is better by 27 dB (Fig. 16).

For further verification, the comparison has been done by comparing the proposed algorithm with other 4 different algorithms:

① Thermometer-coded (TC) based unary weighted structure. (black solid line)
② 2-stage current source sorting (2S-CS) based unary weighted structure. (red solid line)
③ Thermometer-coded (TC) based half-unary weighted structure. (magenta dotted line)
④ 2S-CS based half-unary weighted structure. (blue dashed line)

Using the different number of bits (in this case, 8, 10 and 12), the INL performances are improved by 66%, 12%, 64% and 5% in average, compared to structure ①, ② ,③ and ④ respectively (Fig. 17), and INL is less than 1 LSB. The DNL also improves by 11% compared to ①, ② and ③ structures but is comparable to the structure ④ (Fig. 18). This happens due to the structures ① and ② that use unary cell while ④ and proposed structures use the virtual unary cell that formed through combination of two half-unary cells. However, even structure ③ performs half-unary structure but due to the TC switching scheme, the data-dependent effect is dominant.

We found from the simulation results that the SFDR of proposed technique obtains 18 dB better than structures ① and ③, 1-3 dB compared to structure ② and ④ (Fig. 19).

In order to confirm the performance of the SFDR, we also measured the level of second and third order harmonic distortions (HDs) (Fig. 20, Fig. 21). The proposed structure improves second order HD up to 34% and 33% compared to structure ① and ③, 7% and 6% to structure ② and ④ respectively. Third order HD also improves up to 36% and 33% compared to structure ① and ③, 7% and 5% to structure ② and ④ The improvement of these second and third order HDs is one of the contributor to the SFDR improvement which most nearest to the output signal while the others can be eliminated through an analog filter. By suppressing the effect of second and third order of HDs can relax the requirement of the analog filter and purer output signal can be achieved.

6. Conclusion

We have proposed a 3-stage current sorting technique for current steering DAC linearity improvement as well as its dynamic performance. The proposed structure with digital calibration

algorithm shows their improvement compared to other three structures. This technique improves not only INL but also DNL. The better SFDR can be obtained with second and third harmonics suppression. The key of this proposed depends on the accuracy of the measurement circuit.

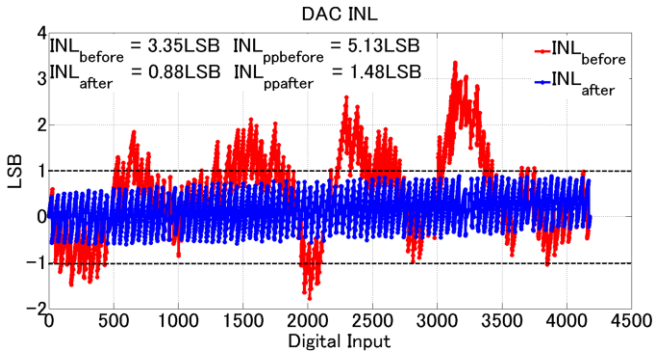

Fig. 13. INL performance.

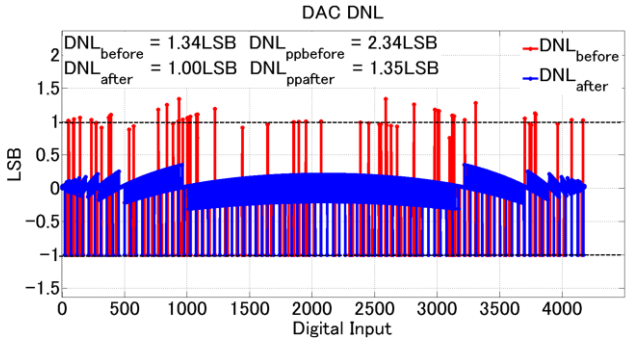

Fig. 14. DNL performance.

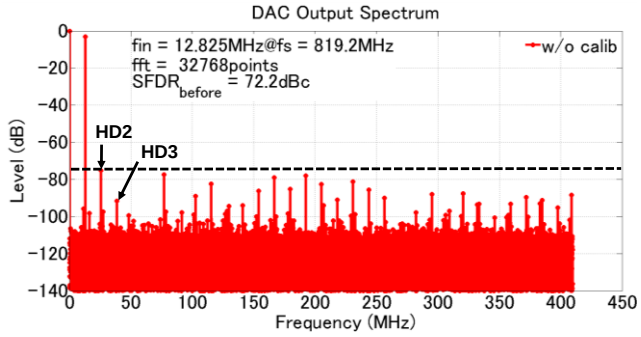

Fig. 15. Output spectrum before calibration.

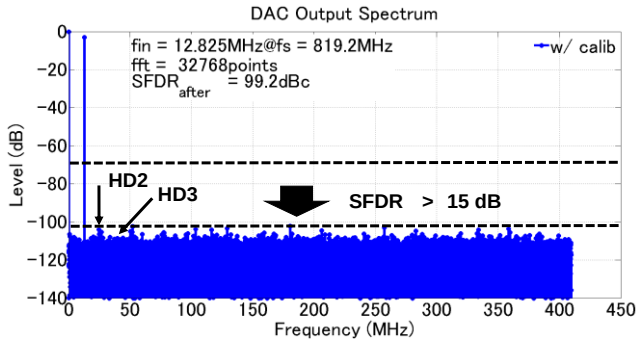

Fig. 16. Output spectrum before calibration.

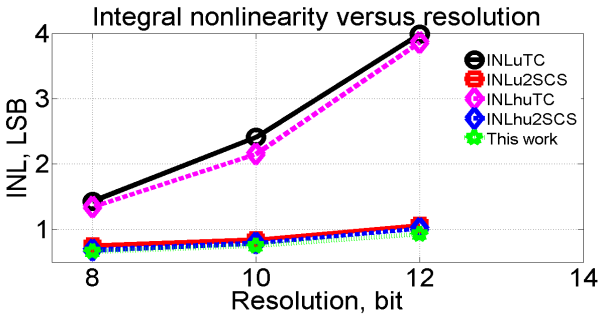

Fig. 17 Integral nonlinearity versus resolution.

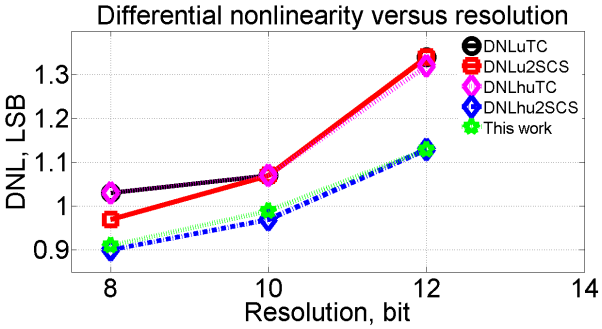

Fig. 18 Differential nonlinearity versus resolution.

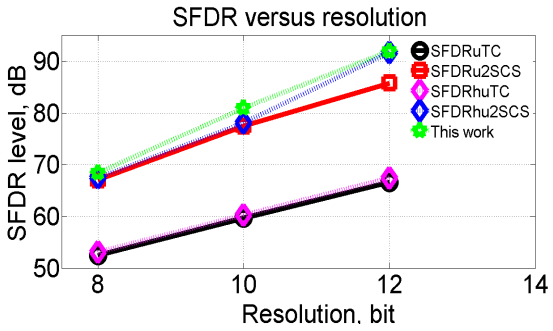

Fig. 19 SFDR versus resolution.

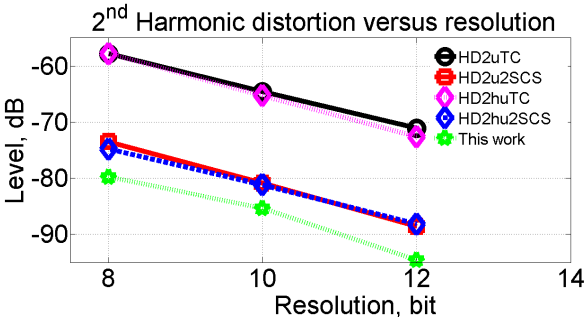

Fig. 20 2nd harmonic distortion versus resolution.

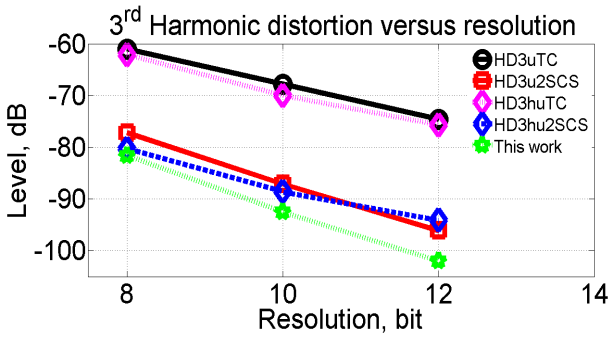

Fig. 21　3rd harmonic distortion versus resolution.

Acknowledgement

We would like to thank Semiconductor Technology Academic Research Center (STARC) for their valuable support on this project.

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