# Spread Spectrum Clock Generator With Adaptive Band Exclusion

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**Abstract** This paper proposes novel spread-spectrum clock generation (SSCG) algorithms that can select and exclude certain spectrum bands from spreading spectrum, adaptively to environmental signal functioning frequencies. This removes the need to choose certain bands for exclusion; as it is done automatically by open circuit designer hands to focus on their design only and not consider its clock EMI effects to other surrounding circuits. The proposed circuit algorithms are fast (reachable at high clock frequency) and flexible (programmable) by taking full advantages of digital circuit simplicity.

**Keywords** Spread spectrum clock generation, Adaptation, EMI, Band selection, Digital-to-Time converter.

## **1** Introduction

Electronics devices use clocks to synchronize data as they move from one place to another or to spot, or measure occurrence of values in time. A clock circuit functions on a certain frequency and radiates an energy that may interfere with other devices in vicinity. This radiation is called electromagnetic interference or EMI in short [1]. Communication watchdogs around the globe that regulates broadcast emission such as in radio or TV (like FCC in US) enforces a limit on EMI for all electronic equipment. Failing to fulfill this requirement prevents manufacturers from entering the market and/or causes delay shipment of final products; solving it is a very time consuming and costly task. Therefore assurance of compliance with EMI limits starts at the very early stage of

device manufacturing [2]. But staying below EMI limit is becoming more and more difficult these days by high increase in clock functioning frequency. Spread spectrum clock generator is a counter-measure which serves as a way to lower EMI [3]. It slows down or slows up clock speed within a few percent of its target frequency, thus hammering its EMI peak by spreading it across a range of frequencies (Fig. 1).



Fig. 1 Spread spectrum clock generator

Spread spectrum clock does not effect device overall performance; in fact here we have neglected cases that it might potentially effect positively as it drops the requirement to work in lower frequency to have a smaller energy radiated. However it requires other surrounding devices to be immune to the added noise in their performing spectrum [4]. Spread spectrum clock generators accomplish their targeted goal easily and satisfactorily and that has been the reason for it to be adopted as the de facto standard so far [5]. But it has very serious drawback; by distributing noise (EMI) in neighboring bands, it pollutes and therefore potentially disrupts surrounding devices that use surrounding frequency band as a mean of communication [6]. Recently with raise in usage of System on Chips (SoCs) and constant increase in consumer electronics and wireless device, this issue is in a deteriorating situation and needs immediate attention [7].

In this paper we have suggested a auto-configurable (therefore adaptive) Spread-Spectrum Clock Generator (SSCG) that dynamically changes clocks spread spectrum in a way to eliminate clock speeded collision with other desired signal in neighboring frequency bands.

While this method does not fully remove high EMI radiation and its distribution strength in neighboring spectrums but it is adds a very viable option for the circuit designers to make sure their speeded spectrum clocks noise does not collide with other desired signals in certain frequency as it extracts and eliminates noise in that band, and pushes it aside.

It is worth to mention that proposed method is based on recently introduced a delta-sigma digital-to-time converter by the authors of this paper and built convictions are all based on the benefits of spread spectrum clock generator built upon it which we discuss in the following sections.

# 2 Digital to Time Converter

Constant trend of device miniaturization and functioning frequency has led to rise in delta-sigma modulation methods popularity. The usage of lower resolution signal with higher samples in delta sigma method simplifies the overall circuit complexity and therefore benefits cost efficiency. Delta-sigma modulation converts the analog voltage into a pulse frequency output easily brought to time domain. This coarsely quantized output has found increasing usage in time domain signal processing [8]. In time domain signal processing, variable is always measured and analyzed against time rather than its amplitude. Functions such as electronic signals, market behaviors are some example of time domain values. Time domain signal processing superiority, arguably; is due to its lack of requirement for process such as filtering, amplifying and mixing plus its support for prediction and regression of the signal behavior over the time.

Further, time domain signal analysis makes it much easier to work in situation where the aim of analysis is to analyze and solve a time domain related problem; this paper's spread spectrum clock generator is such one.

Digital to Time converter (DTC) is an algorithm to bring and convert digital signals (in voltage domain) to analog signal in time domain (timing signal). The process if converting signal from digital to analog (and vice versa) usually involves many techniques such as filtering and smoothing of the signal before convention. In this regard, DTC is no different. DTC includes a digital  $\Delta\Sigma$ modulator and samples are interpolated with analog low pass filter (LPF). In DTC LPF is used to smooth the signal by cutting its high frequency components. Output signal are then converted to one-bit resolution timing signal (Fig. 2).



Fig. 2 Delta-Sigma DTC

DTC's output signal spectrum can easily be manipulated by the algorithm and chosen parameters in the conversion process and its usage was found in spread spectrum clock Generator and power circuits switching EMI removal.

# 3 Adaptive SSCG

In our research we found out that SSCG we have introduced previously [9] is a perfect match (or by some means the only available solution) for adaptive clock spread spectrum as it is a simple digitally implementable method to convert a clock based on digital values and is functional at high frequencies, implementable fully with digital circuit. With a delta-sigma DTC algorithm implemented in programmatically configurable digital circuit, location of the required exclusion spectrum bands can be sensed (by a switch or other measures) and DTC algorithm parameters can change automatically and output clocks shape can change on the fly (Fig. 3).



Fig. 3 Exclusion band

Adaptive SSCG can utilize only one form of many delta sigma DTCs proposed such as PCM or PPM or it can utilize multi methods and choose the method dynamically base on set conditions. (Fig. 5)



#### Fig. 5 Adaptive SSCG

For instance, in case of PCMDTC, based on external factor 1 to 3, PCM configuration changes adaptively and in result notch relocates accordingly (Fig. 6).

In contrast to formerly introduced SSCG, delta-sigma DTC methods, it dynamically computes output pulse timing signals characteristics and shifts the DTC method internally without affecting overall circuit design architecture.



Fig. 6 Notch relocation based on external factor

### 4 Conclusion

In this paper we have introduced the recent development in time domain signal analysis and current situating in its usage in DTCs. Then we talk about a method built over previously introduced SSCG with exclusive noise band to adaptively and dynamically change output pulses characteristics in order to tailor out or exclude certain bandwidth from spreading.

This opens up opportunity for circuit designer to priories their task of passing EMI compliance test for their unit without worrying too much about its later usage and effects on other surrounding electrical circuit equipment's.

The feasibility of current method has been verified by numerical analysis and its real world bench marking is in process of implementation in FPGA.

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## References

 B. Archambeault, C. Brench, O. Rahimi, EMI/EMC Computational Modeling Handbook, Springer Science+Business Media (2001).

[2]. S. Ben Dhia, M. Ramadani, E. Sicard, Electromagnetic Compatibility of Integrated Circuits,Springer (2006).

[3]. C. D. Hoekstra, "Frequency Modulation of System Clocks for EMI Reduction", Hewlett-Packard Journal, no.13, pp.1-7 (Aug. 1997).

[4]. T. Daimon, H. Sadamura, T. Shindou, H. Kobayashi, M. Kono, T. Myono, T. Suzuki, S. Kawai, T. Daimon, H. Sadamura, T. Iijima, "Spread-Spectrum Clocking in Switching Regulators for EMI Reduction", IEICE Trans. Fundamentals, vol. E86- A, no. 2, pp.381-386 (Feb. 2003)

[5]. I. Mori, Y. Yamada, S. A. Wibowo, M. Kono, H. Kobayashi, Y. Fujimura, N. Takai, T. Sugiyama, I. Fukai, N. Onishi, I. Takeda, J. Matsuda, "EMI Reduction by Spread-Spectrum Clocking in Digitally-Controlled DC-DC Converters", IEICE Trans. Fundamentals, volE92-A, no.4, pp.1004-1011 (April 2009).

[6]. S. Uemori, M. Ishii, H. Kobayashi, "Multi-Bit Digma-Delta TDC Architecture for Digital Signal Timing Measurement", IEEE International Mixed-Signals, Sensors and Systems Test Workshop, Taipei (May 2012).

[7]. H. G. Skinner, K. P. Slattery, "Why Spread Spectrum Clocking of Computing Devices is not Cheating", IEEE International Symposium on Electromagnetic Compatibility, vol.1, pp. 537- 544, Montreal (Aug. 2001).

[8]. R. Schreier, G. C. Temes, Understanding Delta-Sigma Data Converters, IEEE Press (2005).

[9]. R. Khatami, H. Kobayashi, et. al, "Delta-Sigma Digital-to-Time Converter and its Application to SSCG", The 4th IEICE International Conference on Integrated Circuits Design and Verification, Ho Chi Minh City, Vietnam (Nov. 2013).

[10]. R. Khatami, H. Kobayashi, Y. Kobori, "Delta-Sigma Digital-to-Time Converter For Band-Select Spread Spectrum", Key Engineering Materials (accepted).