SAR ADC Design Using Golden Ratio Weight Algorithm

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***Abstract*— This paper describes redundant successive approximation register (SAR) ADC design methods which enable high-reliability and high-speed AD conversion using digital error correction. Especially we propose to apply Fibonacci sequence and its property called Golden ratio to SAR ADC design to optimize redundant search algorithms. We present some interesting properties for well-balanced redundant SAR ADC design, as well as golden-ratio-weighted DAC topologies for its internal usage.**

Keywords—Successive Approximation; ADC; Redundancy; Digital Error Correction; Fibonacci Sequence; Golden Ratio

I. INTRODUCTION

Recently, automotive electronics are gathering attention for industry competitiveness of vehicles. SAR ADCs embedded in micro-controller for automotive electronics application need better performance such as high reliability, high speed and high resolution, and we study here redundancy design of SAR ADCs to realize them.

Redundancy design enables digital error correction for SAR ADC [1-4]. One method is to use a non-binary search algorithm instead of a binary search algorithm [1-4]. There, extra comparison steps and a non-binary weighted DAC are needed for a redundant SAR ADC and the designer to determine its non-binary weighted values. Generally, their values are determined using a non-binary radix or selected flexibly by the designer. However, a systematic redundant SAR ADC algorithm design method has not been studied well yet.

In this paper we discuss several methods to design redundant SAR algorithms based on number theory, and we obtain well-balanced non-binary weight values by applying properties of Fibonacci sequence such as the closest terms ratio called "golden ratio" and realization of all terms with integers (without fraction) [5]. We also describe some simple DAC topologies with golden ratio weights used internally for the golden ratio weighted SAR ADC.

II. SAR ADC

SAR ADCs are used for medium sampling speed and high-resolution applications. Since they have features of low power, small chip area, they are widely applied to such as automotive, factory automation. Also they do not require operational amplifiers, which is suitable for nano-CMOS implementation.

The SAR ADC consists of a sample-and-hold circuit, a comparator, a DAC, SAR logic and a timing generator (Fig.1). Conversion of the SAR ADC is based on principle of balance and generally it uses the binary search algorithm. Firstly, the sample-and-hold circuit acquires analog input voltage. Secondly, the comparator compares the input analog voltage and the reference voltage that is generated by the DAC and decides 1-bit digital output. Thirdly, SAR logic provides DAC input based on the comparator output. The input voltage and the updated DAC output voltage are compared by the comparator. This operation is repeated and finally SAR ADC can obtain the whole digital output.

Fig.2 shows the binary search algorithm of a 4-bit SAR ADC. The bold line in Fig.2 indicates the reference voltage value to compare with the analog input at each step. Their values are calculated by either sum or difference between the last step reference voltage and the weighted voltage p(k) of each step as shown in Fig.2. The comparator outputs 1 if the input voltage is larger than the reference voltage; otherwise it outputs 0. Then we obtain the digital output.

Usually, p(k) is a binary weighted value because the binary search algorithm is efficient. However in reality there is possibility of comparator misjudgment due to DAC incomplete settling, and sample-and-hold circuit incomplete settling as well as noise. In the binary weighted SAR ADC, one misjudgment of the comparator leads to incorrect output and low reliability. Hence this paper investigates redundancy design of SAR ADC to enable digital error correction for misjudgment of the comparator.

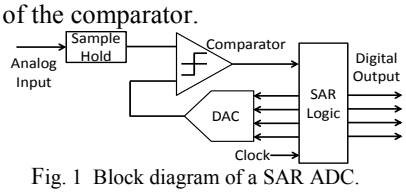

Fig. 1 Block diagram of a SAR ADC.

III. REDUNDANCY DESIGN OF SAR ADC

Redundancy design is a technique to improve circuit and system performance. To apply the redundancy design to the SAR ADC means adding extra comparison [1-4]. This method changes binary weights to non-binary weights for the DAC and realizes digital error correction with redundancy property.

Fig.3 shows an example of two redundant search operations of a 4-bit 5-step SAR ADC. There, the input voltage is around 8.3LSB and the reference voltage weights p(k) are 1, 2, 3, 6 and 8. The one operation (solid arrows) assumes that the comparison is correct, whereas the other (dotted arrows) assumes that it is incorrect. However both obtain the correct digital output of 8 by digital error correction. In the 4-bit 5-step SAR ADC as shown in Fig.3, there are 2^5 comparison patterns and 2^4 output patterns. In other words, a given output level can be expressed by multiple comparison patterns. Therefore even if comparator decision is wrong at some step, the correct ADC output may be obtained. This is the principle of digital error correction. In addition, even though the number of the comparison steps is increased, the digital error correction enables high-speed AD conversion as a whole,

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because the digital error correction can take care of the DAC incomplete settling [1-4]; thus redundancy design has potential for reliable and high-speed SAR AD conversion.

A. Generalization of redundant SAR ADC design

We generalize SAR ADC redundancy design from using some equations [2]. If we realize an N-bit resolution SAR ADC by M-step comparison (M≥N), the reference voltage Vref(k) at k-th step and ADC output Dout are defined by Eq.1 and Eq.2, respectively. Here k=1,2,3,4,…,M and p(k) is the reference voltage weight value for addition to (or subtraction from) the DAC input in the previous step. Moreover, each d(k) is decided by the comparator output. If the comparator digital output at k-th step is 1, then d(k)= 1, and if the comparator digital output at k-th step is 0, then d(k)= -1. Furthermore d(0)= 1.

$$\mathbf{V_{ref}(k)} = \sum_{\mathbf{i=1}}^{\mathbf{k}} \mathbf{d(i-1)p(i)}. \tag{1}$$

$$\mathbf{D_{out}} = \mathbf{0.5d(M) - 0.5} + \sum_{\mathbf{i=1}}^{\mathbf{M}} \mathbf{d(i-1)p(i)}. \tag{2}$$

We can also define "the redundancy at k-th step q(k)" as Eq.3.

$$\mathbf{q(k)} = \mathbf{-p(k+1) + 1} + \sum_{\mathbf{i=k+2}}^{\mathbf{M}} \mathbf{p(i)}. \tag{3}$$

Here q(k) indicates correctable difference between the input voltage and the reference voltage [2]. Even if the comparator result is wrong in the k-th step, we can obtain the correct output as long as q(k)>|Vin−Vref(k)| is satisfied. Fig.4 shows q(k) as an example of Fig.3. In Fig.4, one-way arrows indicate q(k), while two-way arrows show correctable input ranges. As shown in Fig.4, since q(1)>|Vin−Vref(1)| is satisfied, the SAR ADC can obtain the correct output in Fig.3. Therefore q(k) expresses the digital error correction capability. Moreover q(k) is defined by only the reference voltage weight p(k) in Eq.3, and thus p(k) is an important parameter in the redundant SAR ADC algorithm design.

B. Conventional method to decide reference voltage weight

Only reference voltage weight p(k) decides correction capability of the redundant SAR ADC; if the design of the reference voltage weight p(k) is not appropriate, the SAR ADC cannot have the maximum compensation ability. The ratio of the reference voltage weights p(k+1)/p(k) must be between 1 (unary) to 2 (binary). In conventional methods, we can obtain the k-th step reference voltage weight p(k) based on the radix x in Eq.4. Here, N is the ADC resolution, and M is the number of the whole steps.

$$\mathbf{p(k)} = \mathbf{x^{M-k}}. \tag{4}$$

Here 1<x<2 and $p(1)=2^{N-1}$. Additionally, the total number of steps M has to satisfy Eq.5 to enable all output level expression.

$$\mathbf{2^{N-1} - 1} \le \sum_{\mathbf{i=0}}^{\mathbf{M-2}} \mathbf{p(M-i)}. \tag{5}$$

We can systematically decide conditions for redundancy design based on the above equations.

C. Issues of Conventional methods

Conventional methods may have some issues. First, the reference voltage weight p(k) in Eq.4 is not an integer which is not suitable for the circuit design. Since the reference voltage weights p(k) must be integers for conversion accuracy, its rounding to an integer is needed to determine p(k). However rounding causes change of the radix and variability of the correction capability q(k), which may disturb performance improvement.

In addition, there is difficulty of appropriate radix choice. Fig.3 shows an example in case of radix 1.80 and rounding. However in Fig.4, two-way arrows indicate that correctable input range cannot cover all input range, which means that there are some ranges that cannot be corrected. In Fig.4, if ADC input is not within the range of 1~3, 7~9, 13~15[LSB], redundancy design becomes meaningless. Thus the inappropriate selection of a radix loses redundancy design effectiveness. On the other hand, the selection of a small radix for larger values of q(k) induces an increase in the number of SAR comparison steps and hence conversion time. In this way, there is a trade-off between correction capability and conversion speed, and the SAR ADC designer is forced to search a radix that is the most suitable for SAR ADC; these are causes of design difficulty.

IV. Redundancy Design Based on Fibonacci Sequence

We need further investigation of designing the redundant algorithm. Then we propose here a redundancy design method based on "Fibonacci sequence".

A. Fibonacci sequence

Fibonacci sequence is defined by a recurrence relation as shown in Eq.6, where n in Eq.6 is an integer greater than or equal to 0. It was presented in 1202 by Leonardo Fibonacci,

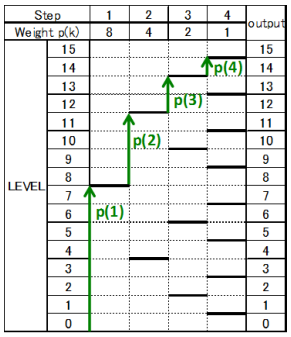

Fig. 2 Binary search algorithm of a 4-bit 4-step SAR ADC.

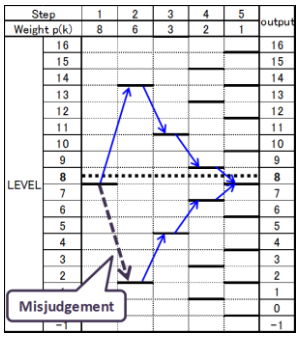

Fig. 3 Operation of a 4-bit 5-step SAR ADC in case of correct and incorrect judgments.

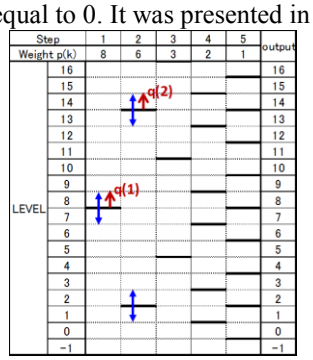

Fig. 4 4-bit 5-step SAR ADC algorithm and definition of correctable difference q(k).

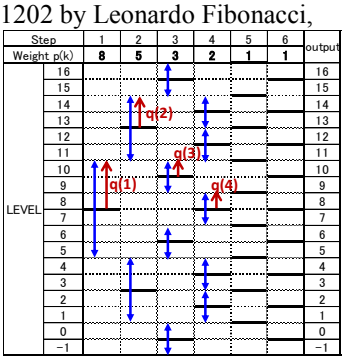

Fig. 5 Non-binary search algorithm using Fibonacci sequence of a 4-bit 6-step SAR ADC.

$$F_{n+2} = F_n + F_{n+1}. \quad (6)$$
$$F_0 = 0, \quad F_1 = 1.$$

Fibonacci numbers are expressed as the following by calculating Eq.6.

0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, 233, 377, 610…

In short, the sum of neighboring two terms is next term. In addition, the closest terms ratio of Fibonacci sequence converges at about 1.62 as shown Eq.7.

$$\lim_{n\to\infty} \frac{F_n}{F_{n-1}} = 1.618033988749895 \ldots = \varphi. \quad (7)$$

This ratio is called "Golden ratio", widely recognized as the most beautiful ratio. We can find Fibonacci sequence and Golden ratio in various places of our surroundings such as nature and human societies, and they have many interesting properties. [5]

B. Fibonacci sequence application to SAR ADC design

Eq.6 indicates that Fibonacci sequence numbers are integers, and Eq.7 indicates that the closest term ratio of Fibonacci number converges at about 1.62 called Golden ratio. In other words, Fibonacci sequence can generate a number string at radix 1.62 with only integer terms. In general, multiplication result of an integer and a decimal fraction is a decimal fraction, nevertheless multiplication result of an integer and a decimal fraction (1.62..) is an integer in Fibonacci sequence. Therefore we can apply Fibonacci sequence to the redundancy algorithm design of the SAR ADC using effective properties of the fixed rate and integer terms.

We select the reference voltage weight p(k) by using the Fibonacci sequence method as shown in Eq.8.

$$\mathbf{p(k)} = F_{M-k+1}. \quad (8)$$

Here p(1)=2^{N-1}. In short, we set p(k) to Fibonacci number in ascending order. Since p(k) follows the property of Fibonacci sequence, the proposed method can realize radix 1.62 by using only integers. Here the total number of steps M satisfies Eq.5.

Fig.5 shows a redundant search operation of a 4-bit 6-step SAR ADC using Fibonacci sequence as shown in Eq.8. One-way arrows indicate q(k) and two-way arrows show correctable input range as shown in Fig.5. We have discovered two interesting properties in Fig.5 as follows:

1) Correctable difference q(k) is Fibonacci number F_{M-k-1}.

2) q (k) of k-th step is exactly in contact with q(k+1) of k+1-th step without overlap. In other words, the tips of two-way arrows of k-th step and k+1-th step point exactly the same level as shown in Fig.5. This means that Fibonacci weight is q(k) boundary between overlap and separating.

C. Effectiveness of redundancy design using number theorys

We have obtained two properties by applying Fibonacci sequence to the redundancy design. In particular, the property 2 is important for design of redundant SAR ADC algorithm due to the following two reasons:

First, the property can be a standard of all redundancy design in the viewpoints of the radix of Fibonacci sequence which is golden ratio 1.62, and the boundary condition of q(k). Hence, we can assume that q(k) becomes overlap, non-overlap or separation by using golden ratio. If the radix value is larger than the golden ratio, the redundancy is small and q(k) boundaries are separated as shown in Fig.4. On the other hand, if the value of the radix is smaller than the golden ratio, the redundancy is large and q(k) boundaries are overlapped. Thus we can easily select the radix by considering the golden ratio as the standard.

Second, the redundancy design using Fibonacci sequence can be considered as the most efficient design. The property 2 indicates that q(k) covers wide input range by minimum extra comparison steps. Therefore, we can realize the redundancy design without waste by only integer terms. Moreover even if we change the first step reference voltage, property 2 holds.

The above two statements show that proposed method using Fibonacci sequence can solve the problems of conventional methods and contribute the efficient redundant algorithm design.

V. DAC Incomplete Settling

A. Summary and Generalization of DAC Incomplete Settling

An SAR ADC contains a DAC that outputs reference voltage by result of comparison at previous step. Since the DAC output must change from previous reference voltage to next one, the DAC output takes some time to settle. In binary search algorithm which does not have redundancy, the DAC must take time to settle between output voltage of DAC and next reference voltage within 0.5LSB for accurate conversion. This DAC settling time often dominates the SAR ADC conversion time. Besides, this settling time is much longer for high resolution SAR ADC. On the other hand, in non-binary search algorithm which has finite correctable difference q(k), the DAC can decrease settling time, thanks to redundancy and digital error correction at the following steps as shown in Fig.6.

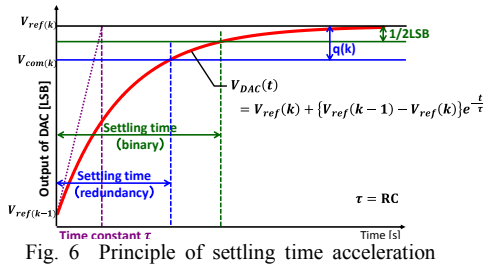

Fig. 6 Principle of settling time acceleration with incomplete settling of the internal DAC.

Difference between the DAC output voltage and the next reference voltage can be smaller than q(k) to accurate conversion when conversion step has correctable difference q(k). We generalize SAR ADC incomplete settling by using a first-order system as shown Fig.6. Firstly, we can obtain output voltage of the DAC as Eq.9 from Fig.6.

$$\mathbf{V_{DAC}(t) = V_{ref}(k) + \{V_{ref}(k-1) - V_{ref}(k)\}e^{-\frac{t}{\tau}}}. \quad (9)$$

Here, τ is a time constant of the DAC output.

To satisfy correctable condition at the redundant SAR ADC, difference between input voltage of the comparator and the reference voltage has to be smaller than q(k). Thus we can use comparison voltage Vcom(k), that has distance q(k) from the original reference voltage, to compare the input voltage. Consequently settling time Tsettle(k) which is the time to make k-th step comparison voltage can be the time to change the last comparison voltage Vcom(k−1) into next comparison

voltage Vcom(k). As we should consider the longest settling time to decide each step settling time, we obtain settling time Tsettle(k) as Eq.10.

$$\mathbf{T_{settle}(k)} = \boldsymbol{\tau} \ln\left(\frac{\boldsymbol{p(k)} + \boldsymbol{q(k-1)}}{\boldsymbol{q(k)}}\right). \quad (10)$$

Note that if correctable difference q(k) is less than 1LSB, we can regard q(k) as 0.5LSB. Finally, a variable clock SAR ADC takes sum of Tsettle as total settling time. However, for a fixed clock SAR ADC total settling time is equal to the longest span of Tsettle multiplied by the number of steps of SAR ADC used.

B. Analysis of Fibonacci SAR ADC settling time

We consider settling time of the redundant SAR ADC using Fibonacci sequence in theory. In Fibonacci sequence SAR ADC, we can transform Eq.10 to Eq.11 by using Eq.8 and property 1.

$$\mathbf{T_{settle}(k)} = \boldsymbol{\tau} \ln\left(\frac{\boldsymbol{F_{M-k+1}} + \boldsymbol{F_{M-k}}}{\boldsymbol{F_{M-k-1}}}\right). \quad (11)$$

Here we transform Eq.11 using Eq.6 as follows:

$$\mathbf{T_{settle}(k)} = \boldsymbol{\tau} \ln\left(\frac{(F_{M-k}+F_{M-k-1})+F_{M-k}}{F_{M-k-1}}\right) = \boldsymbol{\tau} \ln\left(2\frac{F_{M-k}}{F_{M-k-1}} + 1\right).$$

Therefore we obtain settling time of k-th step at SAR ADC using Fibonacci sequence as shown Eq.12 by using Eq.7.

$$\mathbf{T_{settle}(k)} = \boldsymbol{\tau} \ln(2\varphi + 1) = 1.444\tau. \quad (12)$$

Eq.12 indicates that settling time is constant regardless of step number k or usage of variable clock. On the other hand, conventional method using radix cannot realize constant settling time, because reference voltage weight p(k) does not have relationship for correctable difference q(k).

C. Simulation of Fibonacci sequence SAR ADC settling time

We compare the method of Fibonacci sequence and the method of radix in terms of redundant SAR ADC settling time. We have carried out comparison at 8-bit SAR ADC under the condition that variable clock and fixed clock, and obtained the results shown in Fig.7 using Eq.10. We found that total settling time using Fibonacci sequence is the shortest in fixed clock frequency for any ADC resolution.

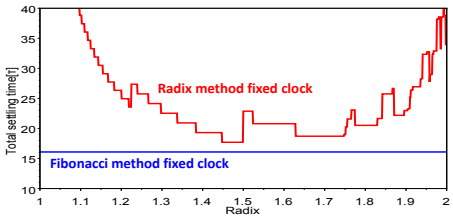

Fig. 7 Result of each method 8bit SAR ADC settling time simulation with 0.001 increment of radix.

VI. GOLDEN RATIO WEIGHTED DAC

This section shows several golden-ratio-weighted DAC topologies used for the Fibonacci sequence SAR ADC. Recall the Fibonacci numbers: 0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89...
Even terms are as follows: 0, 1, 3, 8, 21, 55...
Odd terms are as follows: 1, 2, 5, 13, 34, 89...

We have found that each node voltage in the R-R network with terminations of R (Fig.8 (a)) generates the voltage proportional to the even term, while that in the network with terminations of R||R (Fig.8 (b)) generates the voltage

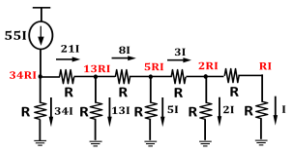

Fig. 8(a) R-R network with terminations of R generates the voltage proportional to the even term.

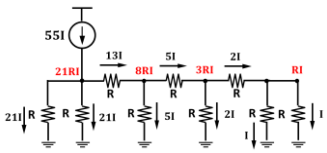

Fig. 8(b) R-R network with terminations of R//R generates the voltageproportional to the odd term.

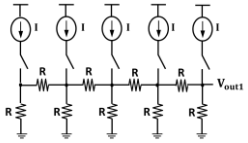

Fig. 9(a) Fibonacci even term weighted DAC.

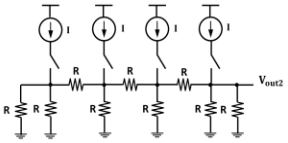

Fig. 9(b) Fibonacci odd term weighted DAC.

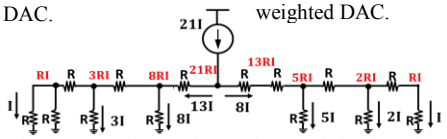

Fig. 10 Fibonacci number weighted voltage generation resistor network.

proportional to the odd term. Then Figs.9 (a), (b) show the DAC with Fibonacci even and odd term weights respectively, and a Fibonacci number weighted DAC can be realized by adding Vout1 and Vout2. The R-R network in Fig.10 generates voltages proportional to Fibonacci numbers and its combination with capacitors can realize another Fibonacci number weighted DAC. Similarly C-C networks also can realize other Fibonacci number weighted DACs.

VII. CONCLUSIONS

In this paper we have proposed redundancy SAR ADC algorithm design methods with applying properties of Fibonacci sequence, and we have obtained some important properties of the radix, the error correctable range with digital calibration for the SAR ADC and incomplete settling time. Besides, we found that our design method using Fibonacci sequence improves settling time compared to conventional redundant SAR ADCs. We have shown also several Fibonacci sequence or golden-ratio weighted DAC topologies. These results indicate that the proposed method contributes to realization of reliable and high-speed SAR ADC.

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