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A Gray Code Based Time-to-Digital Converter Architecture and its FPGA Implementation

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Outline

- Research Objective & Background
- Flash TDC and Problems
- Gray Code
- Gray Code TDC Architecture
- FPGA Implementation
- RTL Verification of Glitch-free Characteristic
- Conclusion

Research Objective

Objective

- Development of

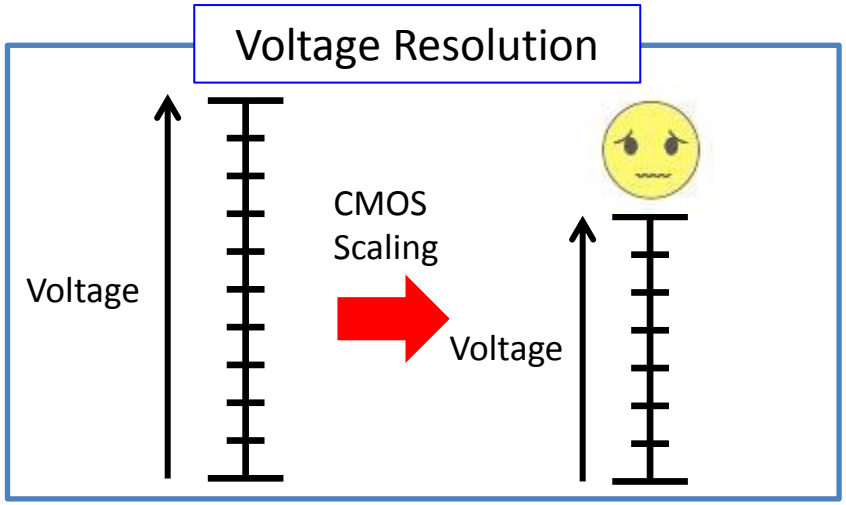
  Time-to-Digital Converter (TDC) architecture with high-speed and small hardware

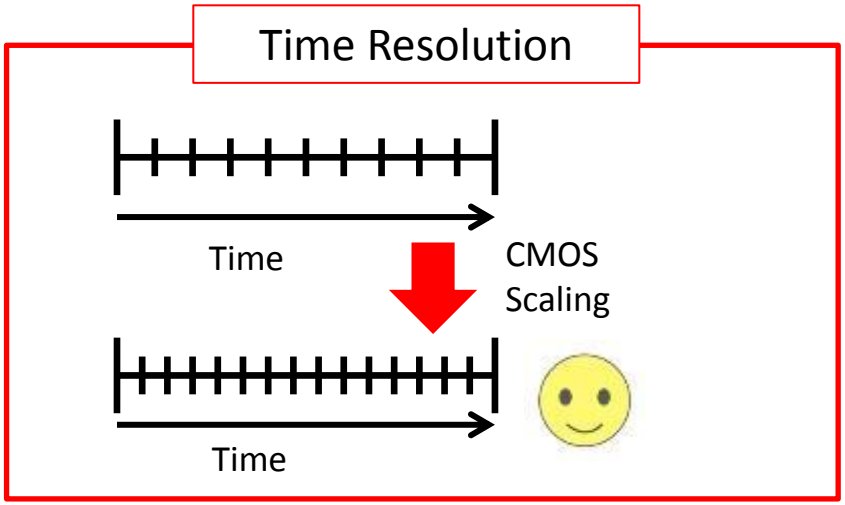
Approach

- Utilization of Gray code

Research Background

TDC plays an important role in nano-CMOS era



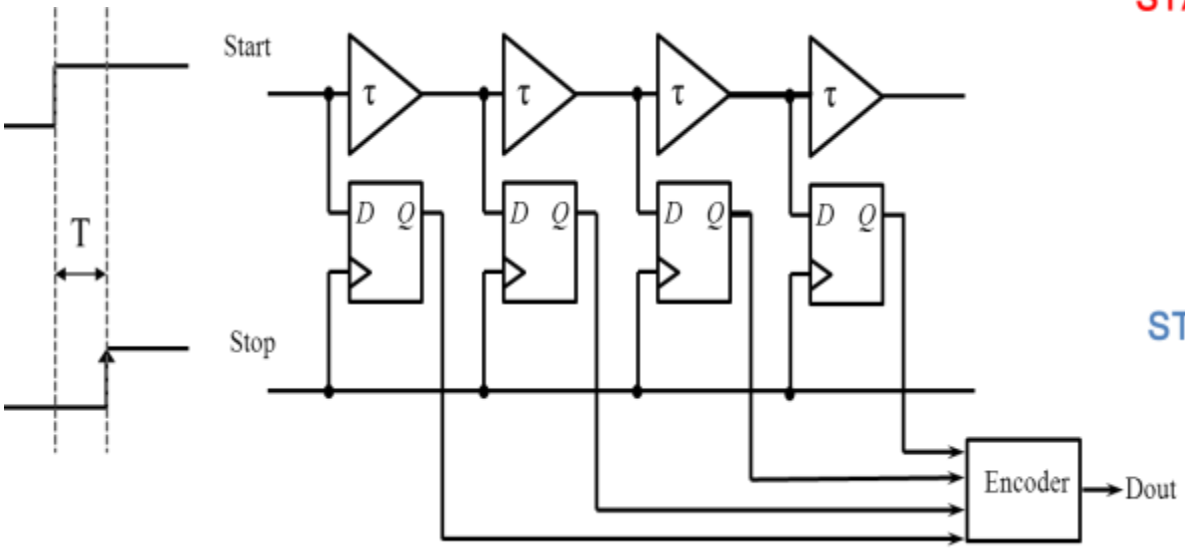


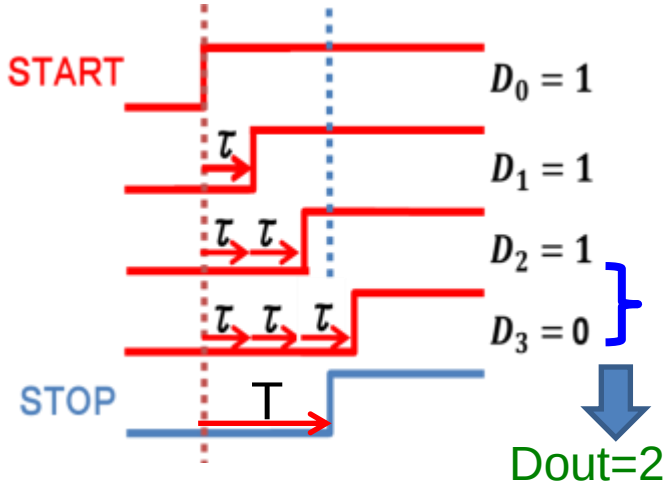
Voltage-domain resolution facing difficulties due to reduced supply voltage

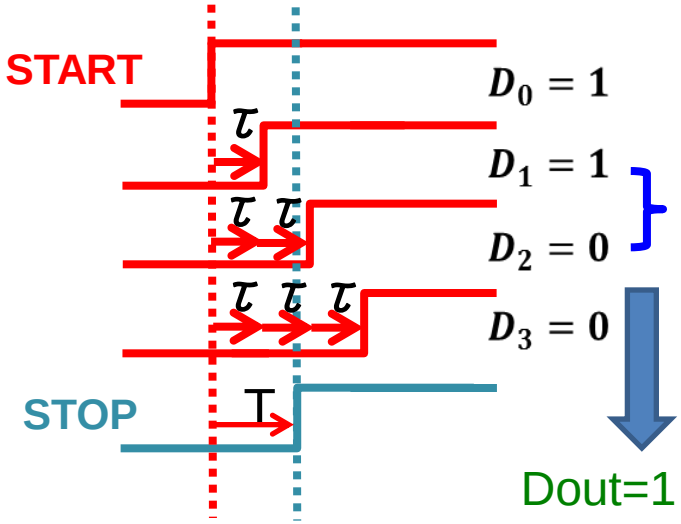
Time-domain resolution becoming superior

TDC measures time interval between two signal transitions, into digital signal.
(widely used in ADPLLs, jitter measurements, time-domain ADC)

Flash TDC







- Digital output (Dout) proportional to time difference between rising edges (T)
- Time resolution τ

Problems of Flash TDC

An n-bit flash TDC with 2^n quantization levels

Advantages

- High-speed timing measurement
- Single-event timing measurement
- All digital implementation

Disadvantages

- 2^n-1 delay elements, 2^n-1 Flip-Flops
- n-bit thermometer-to-binary code encoder

Large circuits
High power consumption

Gray Code (1/2)

Gray Code

a binary numeral system where two successive values differ in only one bit

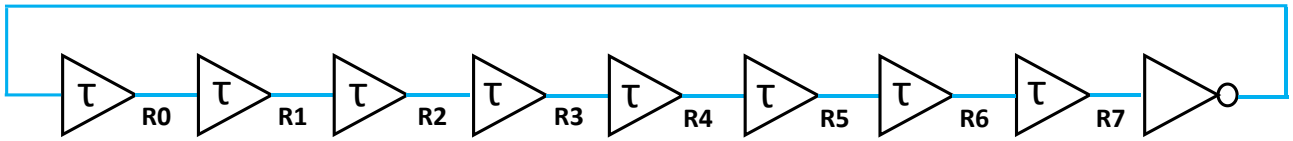
Table. 4-bit Gray Code

Decimal numbers	Binary Code	Gray Code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

- For Gray code, between any two adjacent numbers, only one bit changes at a time
- Gray code data is more reliable compared with binary code

Gray Code (2/2)

In a ring oscillator, between any two adjacent states, only one output changes at a time. This characteristic is very similar to Gray code.



8-stage Ring Oscillator Output								4-bit Gray Code			
R0	R1	R2	R3	R4	R5	R6	R7	G3	G2	G1	G0
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	1	1
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	1	1	0
1	1	1	1	1	0	0	0	0	1	1	1
1	1	1	1	1	1	0	0	0	1	0	1
1	1	1	1	1	1	1	0	0	1	0	0
1	1	1	1	1	1	1	1	1	1	0	0
0	1	1	1	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	0
0	0	0	0	1	1	1	1	1	0	1	0
0	0	0	0	0	1	1	1	1	0	1	1
0	0	0	0	0	0	1	1	1	0	0	1
0	0	0	0	0	0	0	1	1	0	0	0

For any given Gray code, its each bit can be generated by a certain ring oscillator.

Gray Code based TDC Architecture (1/2)

A Gray code TDC architecture can be conceived by grouping a few ring oscillators

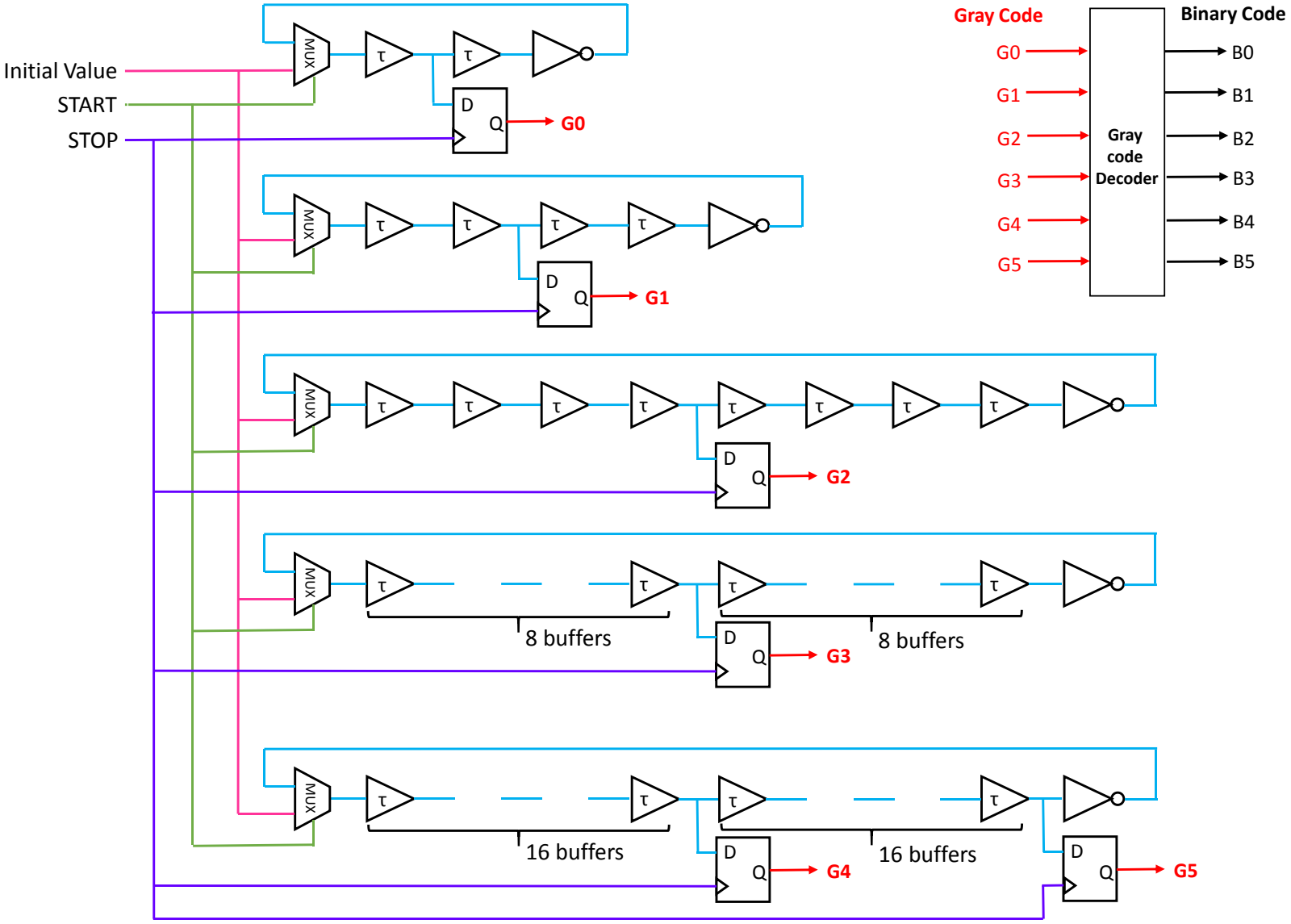
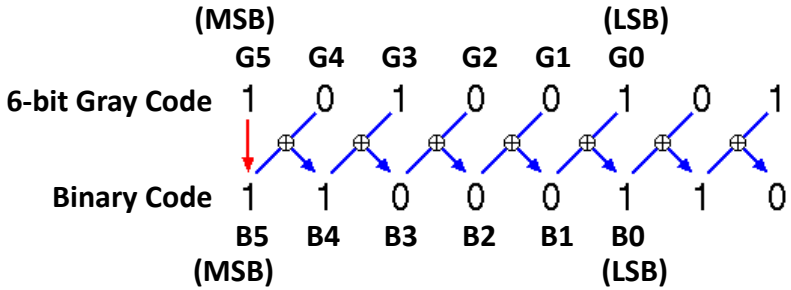


Figure. Proposed 6-bit Gray code TDC

Gray Code based TDC Architecture (2/2)



B5=G5
B4=B5 ⊕ G4
B3=B4 ⊕ G3
B2=B3 ⊕ G2
B1=B2 ⊕ G1
B0=B1 ⊕ G0

Figure. Gray code decoder

Flash vs. Proposed TDCs

for a measurement range of 2^6

	Flash TDC	Proposed TDC
Number of delay elements	64	62
Number of Flip-flop	64	6
The maximum stage	64	32

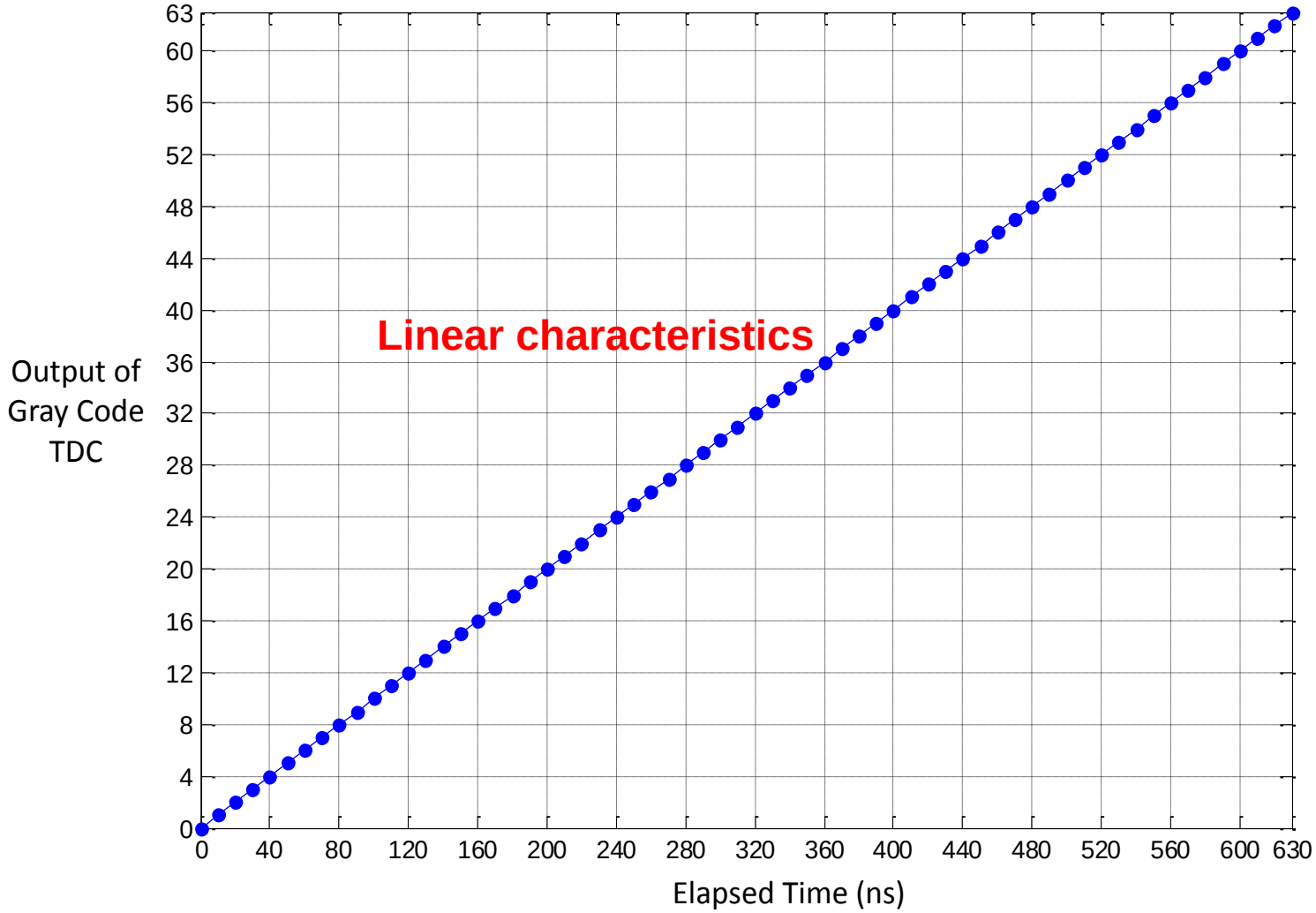
for a measurement range of 2^n significant hardware reduction as # of bits increases.

FPGA Implementation (1/3)

Proposed TDC implementation on Xilinx FPGA

Note: ADC is difficult to implement with full digital FPGA.

FPGA Implementation (2/3)

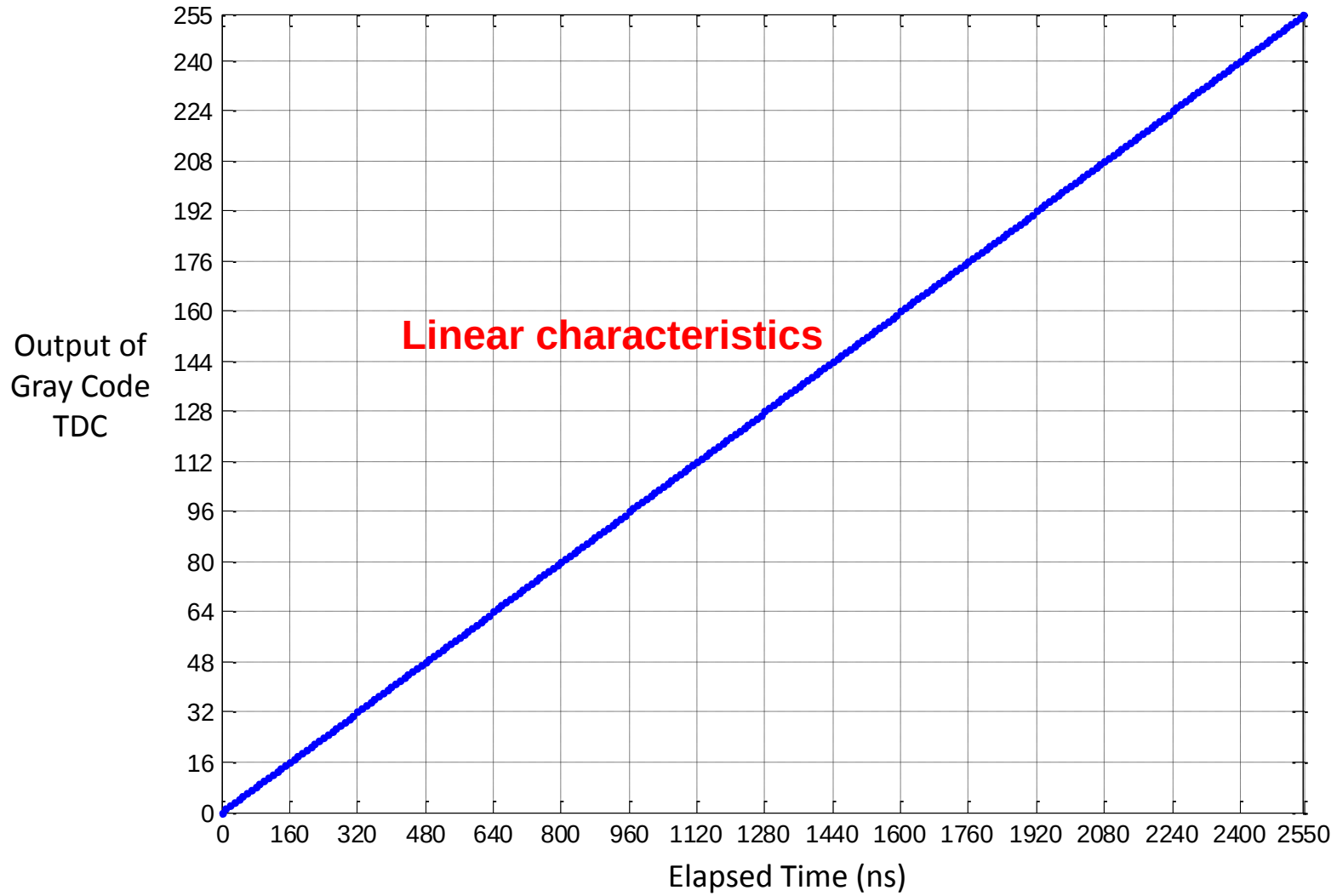


Measurement results of the proposed TDC with FPGA (6-bit case).

Proposed TDC operation is confirmed with FPGA evaluation.

FPGA Implementation (3/3)

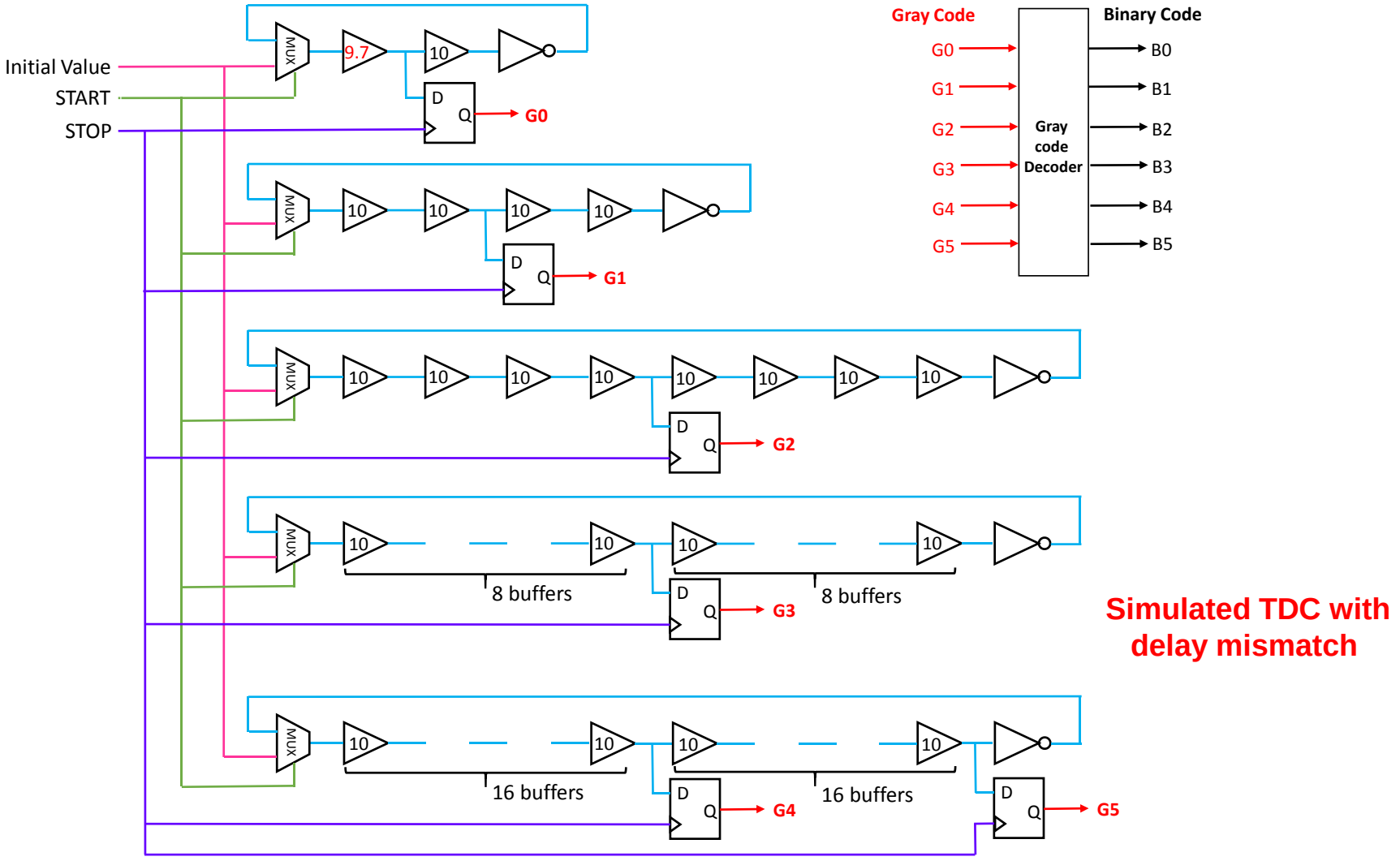
Similarly, 8-bit Gray code TDC architecture was implemented on FPGA.



Measurement results of the proposed TDC with FPGA (8-bit case)

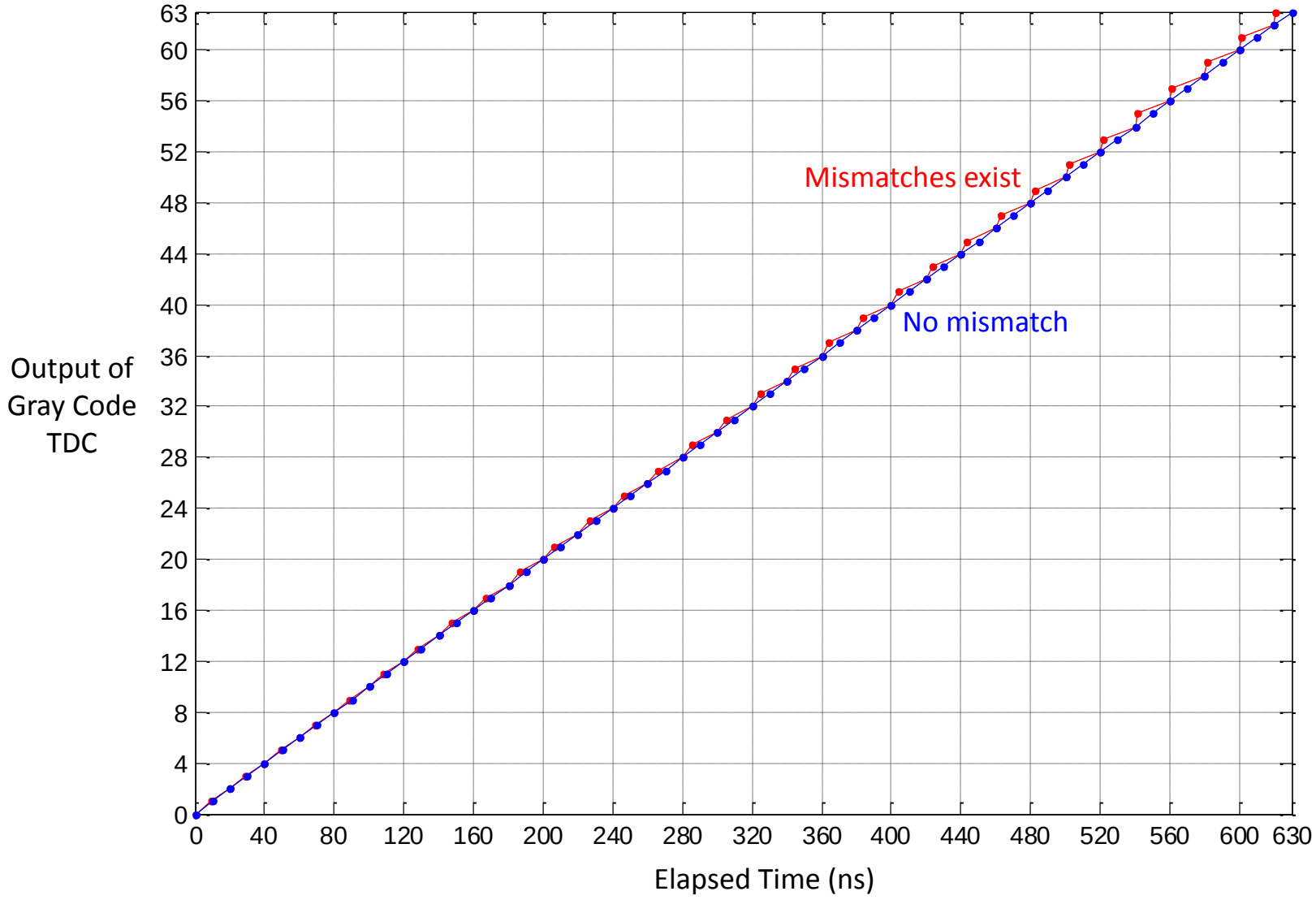
RTL Verification of Glitch-free Characteristic (1/2)

- The proposed Gray code TDC can provide a glitch-free binary code sequence even there are mismatches between the delay stages.
- RTL simulation was conducted to verify this characteristic.



RTL Verification of Glitch-free Characteristic (2/2)

- RTL simulation result shows that no matter there are mismatches among the delay stages or not, the proposed Gray code TDC can always output a glitch-free binary code sequence.



Conclusion

We have proposed a gray code based TDC architecture

- Comparable performance to Flash TDC
- Significant hardware & power reduction

for a measurement range of 2^n

	Flash TDC	Proposed TDC
Number of delay elements	2^n	$2^n - 2$
Number of Flip-flop	2^n	n
The maximum stage	2^n	2^{n-1}

Significant hardware reduction as # of bits increases.

We have implemented the proposed TDC with FPGA

➡ Confirmed its operation