High Efficiency ZPS-PWM Dual-Output Converters with EMI Reduction Method

Yasunori Kobori, Nobukazu Tsukiji, Nobukazu Takai, Haruo Kobayashi

***Abstract*— In this paper, we study a Pulse-Width-Modulation (PWM) controlled Zero-Voltage-Switching (ZVS) for single-inductor dual-output (SIDO) converters. This method can meet the industry demands for high efficiency due to ZVS and small size and low cost, thanks to single-inductor per multiple voltages. We show the single-inductor single-output (SISO) ZVS buck converter with its operation and simulation and then the experimental results. Next proposed ZVS-PWM controlled SIDO converters are explained in the simulation. Finally we have proposed EMI reduction method with spread spectrum.**

Keywords*— *DC-DC Switching Converter, Zero-Voltage-Switching Control, Single-Inductor Dual-Output Converter, EMI Reduction, Spread Spectrum

I. INTRODUCTION

Nowadays, various voltages are required in order to operate electrical appliances, where usually DC-DC converters of the same number as the voltages are required, and one inductor is required for one converter. Such a configuration is expensive and they occupy considerable board area because the inductor size is relatively large. Therefore, there is an increasing interest in single-inductor dual-output (SIDO) converters. We have investigated DC-DC buck converters with SIDO configuration. For example, our recent study reported hysteresis control for SIDO converters [1]. In this paper we present a SIDO converter as well as a SISO converter using ZVS-PWM method. Finally, in order to reduce the EMI noise, spread spectrum with analog noise[2] for ZVS-PWM SISO converter is reported.

II. SISO CONVERTER WITH ZVS-PWM CONTROL

A. SISO Buck Converter with ZVS-PWM Control

Figure.1 shows our SISO buck converter with ZVS-PWM control. This circuit differs from the typical step-down converter; there is a ZVS detection comparator and a resonant capacitor Cr. The ZVS detection comparator is used to compare the voltages of Vsw and Vin. When Vsw is larger than Vin, the comparator output is Hi, and a Flip-Flop becomes a SET state by receiving the Hi signal from the comparator. Then M1 is turned ON. In this way, the switching FET M1 is turned ON until the voltage difference between Vin and Vsw (which is the voltage of the diode) becomes zero. The capacitance Cr is required to adjust the time so that the voltage Vsw is increased to the voltage Vin. Table 1 shows the parameters of the converter.

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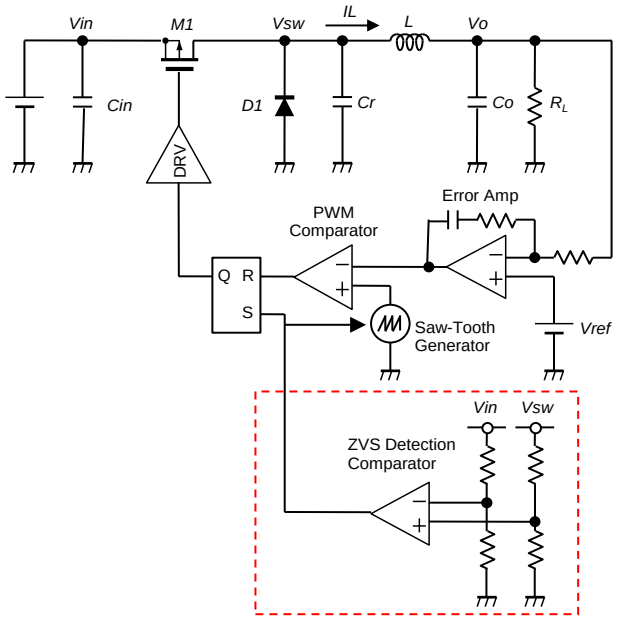

Figure 1. SISO buck converter with ZVS-PWM control.

Table 1. Simulation Parameters of the converter

Parameter	***Value***
Vin	10 V
Vo	6.0 V
L	1.0 uH
Cr	47 nF
Co	470 uF
Io	0.30 A

Figure 2 shows simulation results of the steady-state waveforms of the SISO buck converter with ZVS-PWM control. We see that the circuit operates as designed. Detailed description of the operation is as follows:

(1) During State 1, PWM signal is Hi and M1 is turned ON. In this period, the terminal voltage Vsw is equal to Vin. In addition, the current IL is increased at the rate of (Vin-Vo) / L. Cr is charged to Vin during this period.

(2) During State 2, PWM signal is Lo, and M1 is turned OFF. In this period, D1 is turned OFF, and the current IL is supplied to the output by Cr which is charged during State 1. At the voltage Vsw gradually

decreases due to the current supply from Cr. Finally, the voltage Vsw decreases to negative voltage until D1 is turned ON.

(3) During State 3, the voltage Vsw is negative and D1 is turned ON. The inductor current IL flows through the diode from GND. The current IL decreases at the rate of Vo/L. Cr is charged to a negative voltage equal to the forward bias voltage of D1.

(4) During State 4, the current IL is negative and D1 is turned OFF. The current IL flows through the diode from Co to Cr. The voltage Vsw increases from negative to positive voltages gradually with supply current to Cr. Then, the voltage Vsw reaches Vin and the ZVS detection comparator outputs a signal Hi. Then M1 is turned ON and the state returns to State 1.

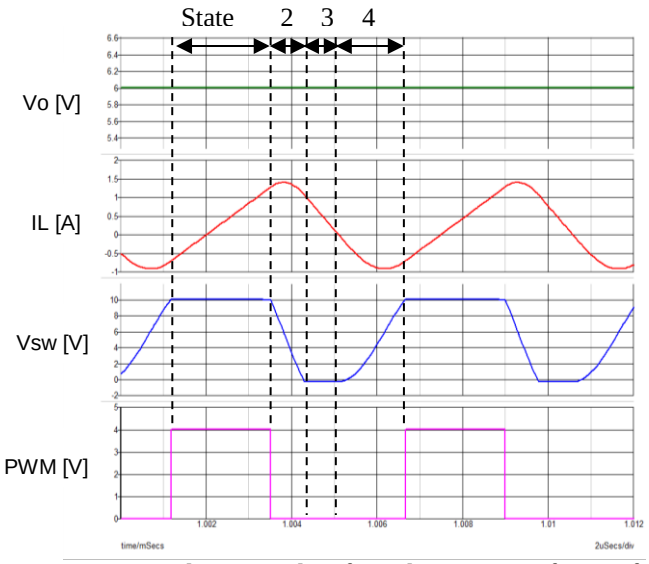

Figure 2. Simulation results of steady-state waveforms of the SISO buck converter with ZVS-PWM control.

Thus the switching losses are reduced with ZVS using the above method in SISO buck converter.

B. *Exprimental results of SISO Buck Converter*

Figure 3 and Fig. 4 show the experimental results of the SISO buck converter with the ZVS-PWM control method. The output voltage is stable of 6.0 V but the output voltage ripple is a little bit large 50mVpp. Seeing the waveform of ⊿Vo in Fig.3, the wave is step up or down. This means that there is a impedance like the ESR (Equivalent Series Resistance) or the line impedance of ground line, because we have made this circuit on the universal board.

The operation frequency is about 250 kHz with the output current 0.3 A. The current of the inductor I_L is like a triangular shown in Fig. 3. The low level of I_L reached less than zero voltage and the peak level is about 0.7 A which is decided by the output current.

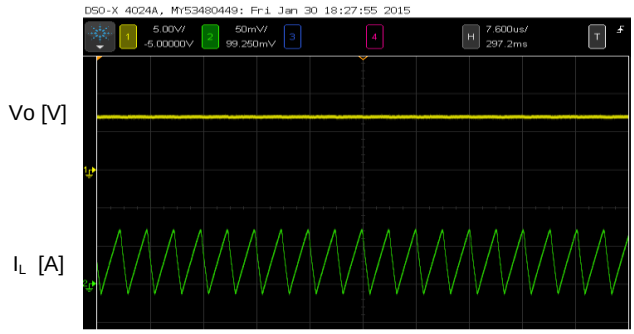

Figure 3. Experimental results of SISO converter

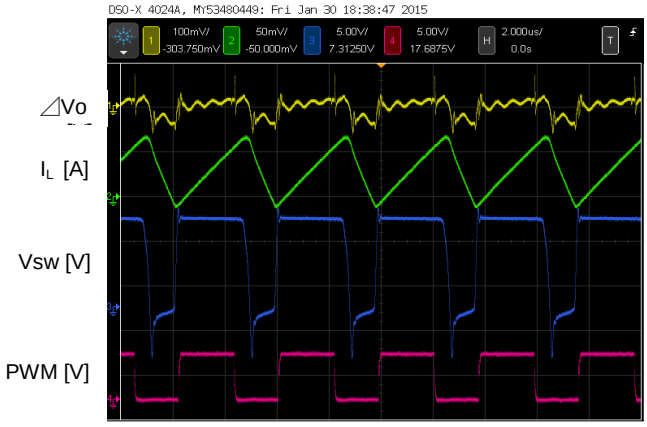

Figure 4. Experimental wave forms of SISO converter

Ⅲ. SIDO BUCK CONVERTER

C. *SIDO Buck Converter with ZVS-PWM Control*

Figure 5 shows a SIDO buck converter with the ZVS-PWM control method and the parameters of this circuit are shown in Table 2. There SEL signal is generated to determine whether the inductor current is supplied to Vo1 or Vo2 by comparing ΔVo1 and ΔVo2; Vo1 is selected when ΔVo1 > ΔVo2. We call this as "exclusive control." It is at the timing when ZVS signal is detected and M1 is turned ON.

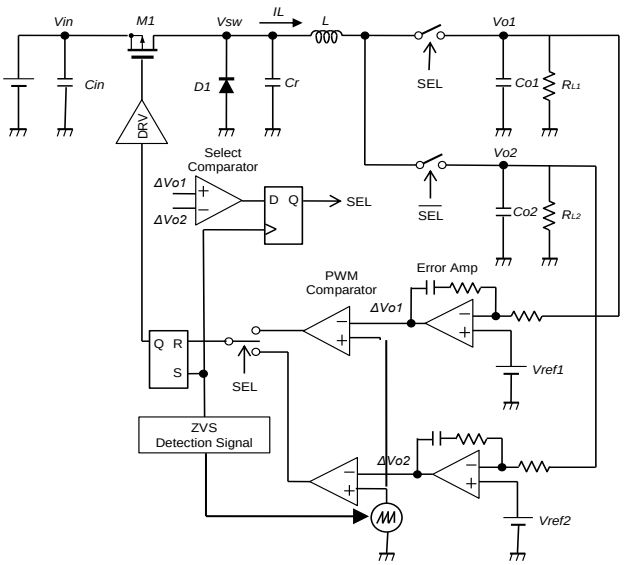

Figure 5. SIDO buck converter with ZVS-PWM control.

TABLE 2. PARAMETERS OF SIDO CONVERTER

Parameter	*Value*
Vin	10 V
Vo1	6.0 V
Vo2	5.5 V
L	2.2 uH
Cr	1.0 nF
Co1 & Co2	470 uF

Figure 6 shows the simulation results of steady-state waveforms of the SIDO buck converter with ZVS-PWM control and Table III shows their simulation conditions. We see that the circuit operates as designed.

Figure 7 shows the transient response when the load currents are change with parameters in Table III. We see that both the self- and cross-regulation voltages are in the order of several ±15mV which is less than ±0.3% of Vo1, Vo2. This result is satisfactory in many applications.

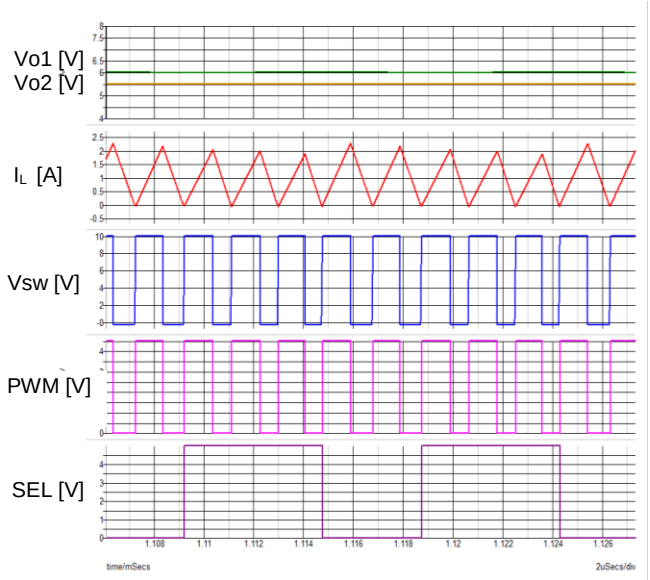

Figure 6. Simulation results of SIDO converter

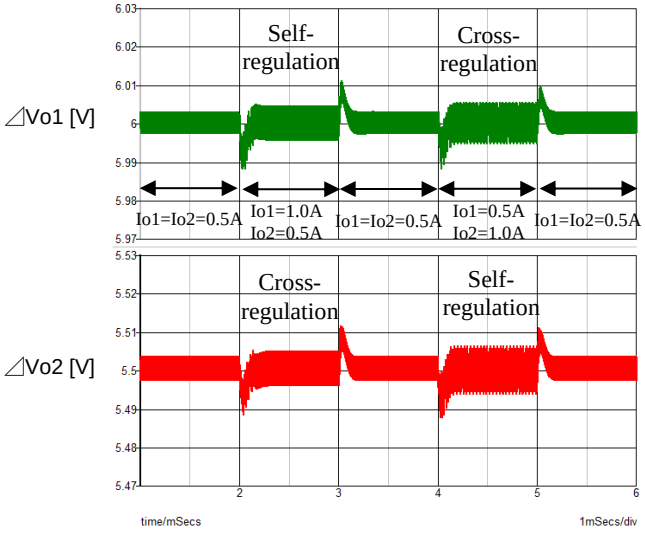

Figure 7. Transient response of SIDO converter

IV. SPREAD SPECTRUM METHDOLOGY

D. Spread Spectrum in Converters

Figure 8 shows the image of spread spectrum. The number of generated line spectrum is proportional to that of modulation, and noise energy is spread discretely in conventional digital spread.

In the conventional digital spread method of Fig.8(a), the spectrum of fundamental frequency turns into modulated spectrums of its both side when the number of modulation frequency is only one. In Fig.8(b), analog spread is expected to reduce the spectrum level more than digital spread, because it spread in a wide range of the frequency through continuous fluctuation of the phase.

Figure 9 shows the switching converter with the PWM signal which is generated by comparing between the amplified error output voltage and the saw-tooth signal. In a spread spectrum method, a small analog noise is added to the referencevoltage.

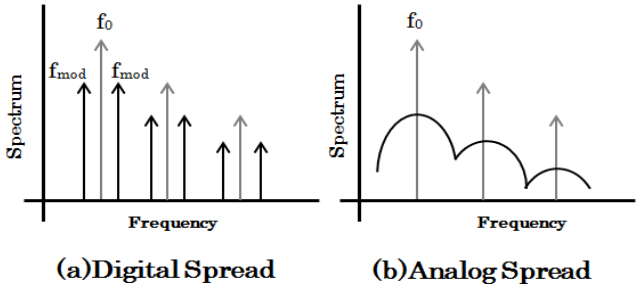

Figure 8. Image of EMI reduction with spread spectrum

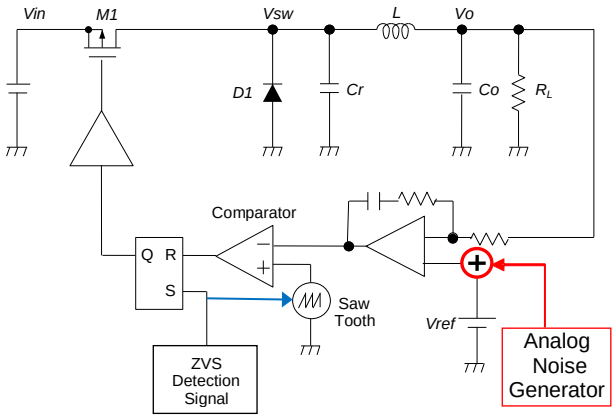

Figure 9. ZVS-PWM converter with analog noise generator

E. Analog Noise Generator

Figure 10 shows M-sequence circuit, D/A converter and a LPF circuit. M-sequence circuit is known as a method to generate random digital noise. It is composed of shift registers and Exclusive ORs. It generates the number of $N=(2^n-1)$ levels on the basis of the bit number n of primitive polynomial. There are two primitive polynomials of three degree as bellow. The output of M-sequence circuit (Eq. 1) is converted to the analog step pattern and it is smoothed to the analog noise by the LPF circuit shown in Fig. 11.

$$G(x) = x^3 + x^2 + 1 \quad (1)$$

$$G(x) = x^3 + x + 1 \quad (2)$$

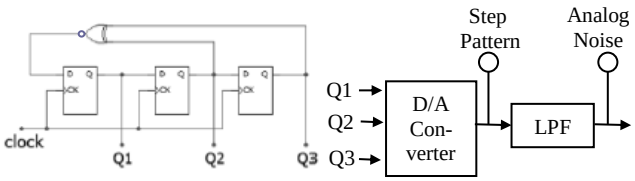

Fig. 10 M-sequence circuit and analog noise generator

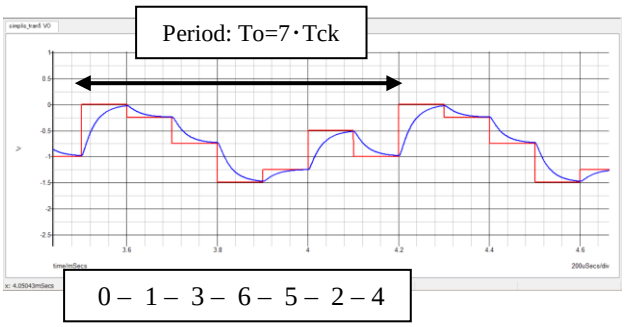

Figure 11. Step pattern and the analog noise

Figure 11 shows the output analog step pattern levels and the output of the LPF circuit. The step pattern is converted bits binary code by M-sequence circuit based on Eq. (1). There are cyclic pattern of 7 levels with 0-1-3-6-5-2-4 (shown in negative). In this step pattern, there are only seven levels. In order to make much more levels, this pattern is smoothed by the LPF circuit to the analog noise. In this case, the analog noise is periodic signal. The clock frequency of this signal is 10 kHz.

On the other hand, the ZVS-PWM switching converter does not use a clock and its frequency of the control signal is always changed in small level because of the negative feedback control circuit. So the control signal of the converter is not a periodic signal nor synchronized with the periodic analog noise shown in Fig.11.

F. Simulation Results with Spread Spectrum

Figure 12 shows the output voltage ripple and the analog noise. The output ripple is about 10 mVpp. Here, the shape of the voltage ripple is not similar to that of the analog noise. Parameters of this SISO converter are same as shown in Table 1.

Figure 13 shows the spectrum of the control pulse (the PWM pulse) in the ZVS controlled converter without analog noise modulation. Parameters of this SISO converter are same as shown in Table 1. In this case, the controlled basic frequency is about 377 kHz and the peak level of this frequency is 3.0V and there are high level spectrums at harmonic frequencies. The peak level of 1.13 MHz (the frequency at three times of basic frequency) is about 900 mV.

Figure 14 shows the spectrum of the control pulse in the ZVS controlled converter with analog noise modulation. The peak level of the spectrum of the basic frequency is reduced to 1.2 V (- 4.0 dB) and the level of 1.13 MHz is to 400 mV (-3.5 dB). There is no line spectrum.

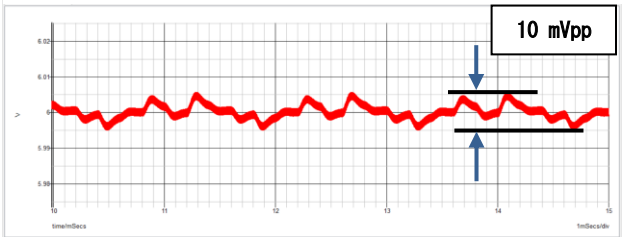

Figure 12. Output Voltage Ripple with analog noise modulation

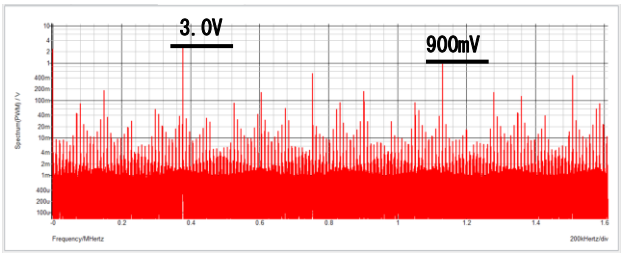

Figure 13. Spectrum of the control pulse of ZVS converter without analog noise modulation

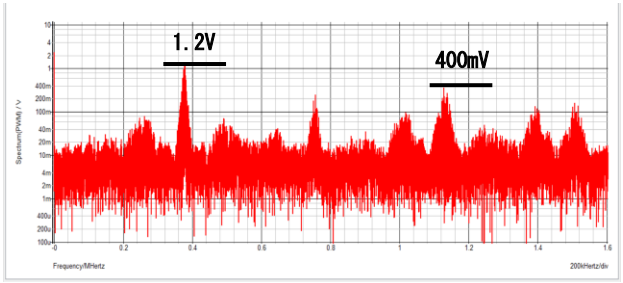

Figure 14. Spread spectrum of the control pulse of ZVS converter with analog noise modulation

III. CONCLUSION

We have described ZVS configuration, operation and experimental results for SISO buck converter. We have extended this ZVS method to SIDO converters and shown their simulation results in the steady state as well as in the transient state. We consider that ZVS will improve the efficiency of these SISO and SIDO converters, which we will investigate in theory and simulations. the switching converters with ZVS control are expected to realize high efficiency power supply circuits.

REFERENCES

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