EMI Reduction by Extended Spread Spectrum in Switching Converter

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Abstract: This paper proposes new EMI reduction method by extended spread spectrum using the PLL circuit with pseudo analog noise which is produced from new M-sequence circuit. The PLL circuit makes the reference clock modified with non-periodic analog noise which is supplied from new 3-bit M-sequence circuit. New pseudo analog noise is produced by inversing and/or exchanging the 3-bit. Using this modified clock from the PLL circuit for the saw-tooth signal in the switching converter, the spectrum of the PWM pulses is widely spread and the peak levels of the spectrums of the fundamental frequency and the harmonic frequencies are much reduced.

(Keywords, EMI Reduction, Spread Spectrum, PLL Circuit, Pseudo Analog Noise, Switching Converter)

1. Introduction

In recent years, the expansion of the use of mobile devices has been accelerated by the progress in an information society. The switching power converter is well known for its downsizing, light weight and high efficiency. As for the Pulse Width Modulation (PWM) control method is usually used for the switching converters, however, electromagnetic noise concentrates at a specific frequency of PWM signal and higher harmonics, which causes an Electro Magnetic Interference (EMI) problem. While the standards for EMI are getting strict along with the spread of electronic equipment, a reduction of the electromagnetic noise is very important for the switching converter.

This paper proposes new method topologies in order to reduce the EMI noise using spread spectrum method by adding fluctuation to PWM signal to modulate the phase of PWM signal. The conventional method of spread spectrum[1][2] is to use only discrete digital spread and has a limit to the noise reduction. In contrast, analog spread method[3][4] is able to spread the main spectrum continuously to reduce the noise more than conventional digital spread method.

2. Spread Spectrum Methodology

2.1 Spread Spectrum

Fig.1 shows the image of spread spectrum. The number of generated line spectrum is proportional to that of modulation, and noise energy is spread discretely in conventional digital spread.

In the conventional digital spread method of Fig.1(a), the spectrum of fundamental frequency turns into modulated spectrums of its both side when the number of modulation frequency is only one. In Fig.1(b), analog spread is expected to reduce the spectrum level more than digital spread, because it spread in a wide range of the frequency through continuous fluctuation of the phase.

$$F_{mod} = f_0 \pm \triangle f$$

Fig.2 shows the switching buck converter with the PWM signal which is generated by comparing between the amplified error output voltage and the saw-tooth signal. In a spread spectrum method, the phase or the frequency of the saw-tooth signal is usually modified in order to spread the spectrum.

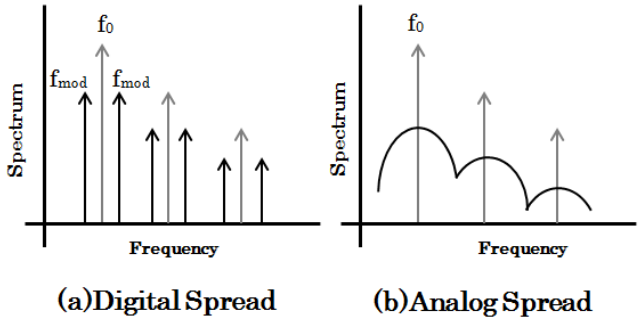

Fig.1 Image of EMI reduction with spread spectrum

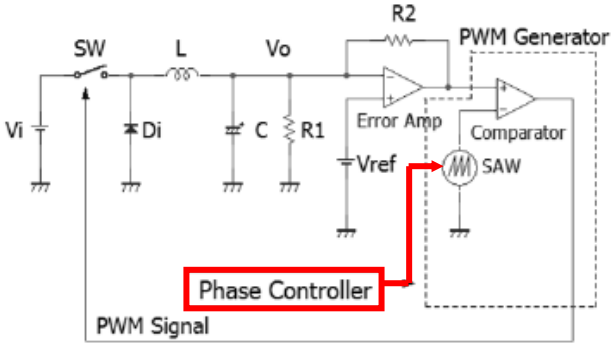

Fig.2 Block Diagram of Switching Converter with PWM phase modulator

2.2. Pseudo Analog Noise and PLL Clock Generator

M-sequence circuit shown in Fig.3 is known as a method to generate random digital noise. It is composed of shift registers and Exclusive ORs. It generates $N=(2^n-1)$ levels on the basis of the bit number n of primitive polynomial. There are two primitive polynomials as bellow.

$$G(x) = x^3 + x^2 + 1 \qquad (1)$$

$$G(x) = x^3 + x + 1 \qquad (2)$$

Fig.4 shows the output analog levels converted bits binary code by M-sequence circuit based on Eq. (1). There are cyclic pattern of 7 levels with 0-1-3-6-5-2-4 shown in Fig. 4. Fig. 5 shows the block diagram of the modified clock generator with the pseudo analog noise generator and the PLL circuit. In this figure, the output signal of the LPF is pseudo analog noise we call. The PLL circuit including the VCO (Voltage Controlled Oscillator) makes the non-periodic clocks modified by frequency, because the characteristics of the PLL is not strongly locked with the reference clock. The clock frequency of M-sequence circuit is 8.1 kHz (Tck=0.123 us).

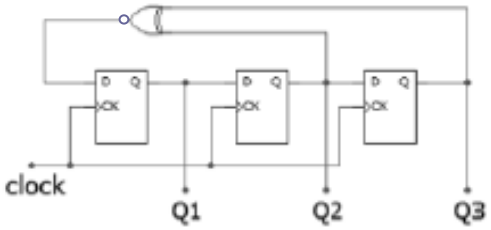

Fig. 3 M-sequence circuit [$G(x)=x^3+x^2+1$]

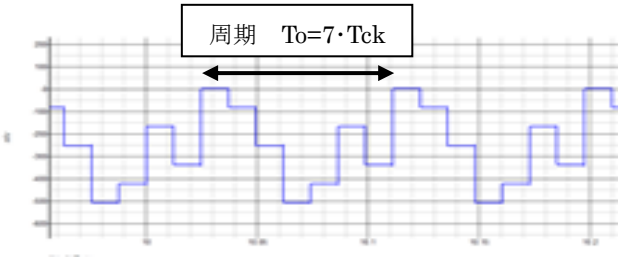

Fig. 4 Output wave form of M-sequence circuit

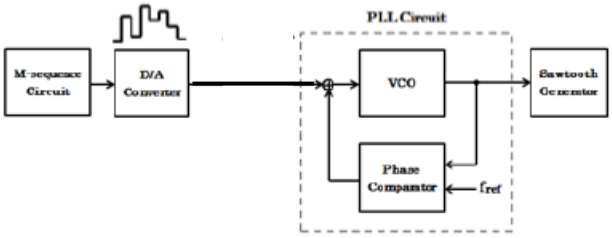

Fig. 5 Block diagram of conventional modulation method

2.3 Conventional digital modulation method

The conventional spread spectrum with the digital modulation needs a lot of digital circuit, which are 10 to 12 bits of shift registers and more than 1,000 signal selectors. Sometimes they make the output voltage ripple larger than the limited level. So the analog random noises made from M-sequence circuit are usually used for spread spectrum method shown in Fig. 5. In Fig.5, the binary signal generated by M-sequence circuit is converted to analog step signal shown in Fig.4. This analog signal is added into the phased-lock loop (PLL) including the voltage controlled oscillator (VCO) with the step noises. In this case, in order to generate many analog levels it needs a large number of digital counters and the results of spectrum spread is in discrete spectrum.

2.4. Proposed Pseudo Analog Modulation Method

Fig.6 shows the block diagram of proposed analog modulation method. In this circuit, low pass filter (LPF) is added in front of the PLL circuit in order

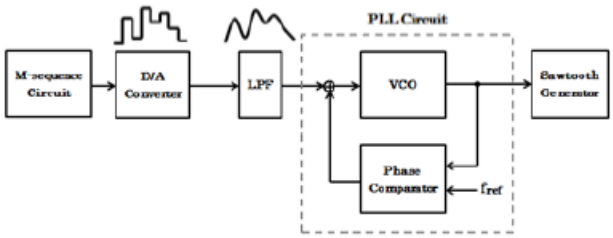

Fig. 6 Proposed analog modulation method with LPF

to convert the step noise to the smoothing analog noise. But the smoothing noise is still cyclic signal. If we observe the signal for just a short period of time, no signal patterns will be found, but if we observe it longer, the similar signal patterns occur repeatedly. In order to add more fluctuation, the noise is inputted into Phase Locked Loop (PLL) circuit. Then, modulated square wave is generated depending on variation of voltage by adding the noise to PLL circuit. The step response of the PLL circuit is dull characteristics of step response shown in Fig. 7 , in which the wave means the variation of the clock frequency. Finally, saw-tooth wave for the switching converter is aperiodically modified by the pseudo analog noise.

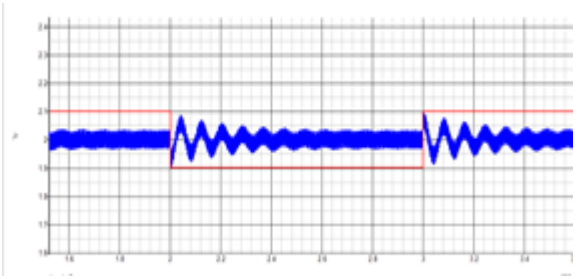

Fig. 7 Step response of PLL circuit

3. Simulation Results

3.1. Simulation Results with Conventional Modulation

The simulation circuit of DC-DC switching buck converter with spread spectrum technology is shown in Fig.2, and Table 1 shows the parameters of switching converter. The frequency or phase of the saw-tooth signal is modified because of the modulation of the clock pulse. Fig. 8 shows the spectrum of the PWM signal in the switching converter without modulation. The peak level of the fundamental clock (200 kHz) is 3.5V with no side-band spectrum and there are high harmonic spectrums at harmonic frequencies. The peak level of 1 MHz which is 5 times of the fundamental frequency is about 700mV.

Table 1 Parameters of Switching Converter

Vin	9.0 V
Vo	5.0 V
Io	0.5 A
L	10uH
Co	470 μ F
Fck	200kHz

Fig. 9 shows the digital modulation with 7 levels shown in Fig. 4 without PLL circuit. The peak level of basic frequency is 3.0V and there are several side-band spectrums. The peak levels of the harmonic frequencies are largely reduced with many side-band spectrums and the peak level of 1 MHz is about 250mV. This simulation is operated by an electronic circuit simulator SIMPLIS.

3.2 Simulation Results with Proposed Analog Modulation

We have proposed the new phase modulation method with analog noise and PLL circuit using 3 bit M-sequence circuit. The pattern levels of the D/A converter are seven and the periodic length is seven clocks (To=7). Fig. 10 shows the spread spectrum using Eq.(1). The peak level of fundamental frequency is 2.0V and there appear many side-band spectrums. The peak level of 1 MHz is about 100mV. The harmonic spectrums are much reduced with no line spectrum. In this case, the output voltage ripple of the switching converter is shown in Fig. 10 and its level is about 7 mVpp.

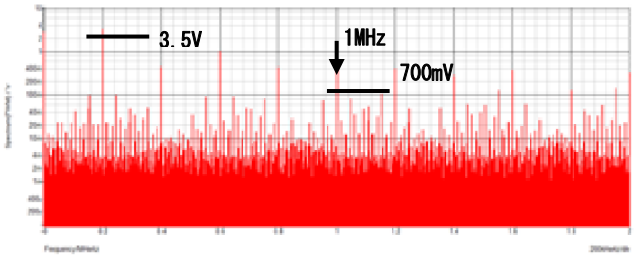

Fig.8 Spectrum without spread modulation

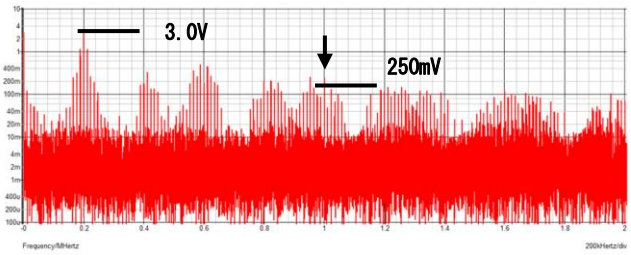

Fig.9 Spectrum with digital modulation (T=7)

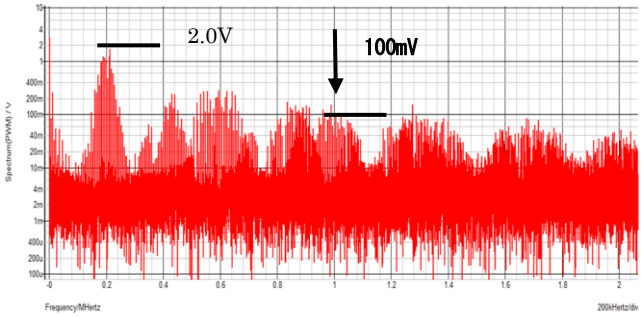

Fig.10 Spectrum with analog modulation (T=To)

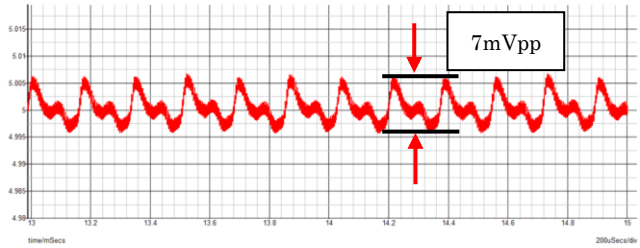

Fig.11 Output Ripple of Switching Converter (T=To)

4. New Analog Pattern Generators with Bit Operation

4.1 Expansion of analog pattern length with bit exchange

We have investigated new analog noise generator with bit exchange witch are generated from M-sequence circuit. The longer the pattern length of the analog noise is, the lower the peak level of the fundamental frequency is and the wider the side-band spectrums of the harmonic frequencies spread. The three bits make 8 analog levels and the number of permutations of pattern level makes ${}_7P_7$=7･6･5･4･3･2･1= 5,040 when the start level is set to 0. In the equation (1) or (2), there is only one or two pattern. Reversing some of the bits from M-sequence circuit makes the new pattern levels.

Equations (3)~(10) show the result of the bit reversed level streams of equation (1). In these results, there is no same stream and we can understand that using theses streams in the analog noise cycle makes the analog noise period longer with 8 times of equation (1) and the pattern length makes 56 patterns a period (T=8To).

0) $Q_1Q_2Q_3$: 0 - 1 - 3 - 6 - 5 - 2 - 4 - (3)

1) $\overline{Q_1}Q_2Q_3$: 1 - 0 - 2 - 7 - 4 - 3 - 5 - (4)

2) $Q_1\overline{Q_2}Q_3$: 2 - 3 - 1 - 4 - 7 - 0 - 6 - (5)

3) $\overline{Q_1}\overline{Q_2}Q_3$: 3 - 2 - 0 - 5 - 6 - 1 - 7 - (6)

4) $Q_1Q_2\overline{Q_3}$: 4 - 5 - 7 - 2 - 1 - 6 - 0 - (7)

5) $\overline{Q_1}Q_2\overline{Q_3}$: 5 - 4 - 6 - 3 - 0 - 7 - 1 - (8)

6) $Q_1\overline{Q_2}Q_3$: 6 - 7 - 5 - 0 - 3 - 4 - 2 - (9)

7) $\overline{Q_1}\overline{Q_2}\overline{Q_3}$: 7 - 6 - 4 - 1 - 2 - 5 - 3 - (10)

4.2 Circuit of New Bit Generator with bit inverse

Fig.12 shows the simulation block diagram of the new M-sequence circuit with bit inverse. Bits inverses are operated at the exclusive-ORs which are controlled the 3 bits counter of the period of the M-sequence circuit. Then at the output of the DAC appears the analog noise of 56 patterns a period (T=8To). Fig.13 shows the bit pattern generated from the circuit of Fig. 12.

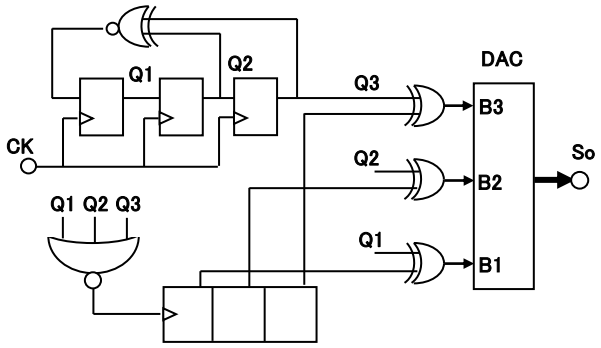

Fig. 12 New Generator with bit inverse

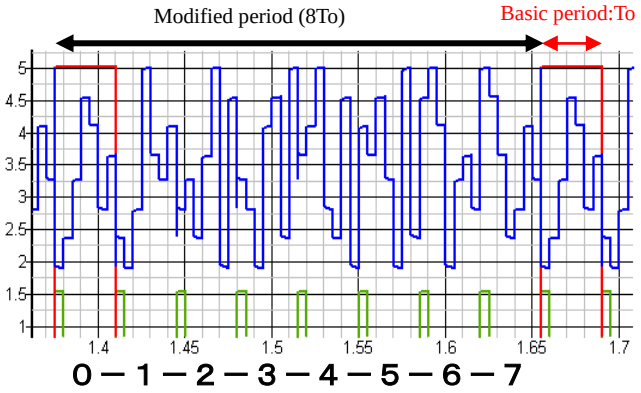

Fig. 13 Output of New Generator with bit inverse

4.3 New Analog Pattern Generators with bit exchange

In order to make the period of the analog noise much longer, we have utilized the bit exchange shown below. In this case, there is no same bit stream and they make the pattern length of the analog noise 6 times of above. Then the pattern length makes 6･8･To=336 patterns a period (T=48To).

0) $Q_1Q_2Q_3$:	0 - 1 - 3 - 6 - 5 - 2 - 4 -	(3)
A) $Q_1Q_3Q_2$:	0 - 1 - 5 - 6 - 3 - 4 - 2 -	(11)
B) $Q_2Q_1Q_3$:	0 - 2 - 3 - 5 - 6 - 1 - 4 -	(12)
C) $Q_2Q_3Q_1$:	0 - 4 - 5 - 3 - 6 - 1 - 2 -	(13)
D) $Q_3Q_1Q_2$:	0 - 2 - 6 - 5 - 3 - 4 - 1 -	(14)
E) $Q_3Q_2Q_1$:	0 - 4 - 6 - 3 - 5 - 2 - 1 -	(15)

4.4 Circuit of New Bit Generator with bit exchange

Fig.14 shows the simulation block diagram of the new M-sequence circuit with bit exchange. Bits exchanges are operated in the matrix block sequentially. Then at the output of the DAC, there appear the analog steps of 6 times of the input pattern steps. Fig. 15 shows the bit pattern generated from the circuit of Fig. 14.

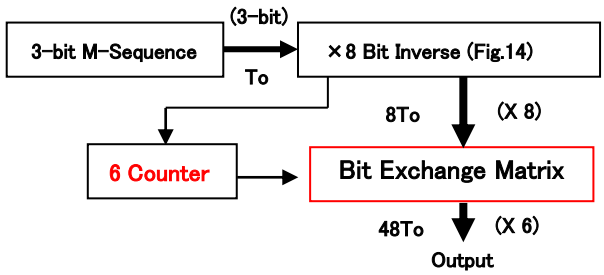

Fig. 14 New Generator with bit exchange

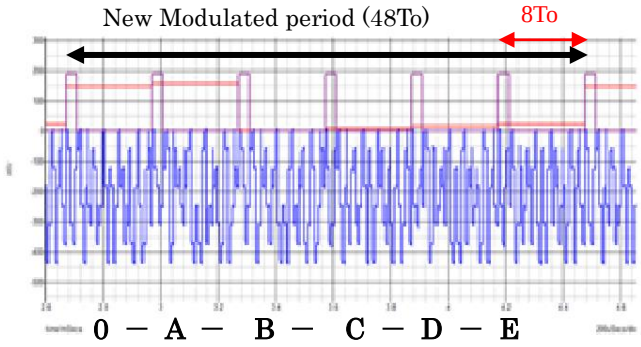

Fig. 15 Output of New Generator with Bit Inverse and Echange

5. Simulation Results with New Pattern Generator

Fig. 16 shows the simulation results of the spread spectrum using new analog noise generator with bit inverse and its pattern length is T=8To=56 pattern length. The peak level of fundamental frequency is 2.0V and there is no line spectrum. The peak level of 1MHz is about 50mV.

Fig. 17 shows the spread spectrum using new analog noise generator with bit inverse and exchange. Its pattern length is T=6･8To=48To=336 pattern length a period. The peak level of fundamental frequency is down to 0.5V and the harmonic spectrums are much more reduced.

Fig. 18 shows the output ripples of the switching converter using the pattern of T=48To. The ripple is about 11mVpp. The period of the ripple is about 4.15 ms (T=48･7Tck). Fig.19 shows the PWM pulses in the switching converter. The density of the PWM pulses is proportional to the analog noise from the new bit generator.

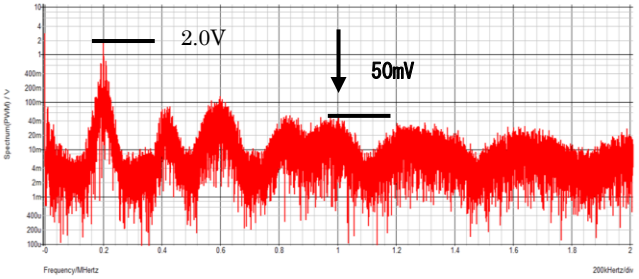

Fig.16 Spread Spectrum using New Analog Modulation with Bit Inverse (T=8To)

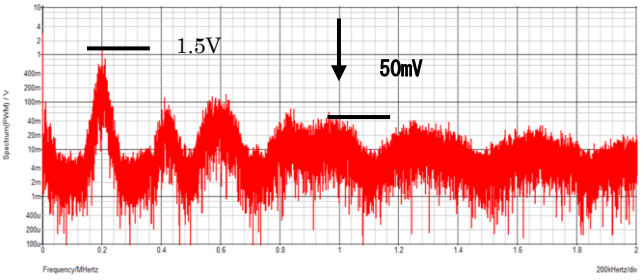

Fig.17 Spread Spectrum using New Analog Modulation with Bit Inverse and Exchange (T=48To)

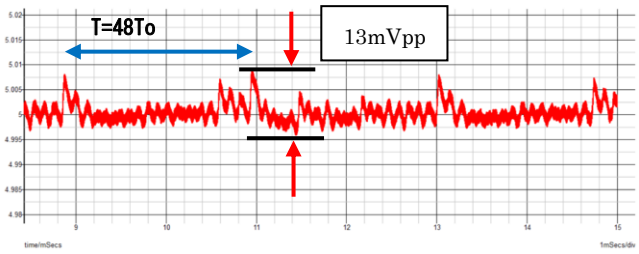

Fig.18 Output Ripple of Switching Converter (T=48To)

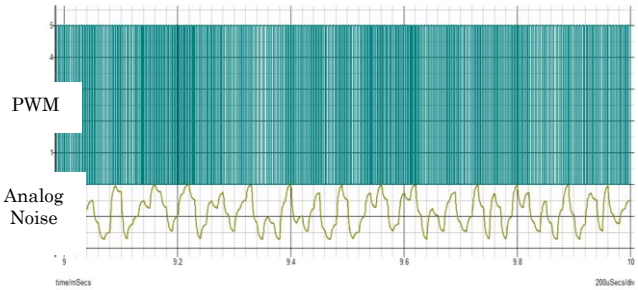

Fig. 19 PWM Pulses in Switching Converter (T=48To)

6. Conclusion

This paper proposes new EMI reduction method by extended spread spectrum using the PLL circuit with pseudo analog noise which is produced from new M-sequence circuit. The PLL circuit makes the reference clock modified with non-periodic analog noise which is supplied from new 3-bit M-sequence circuit. New pseudo analog noise is produced by inversing and/or exchanging the 3-bit. Using this modified clock from the PLL circuit for the saw-tooth signal in the switching converter, the spectrum of the PWM pulses is widely spread and the peak levels of the spectrums of the fundamental frequency (200 kHz) and the harmonic frequencies are much reduced. The peak spectrum level of 200 kHz is reduced by 2.ov and that of 1 MHz is reduced by 650mV which is about 16dB down compared with non-modified spread.

References

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