Proposal of High Reliability LDMOS Structure

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Abstract

This paper proposes 0.35-micron process dual RESURF Nch-LDMOS to enhance reliability for 30-50V application for automotive usage. The LDMOS adequately suppresses drain current expansion caused by Kirk effect(1), and generates pn junction breakdown in the bulk under the drain, leading to good ESD performance.

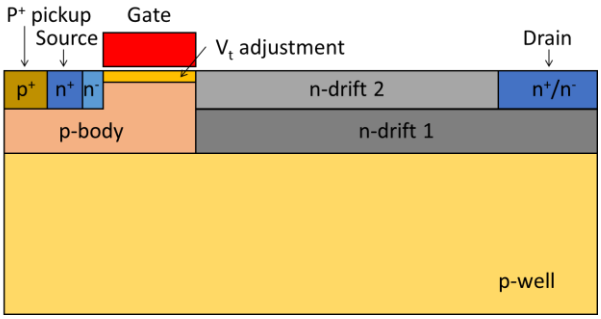
Introduction

Lateral Double-diffused MOSFET (LDMOS) for automotive applications requires much higher reliability and wide Safe Operating Area (SOA). However the conventional LDMOS has an issue of Current Expansion(CE) (2)(3) which limits reliability and SOA; this CE phenomenon is current increase at high VDS/VGS operation. We propose here a new LDMOS structure to suppress this phenomenon, and verify its operation and characterisitics with TCAD simulation.

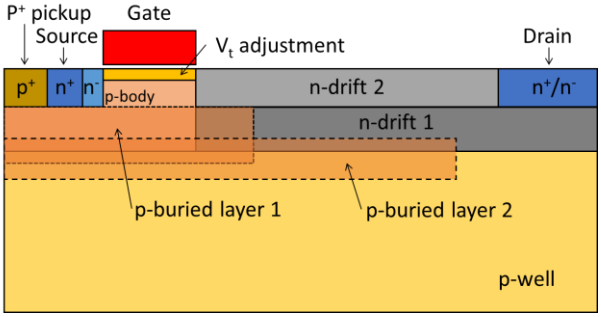
TCAD Simulation

In order to provide high reliability for LDMOS, we have carried out two attempts. First one is to suppress the generation of electron-hole pairs due to impact ionization in a drift region around the drain-side gate edge of the intrinsic MOSFET of an LDMOS, and also to suppress the drain current increase due to Kirk effect. Second one is to generate pn junction breakdown in the bulk under the drain of an LDMOS in order to prevent gate oxide failure on Electro Static Discharge(ESD).

Fig. 1 shows impurity doped regions for conventional and new N-ch LDMOSs. New Nch-LDMOS has dual p-buried layers; p-buried 1 contributes to reduced surface field (RESURF) at the drift edge, p-buried 2 to that

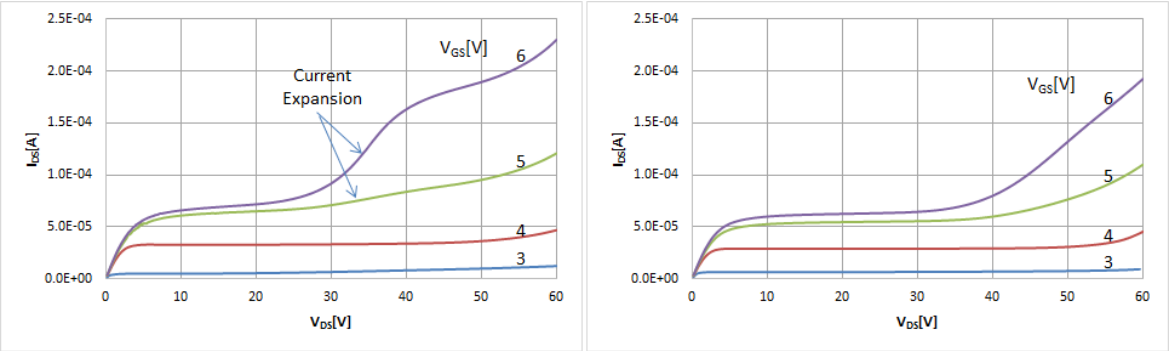


(a) Conventional LDMOS



(b) Proposed LDMOS

Fig. 1. Structures of conventional and proposed LDMOSs.



(a) Conventional LDMOS (b) New LDMOS

Fig. 2. TCAD simulation results of I_{DS}-V_{DS} characteristics for conventional and new LDMOS.

for the total drift region.

Results and Discussion

Fig. 2 shows simulated I_{DS}-V_{DS} characteristics of conventional and new LDMOSs. Fig. 2 (a) states that at V_{GS} = 5V, the conventional LDMOS starts to generate weak CE around V_{DS} = 30V, and at V_{GS} = 6V, significant CE. Also Fig. 2(b) shows that the proposed LDMOS has current increase at V_{GS} = 5 and 6V and around V_{DS} = 40V, but CE does not occur.

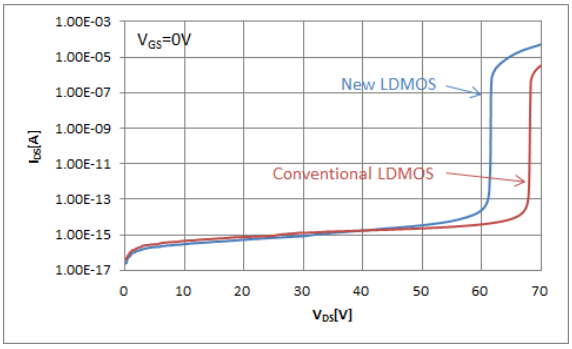


Fig. 3. TCAD simulation results of I_{DS}-V_{DS} characteristics at breakdown for conventional and proposed LDMOSs.

Next, we show I_{DS}-V_{DS} breakdown characteristics of conventional and proposed LDMOSs in Fig.3. Breakdown voltage of the conventional is 68V, while that of the proposed, 61V. The breakdown voltage of the proposed is lower than that of the conventional. However, since we intend to use V_{DS} below 50V for its operation, this is not a problem. Breakdown locations both of the conventional and proposed LDMOSs are in the bulk under the drain, so the proposed LDMOS leads to good ESD performance same as the conventional one.

Also we see that on-resistance is 68.7mΩmm^2 in the conventional and 69.3mΩmm^2 in the proposed; they are comparable values.

Conclusion

We have proposed a new LDMOS structure which does not have current expansion, leading to good reliability and wide SOA suitable for automotive applications. These are realized by forming dual p-buried layers for the drift layer and generating pn junction breakdown in the bulk under the drain. Our TCAD simulation has shown that the proposed LDMOS can stably operate at V_{DS} = 40V and V_{GS} = 5V.

We would like to thank AdvanceSoft Corporation for providing us their TCAD simulator with

which TCAD simulation results here were obtained.

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