P8-22

Proposal of High Reliability LDMOS Structure

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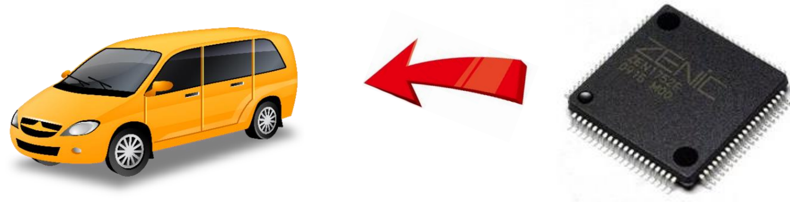
Introduction

Research Background & Objective

LDMOS･･･Laterally Diffused MOS

Used as high-voltage switching



Adopting to automotive applications

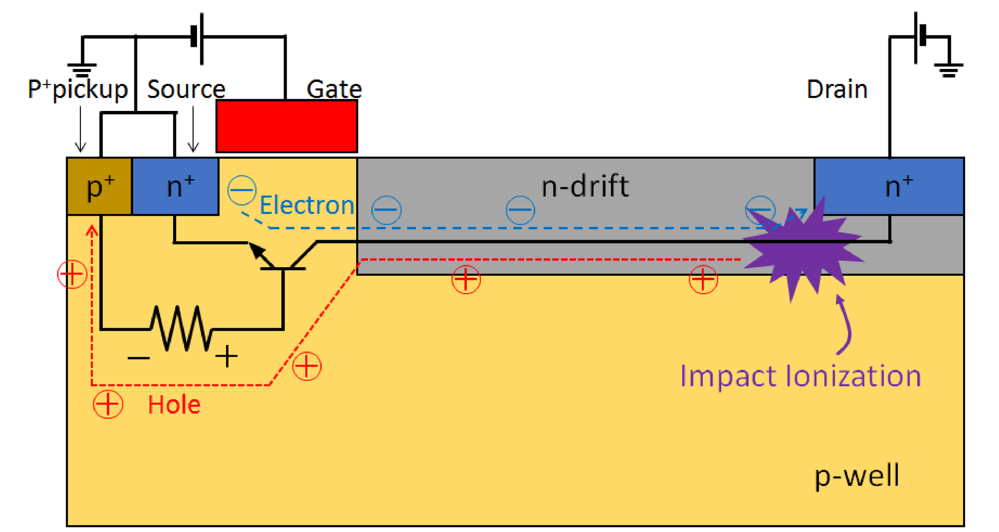
If it were not highly reliable …...?

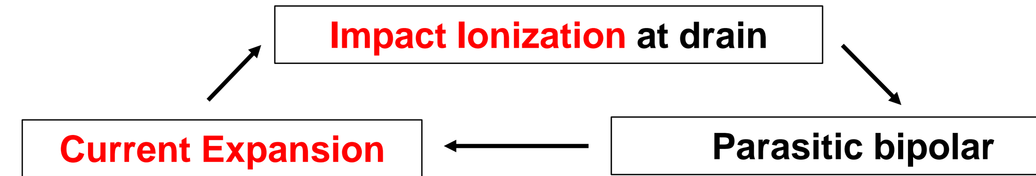
Accident !!!

High reliability realization

- Reinforcement of Hot Carrier Endurance
  - ✓Suppression of impact ionization around drain edge of intrinsic MOSFET of LDMOS
  - ✓Suppression of Current Expansion (Kirk effect)
- Reinforcement of ESD Endurance
  - ✓Generation of Bulk Breakdown (pn junction breakdown location is in bulk.)

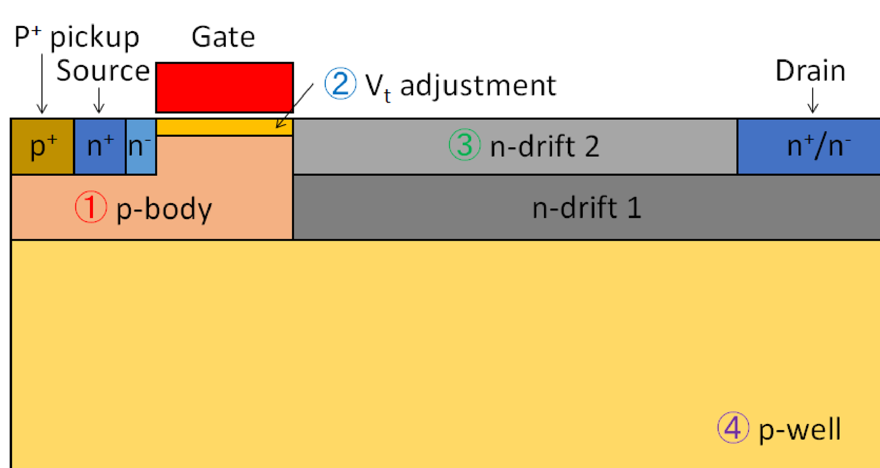
Impact Ionization & Current Expansion

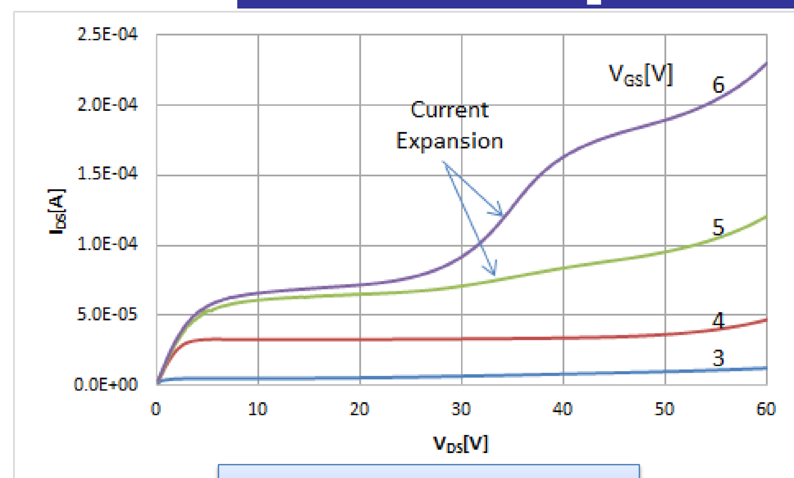




Proposed Structure

Conventional LDMOS





I_{DS}-V_{DS} Characteristics

$R_{on}A$=68.7 mΩmm²

Purpose of Doping

To suppress Current Expansion

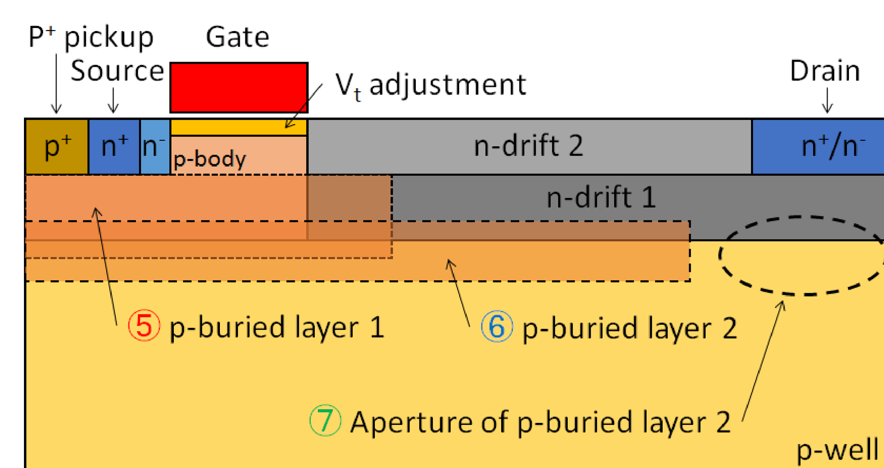
⇒ ① Highly doped p-body ② V_T adjustment ③ n-drift 2

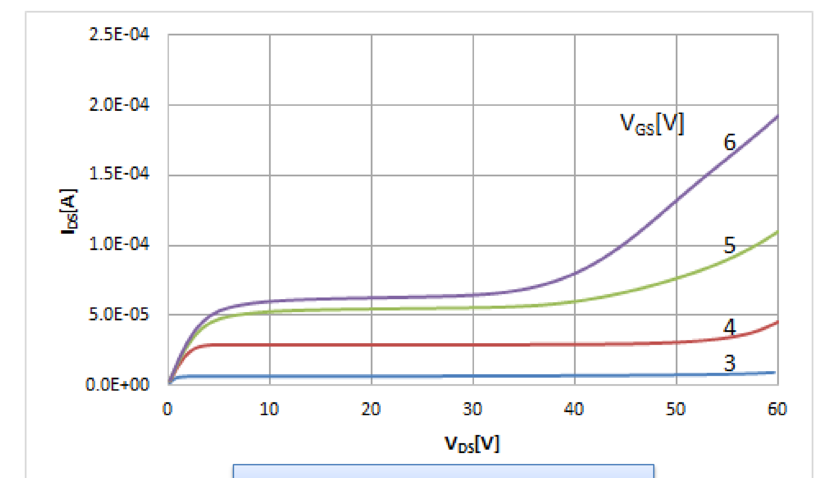
RESURF

⇒ ① Highly doped p-body around drift edge ④ p-well along drift region

Low RonA ⇒ ③ n-drift 2

New LDMOS





I_{DS}-V_{DS} Characteristics

$R_{on}A$=69.3 mΩmm²

Purpose of Doping

To suppress Current Expansion

⇒ ⑤ p-buried layer 1

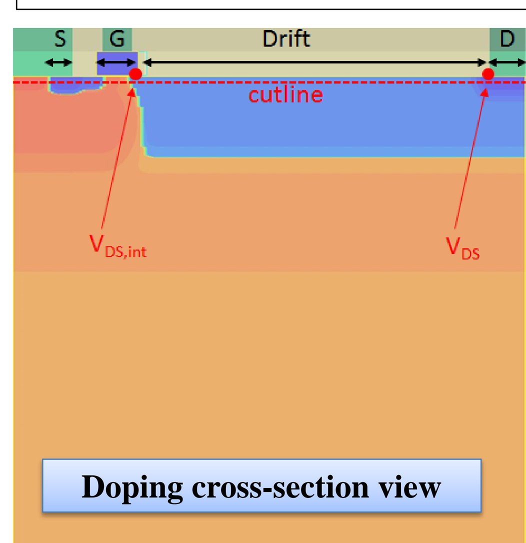
⑦ Aperture of p-buried layer 2 under n+ drain region

Reinforcement of RESURF

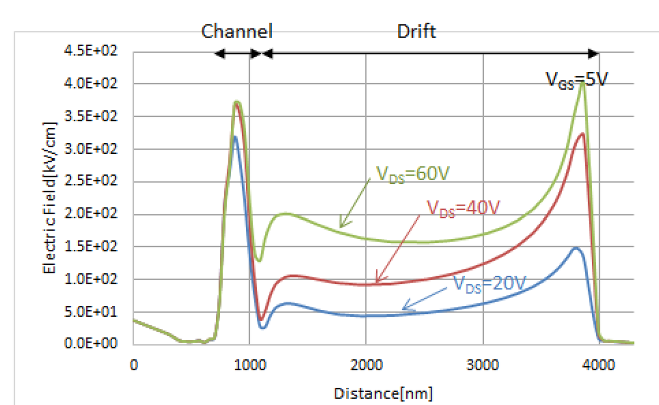
⇒ ⑤ p-buried layer 1 around drift edge ⑥ p-buried layer 2 along drift region

Comparison of Conventional & New

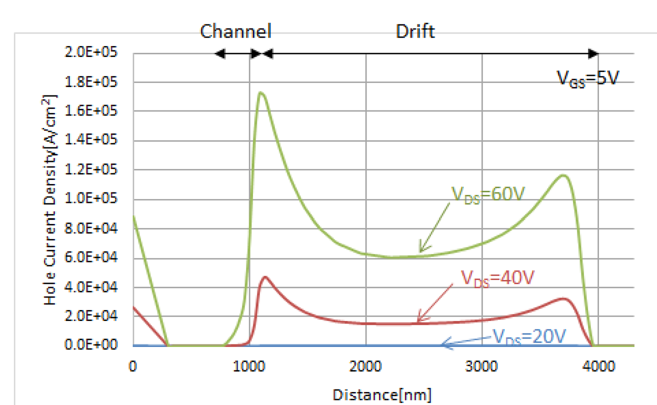
Conventional LDMOS



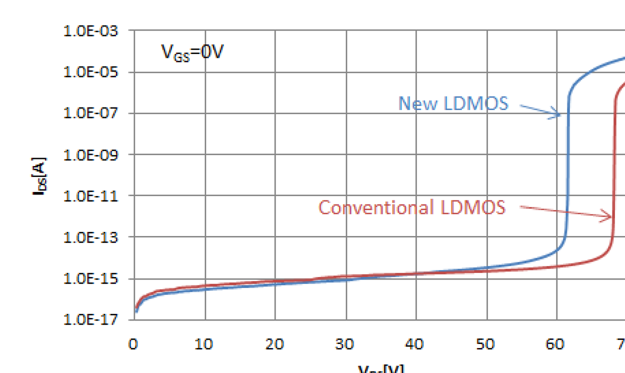
Doping cross-section view



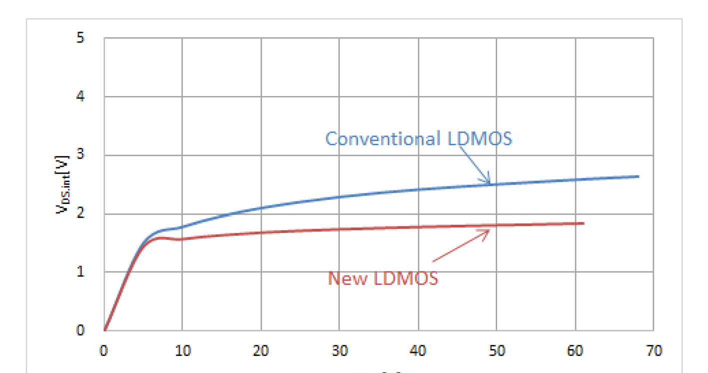
Electric Field Profile



Hole Current Density Profile



Breakdown Characteristics



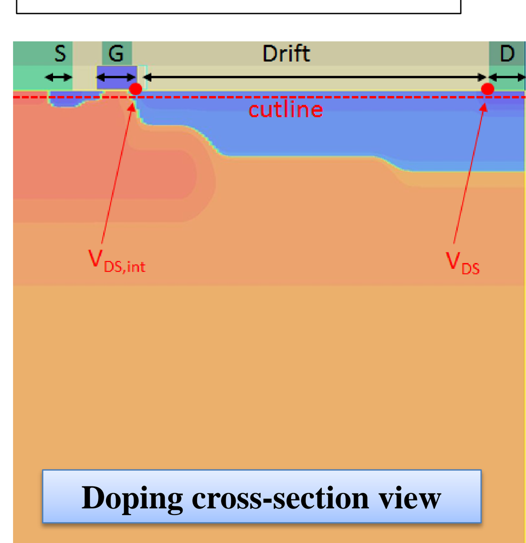
$V_{DS,int}$-V_{DS} Characteristics

･Peak reduction at drift region

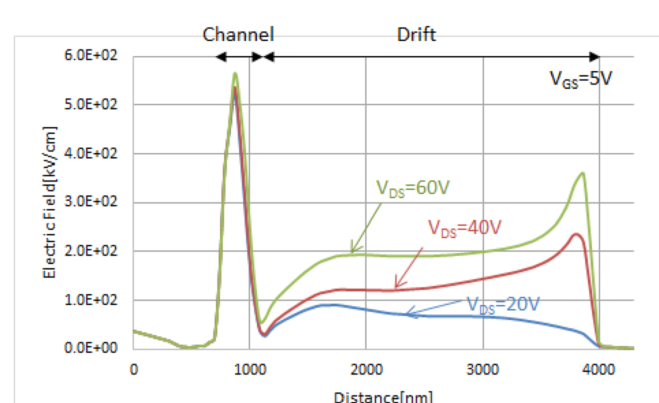
･No peak at channel side of drift region

･Flat characteristic and small value

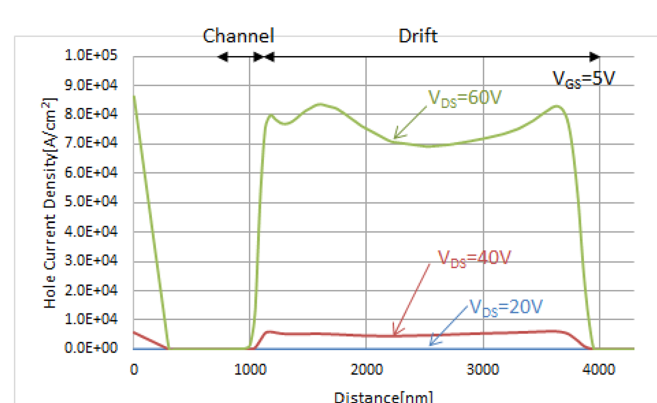
New LDMOS



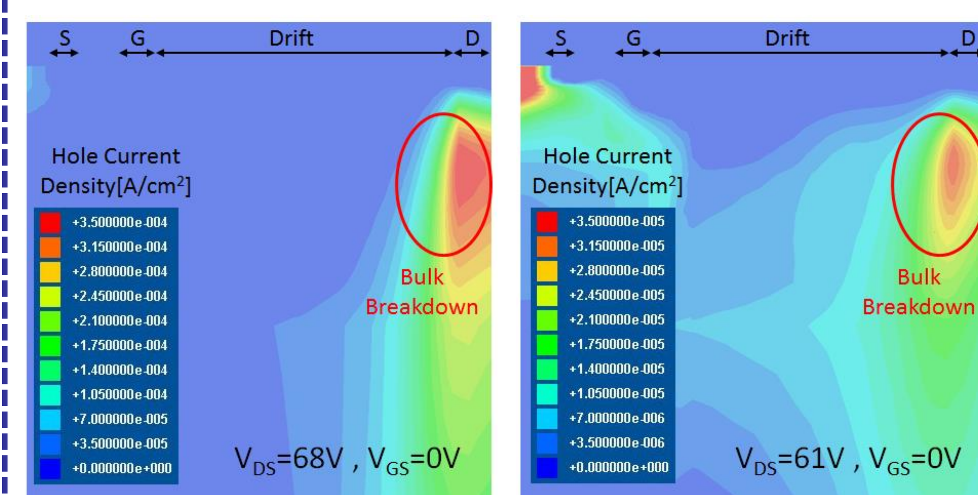
Doping cross-section view



Electric Field Profile



Hole Current Density Profile



Conventional LDMOS structure Location of Breakdown

New LDMOS structure Location of Breakdown

At breakdown

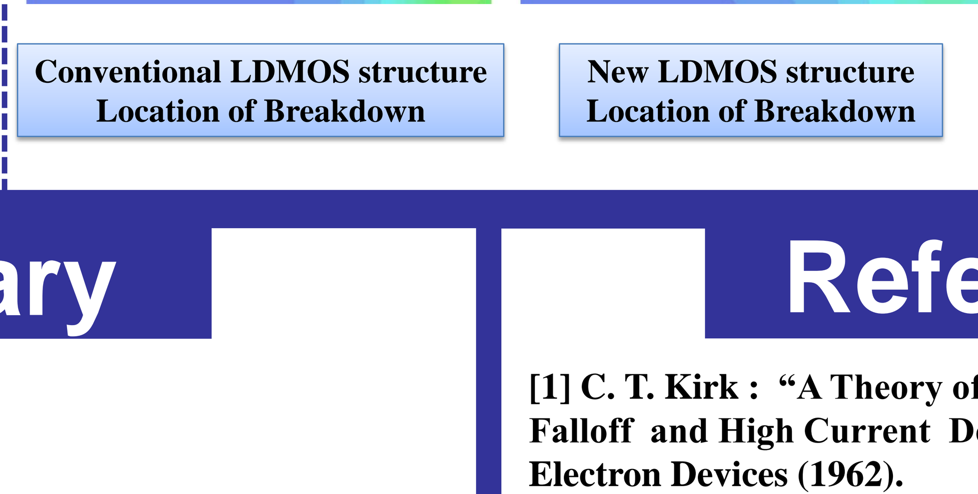
Conventional LDMOS･･･

$V_{DS,int}$ = 2.64V at BV_{DS} = 68V

New LDMOS･･･

$V_{DS,int}$ = 1.84V at BV_{DS} = 61V

High Reliability!!!



Result

Items	Conventional LDMOS	New LDMOS
Hole current density around drain side gate edge of intrinsic MOSFET	High	Low
Magnitude of electric field in drift region around drain edge of intrinsic MOSFET	High	Low
Location of pn junction breakdown	Bulk	Bulk
Current increase	Strong (current expansion) (Generation for V_{DS}>25V and V_{GS}≧5V)	Weak (Generation for V_{DS}>40V and V_{GS}≧5V)
$V_{DS,int}$ (V) at BV_{DS}	2.64	1.84
BV_{DS}(V)	68	61
RonA (mΩ mm²)	68.7	69.3
V_T(V) at I_{DS}=1×10⁻⁸ A	2.4	2.1

Summary

Conclusion

- Proposed a new LDMOS structure for automotive applications.
- Realized by forming dual p-buried layers.
- Leading to high reliability and wide SOA.

Challenge for the future

- Reducing the on-resistance
- 3D Simulation, collaborating with Toronto University, Canada

References

[1] C. T. Kirk : "A Theory of Transistor Cutoff Frequency (ft) Falloff and High Current Densities", IRE Transactions on Electron Devices (1962).

[2] C.-C. Cheng, et. al. : "Investigation of Parasitic BJT Turn-on Enhanced Two-stage Drain Saturation Current in High-voltage NLDMOS", 23rd International Symposium on International Power Semiconductor Devices & IC's (2011).

[3] J. Chen : "HV EDMOS Design with Expansion Regime Suppression", Master Thesis of Applied Science, Department of Electrical and Computer Engineering, University of Toronto (2013).

AdvanceSoft Corporation is acknowledged for providing TCAD simulator.