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Fibonacci Sequence Weighted SAR ADC Algorithm and its DAC Topology

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Outline

- Objective
- SAR ADC Redundancy Design
- Proposed SAR Algorithm Using Fibonacci Sequence
  - Error Correction Range
  - Settling Time
- Realization of Fibonacci DAC
- Conclusion

Outline

- **Objective**
- SAR ADC Redundancy Design
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Research Objective

Objective

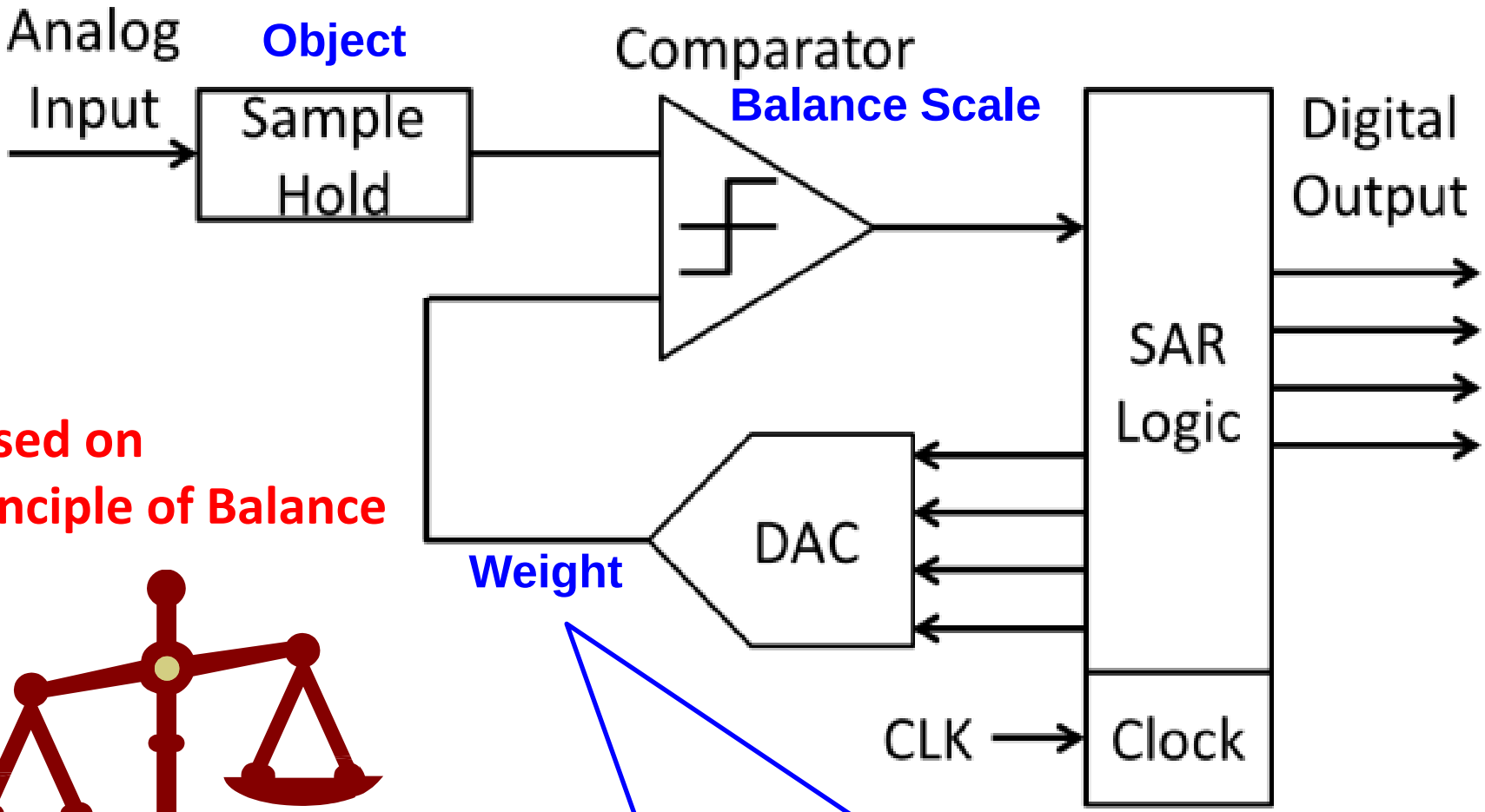
- **Development of**
  Reliable & High-speed SAR ADC

Our Approach

- **Redundancy search algorithm design with Number Theory**

SAR ADC : Successive Approximation Register ADC

SAR ADC Configuration



Based on Principle of Balance

Generally use binary weight

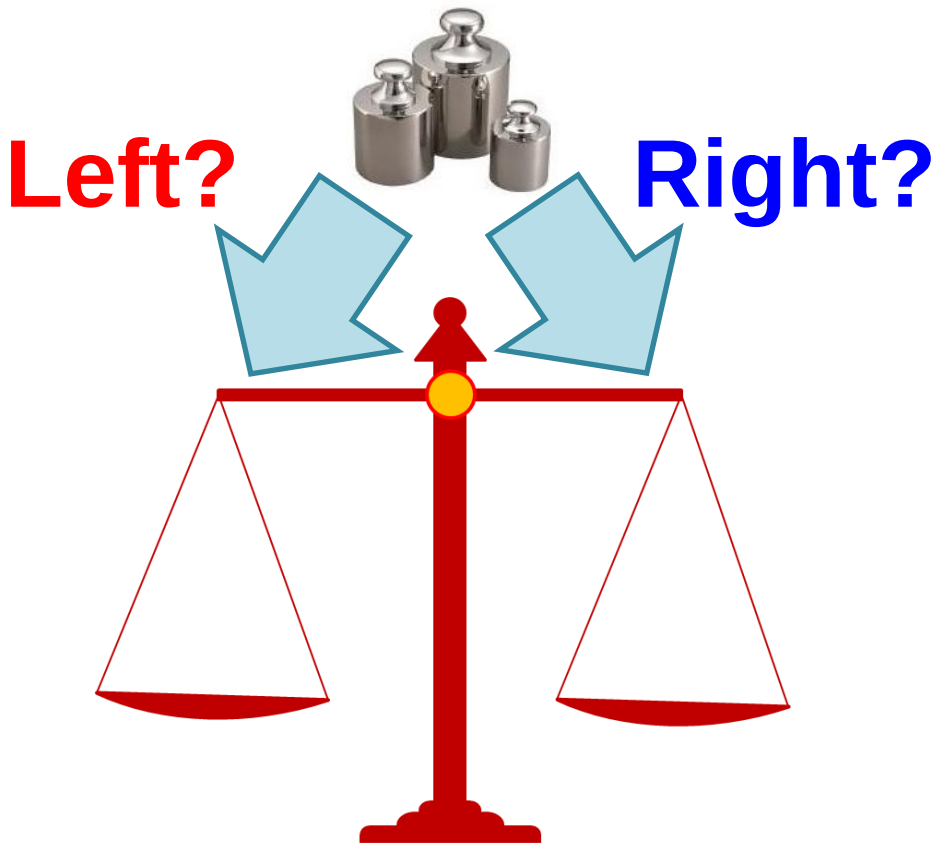
(1 , 2 , 4 , 8 , 16 , 32, 64 …)

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input : 7.3 [V]
- Binary weight :

16, 8, 4, 2, 1



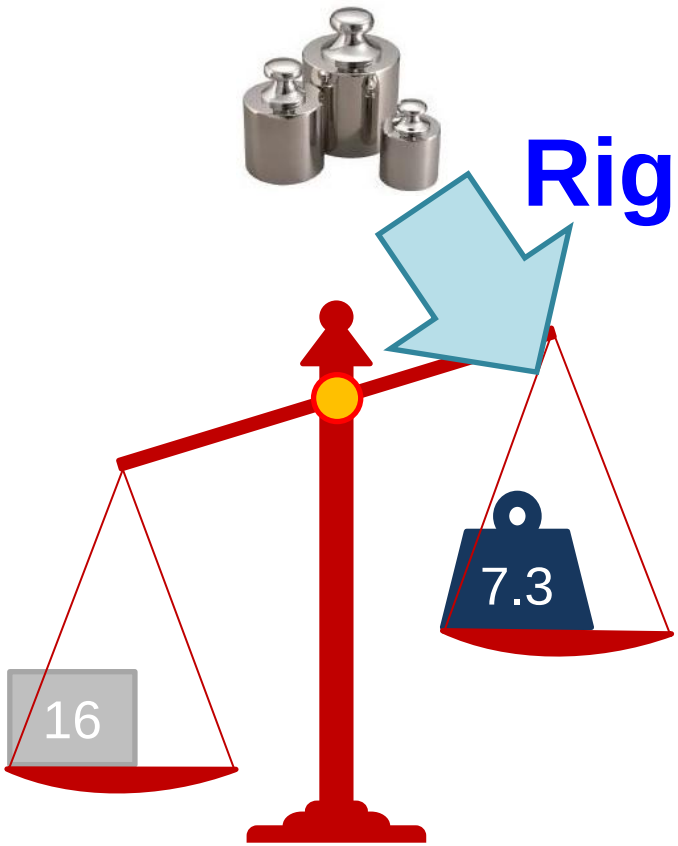
Step		1st	2nd	3rd	4th	5th	output
Weight p(k)		16	8	4	2	1	
Level	31						31
	30						30
	29						29
	28						28
	27						27
	26						26
	25						25
	24						24
	23						23
	22						22
	21						21
	20						20
	19						19
	18						18
	17						17
	16						16
	15						15
	14						14
	13						13
	12						12
	11						11
	10						10
	9						9
	8						8
	7						7
	6						6
	5						5
	4						4
	3						3
	2						2
	1						1
	0						0

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input : [V]
- Binary weight :

8, 4, 2, 1



Step		1st	2nd	3rd	4th	5th	output
Weight p(k)		16	8	4	2	1	
Level	31						31
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	24						24
	23						23
	22						22
	21						21
	20						20
	19						19
	18						18
	17						17
	16						16
	15						15
	14						14
	13						13
	12						12
	11						11
	10						10
	9						9
	8						8
	7						7
	6						6
	5						5
	4						4
	3						3
	2						2
	1						1
	0						0

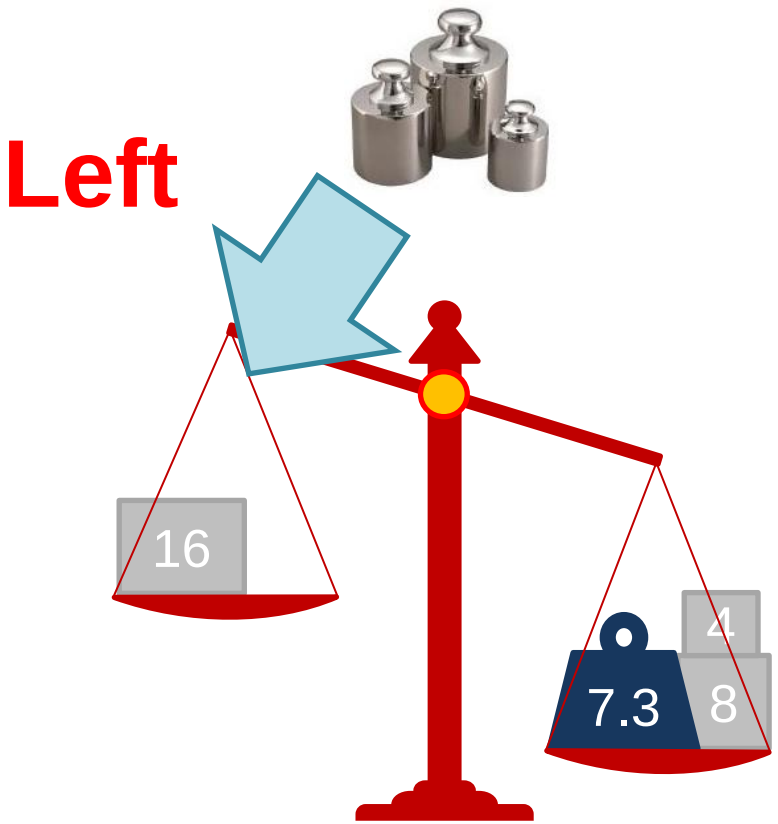
Down!

0

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input : [V]
- Binary weight : 2, 1



Step		1st	2nd	3rd	4th	5th	output
Weight p(k)		16	8	4	2	1	
Level	31						31
	30						30
	29						29
	28						28
	27						27
	26						26
	25						25
	24						24
	23						23
	22						22
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	19						19
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	16						16
	15						15
	14						14
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	12						12
	11						11
	10						10
	9						9
	8						8
	7						7
	6						6
	5						5
	4						4
	3						3
	2						2
	1						1
	0						0

UP!

0 0 1

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input : [V]
- Binary weight :

$$7.3 \Rightarrow 00111 \Rightarrow 7$$

$$16 - 8 - 4 + 2 + 1 + 0.5 - 0.5 = 7$$

Step	1st	2nd	3rd	4th	5th	output
Weight p(k)	16	8	4	2	1	
Level 31						31
30						30
29						29
28						28
27						27
26						26
25						25
24						24
23						23
22						22
21						21
20						20
19						19
18						18
17						17
16						16
15						15
14						14
13						13
12						12
11						11
10						10
9						9
8						8
7						7
6						6
5						5
4						4
3	0	0	1	1	1	3
2						2
1						1
0						0

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SAR ADC Redundancy Design

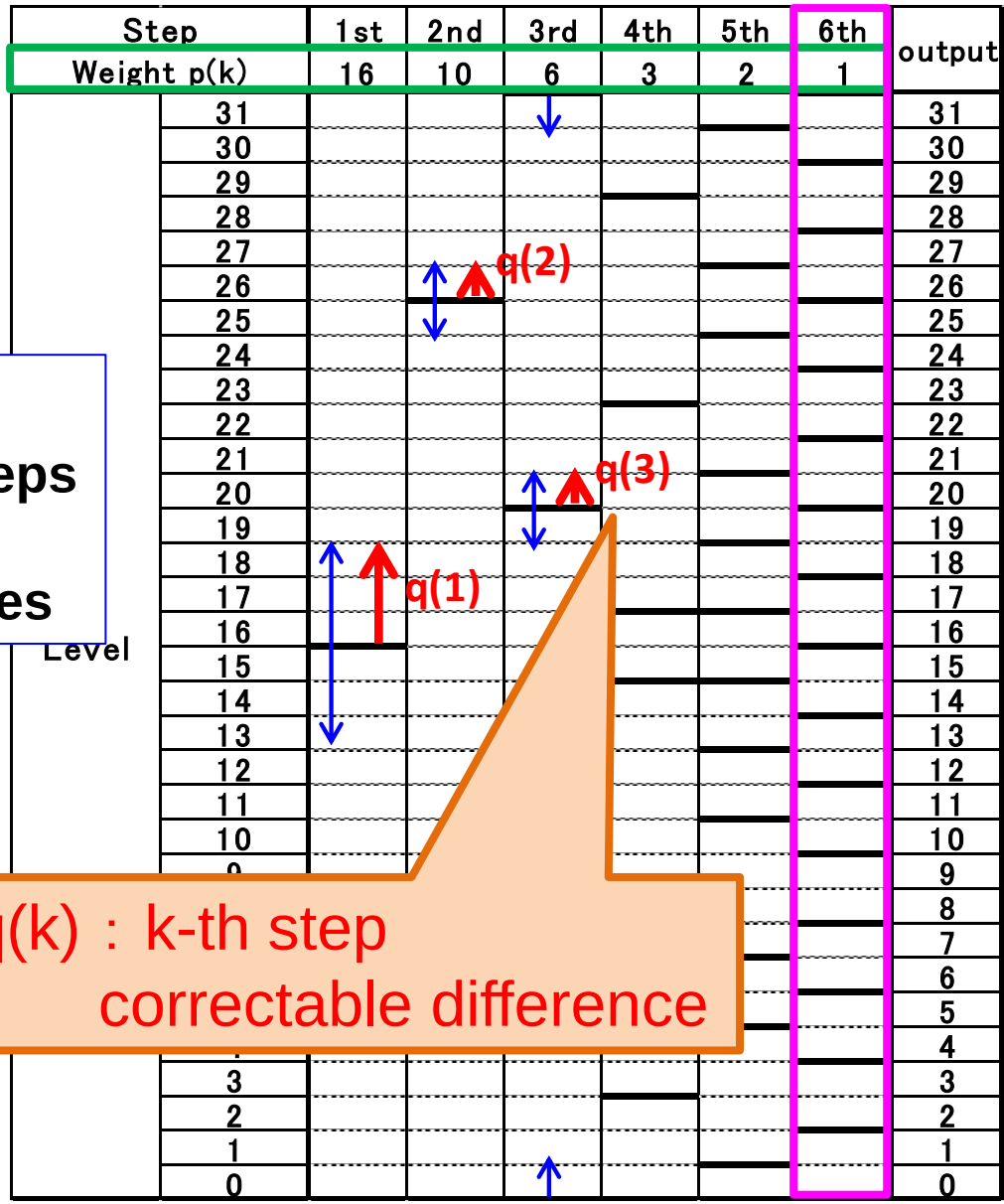
Redundancy

- Surplus, Extra

Using time redundancy

- Increase Extra comparison steps
- Change reference to Non-binary voltages

Enable digital error correction!



Redundancy Design Operation(No Error)

4bit-5step SAR ADC

- Analog input : 6.3
- Redundant weight :

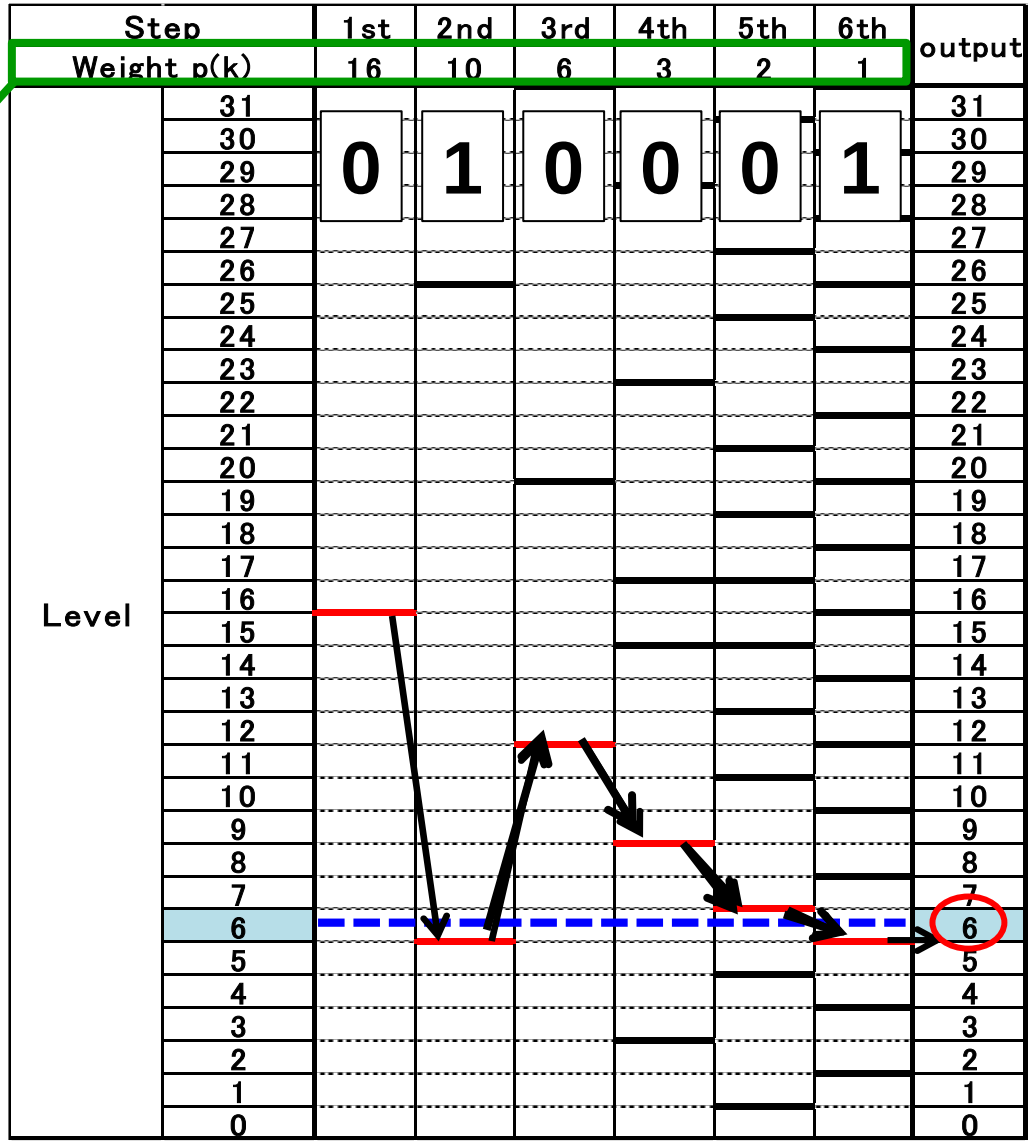
  16, 10, 6, 3, 2, 1

Correctable expression

6.3⇒010001⇒6

$$16 - 10 + 6 - 3 - 2 - 1 + 0.5 - 0.5$$

=6



Redundancy Design Operation(One Error)

4bit-5step SAR ADC

- Analog input : 6.3
- Redundant weight :
  16, 10, 6, 3, 2, 1

Correctable expression

6.3⇒010001⇒6

Another expression

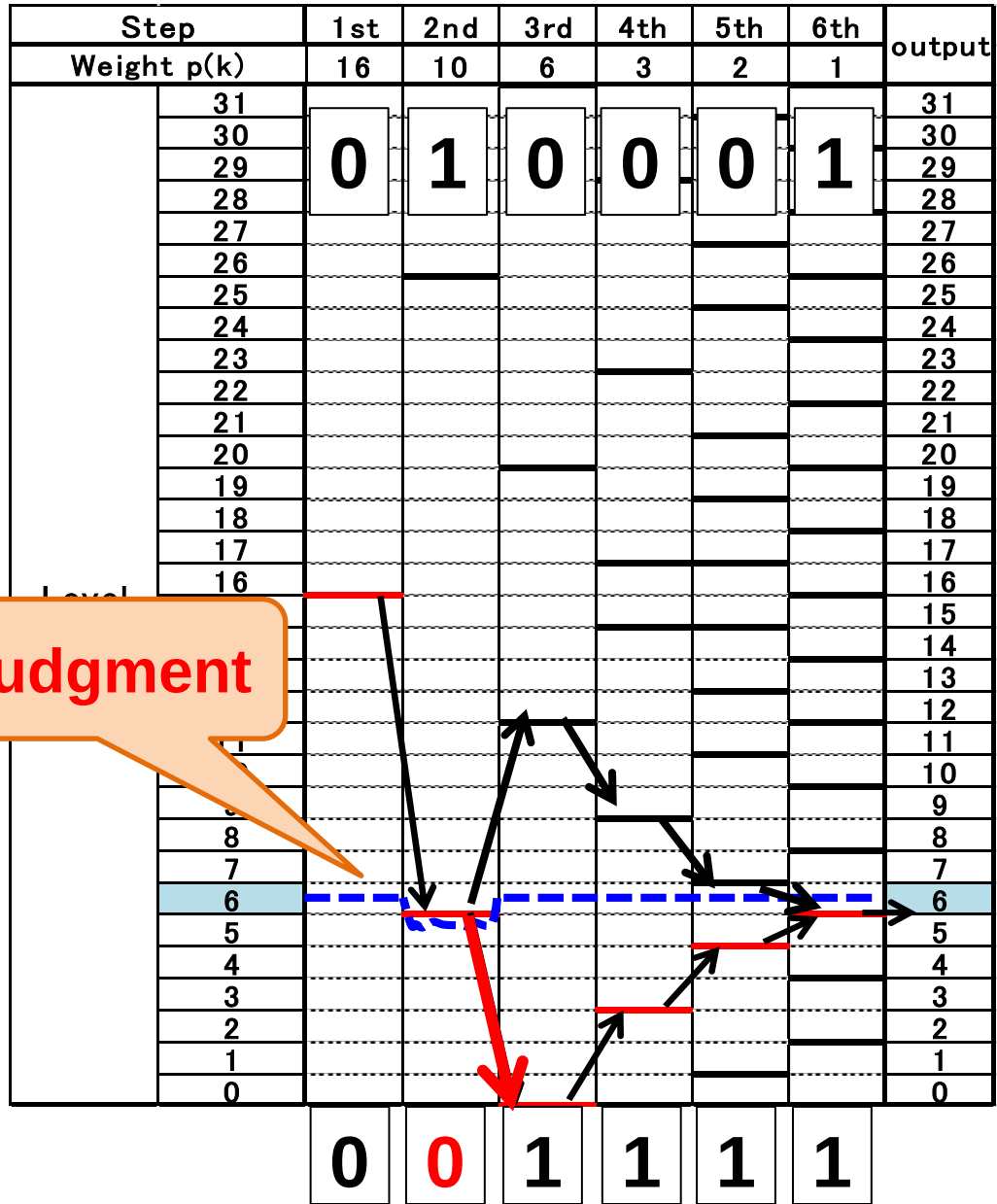
6.3⇒001111⇒6

$16 - 10 - 6 + 3 + 2 + 1 + 0.5 - 0.5$

$= 6$

Error correction

High-Reliability



Issues of Conventional Method

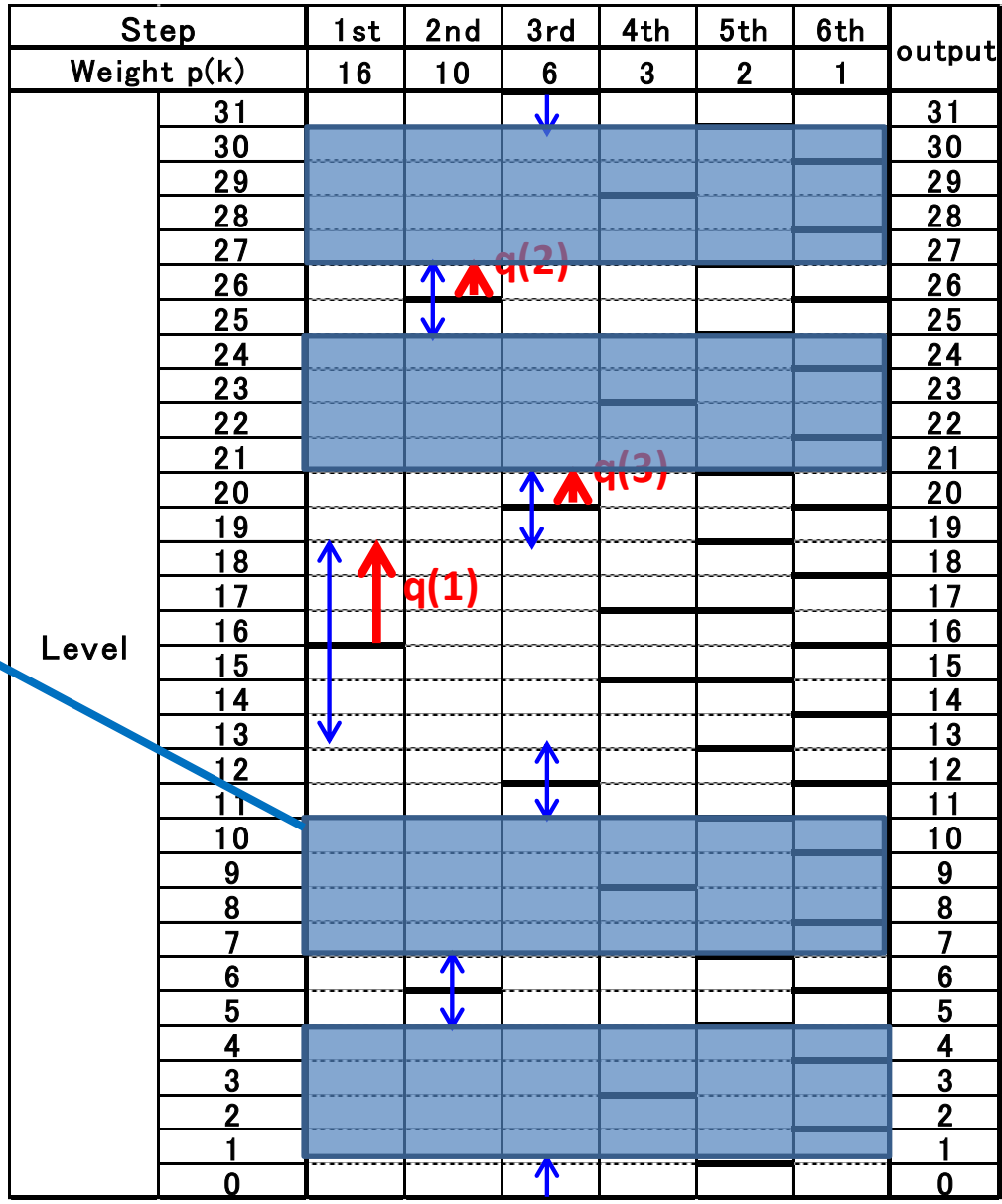
Selection Reference Voltages

1. ***Difficult to select good reference voltages***
2. ***q(k) must be fraction***

Uncorrectable Range

Not effective redundancy design

Good selection method is needed !



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Fibonacci Sequence

Fibonacci Definition

$$F_0 = 0$$
$$F_1 = 1$$
$$F_{n+2} = F_n + F_{n+1} \qquad \text{(n=0,1,2…)}$$

Example of Fibonacci number

$$0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55 \ldots$$

Leonardo Fibonacci
(Italy:1170-1250)

Property

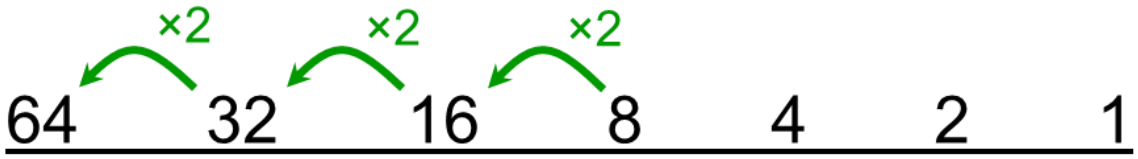
The closest terms ratio : ***"Golden Ratio"***

(about 1.62 number)

$$\lim_{n\to\infty} \frac{F_n}{F_{n-1}} = 1.618033988749895$$

Use of Fibonacci Sequence

Use of **Binary**

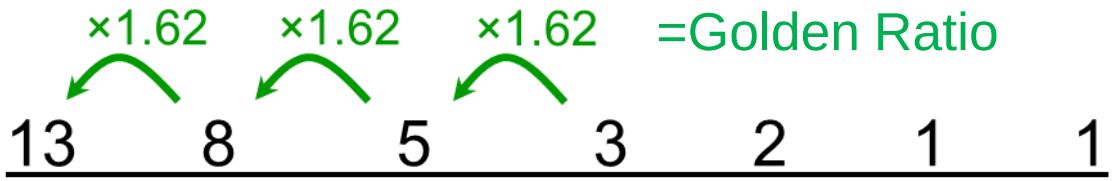


Binary Weighted (Radix=2)

Radix：Decision weighted number

Change weighted

Use of **Fibonacci**



Fibonacci Weighted (Radix=1.62)

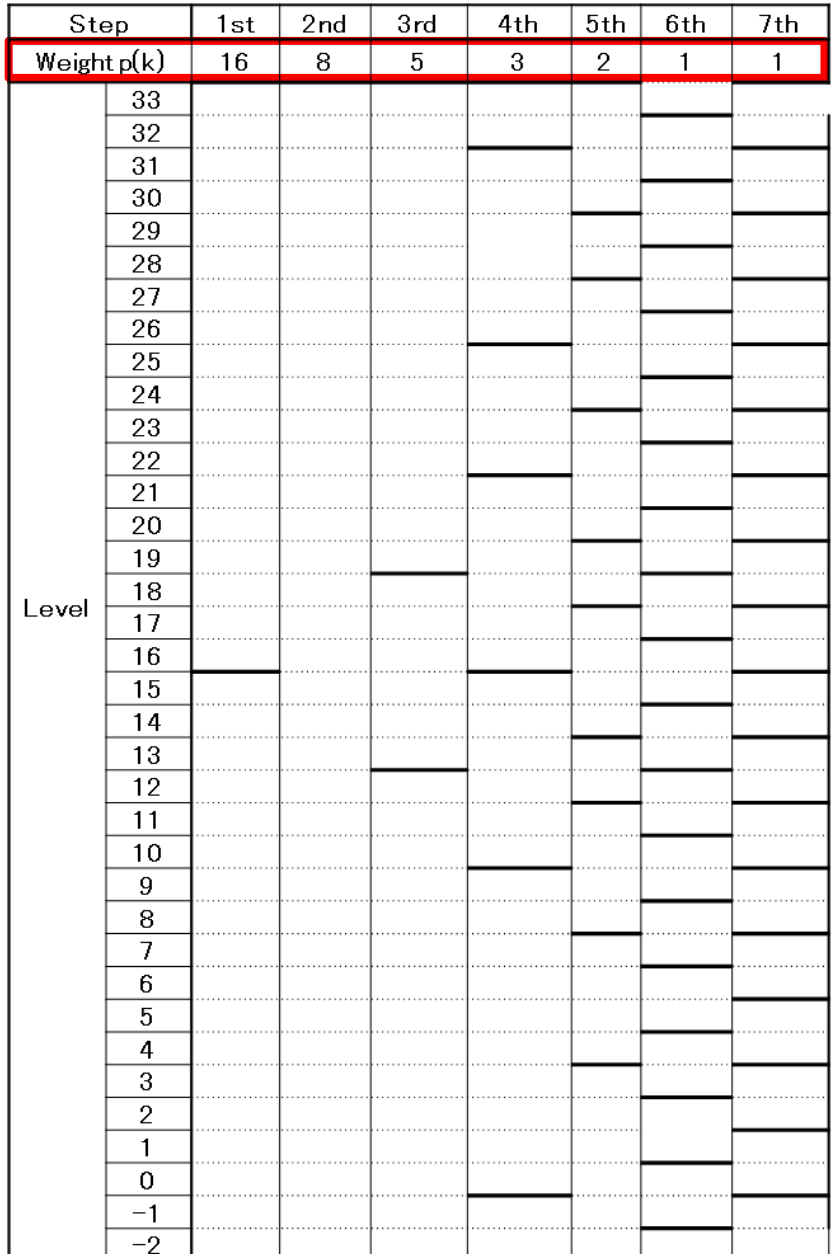
Realize 1.62 weighted by using only integer

Correction of Fibonacci Redundant Design

Fibonacci sequence SAR ADC

Detect new natures of two points !

1. ***Correctable range q(k) is always Fibonacci number*** F_{M-k-1}.
2. ***q(k) is exactly in contact q(k+1) without overlap.***



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Fibonacci sequence SAR ADC

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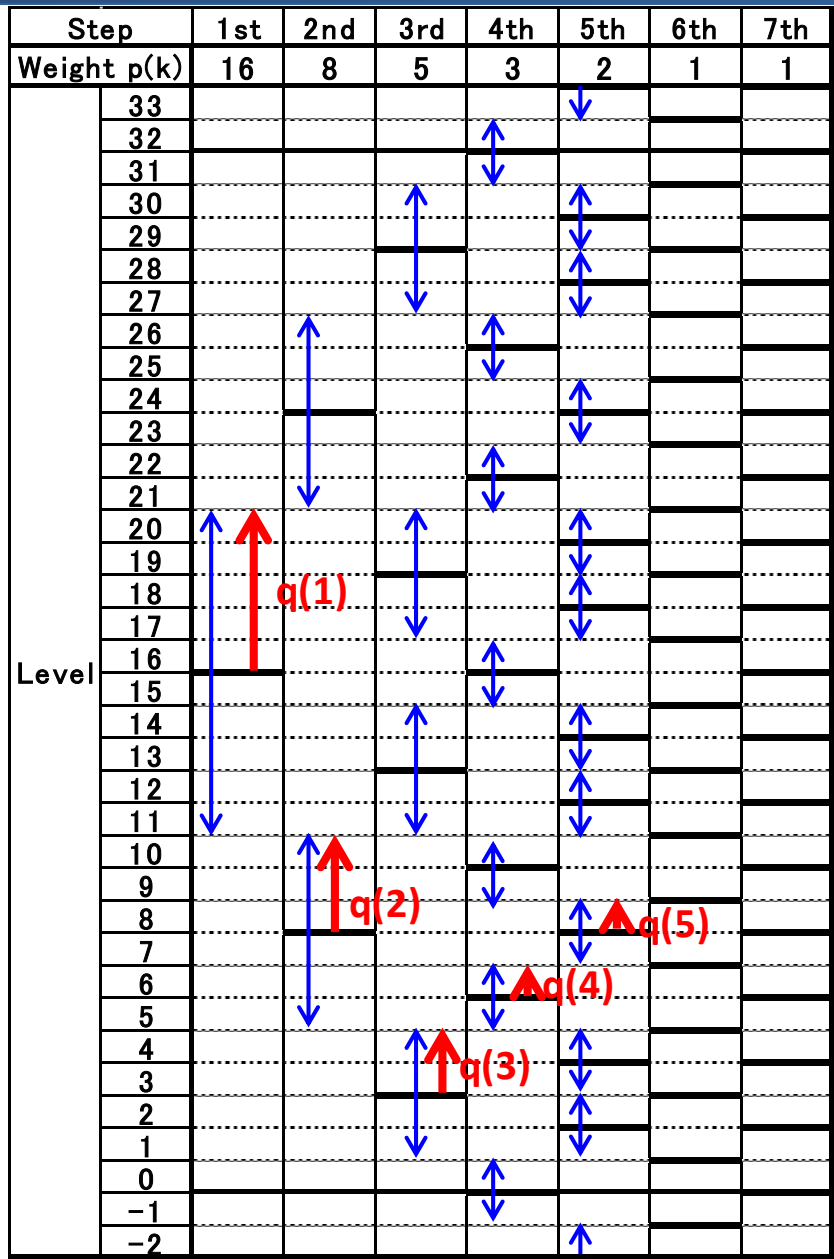

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Fibonacci sequence SAR ADC

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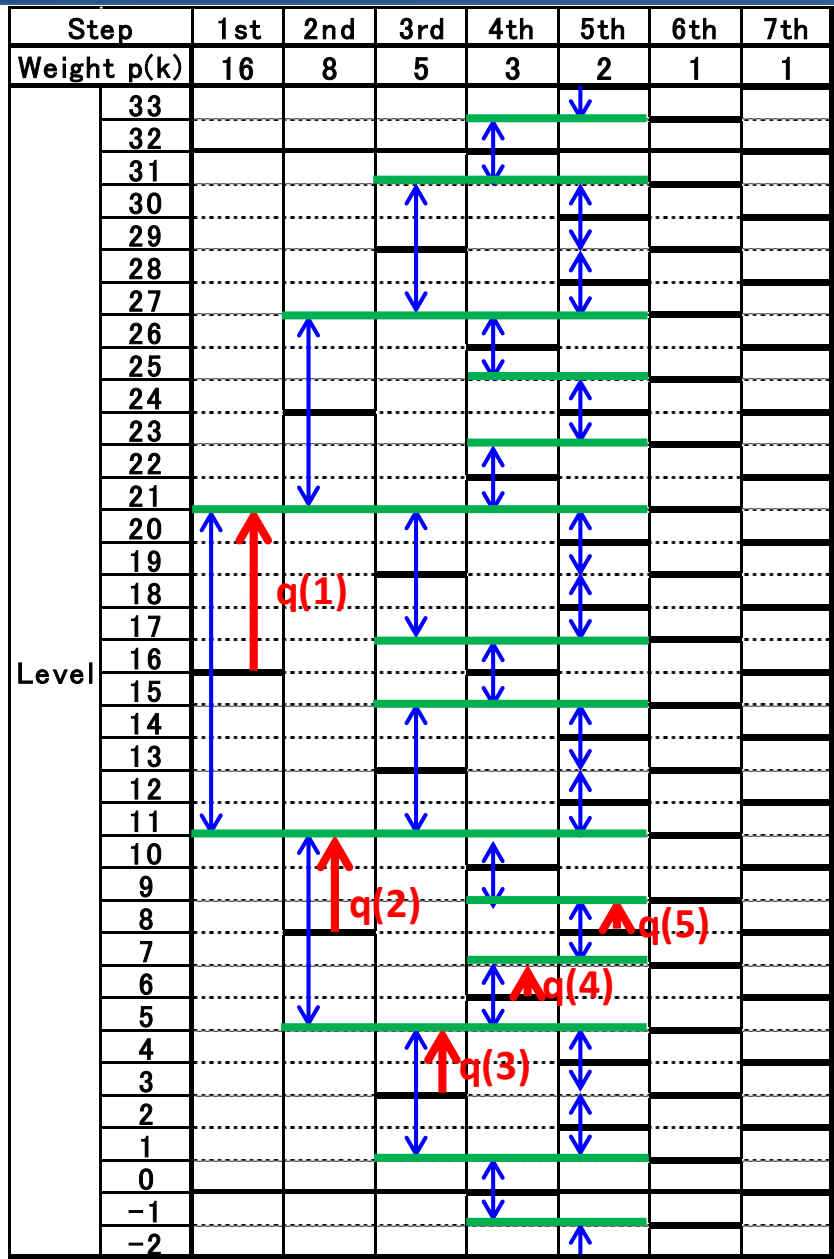


Correction of Fibonacci Redundant Design

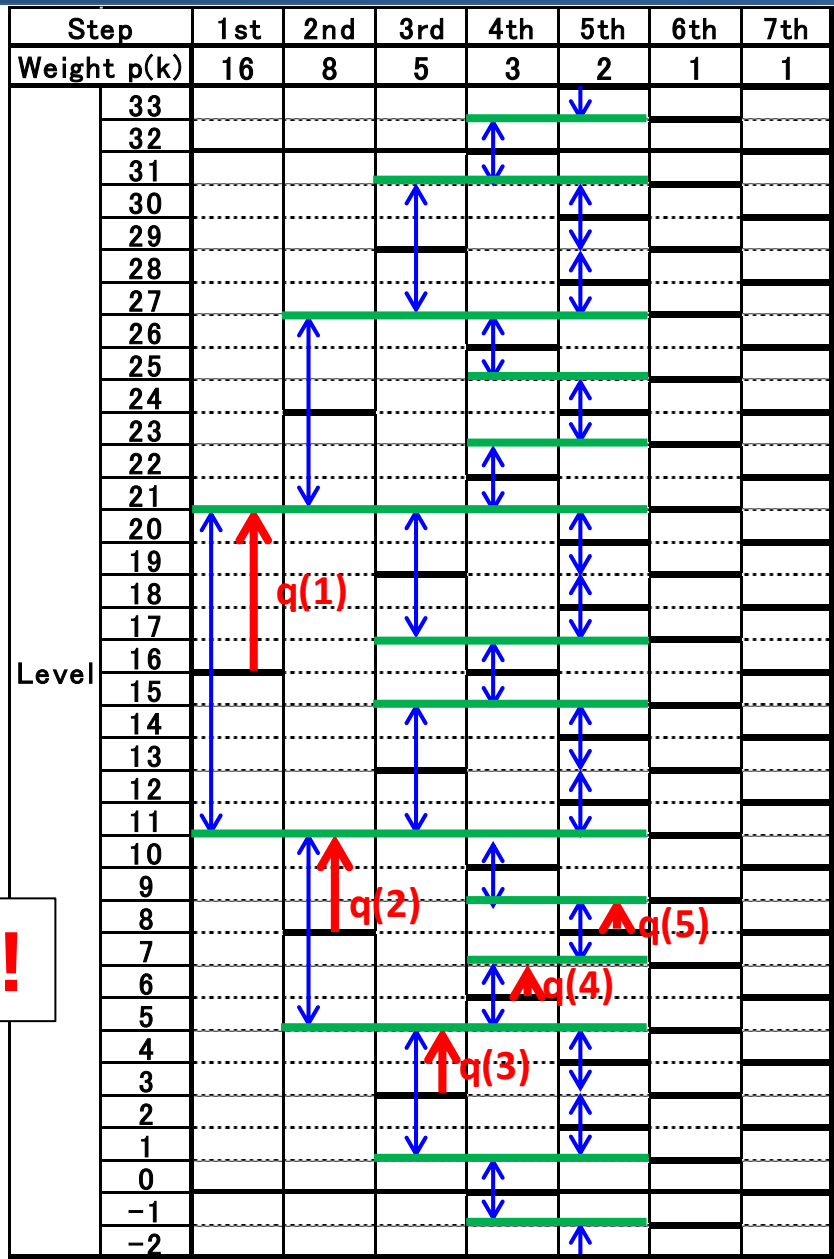
Fibonacci sequence SAR ADC

Detect new natures of two points !

1. ***Correctable range q(k) is always Fibonacci number*** F_{M-k-1}.
2. ***q(k) is exactly in contact q(k+1) without overlap.***

Golden ratio covers wide input range by minimum extra comparison steps.

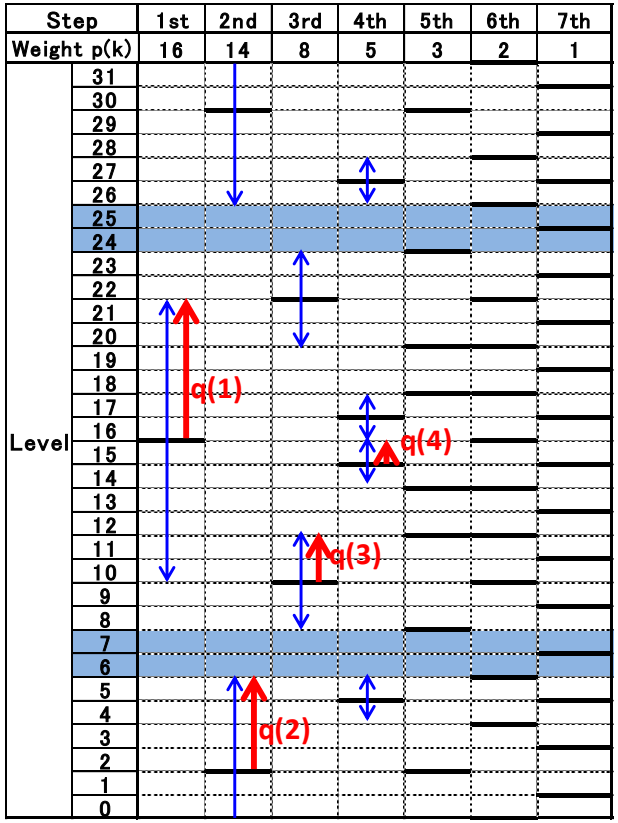
The most efficient design !

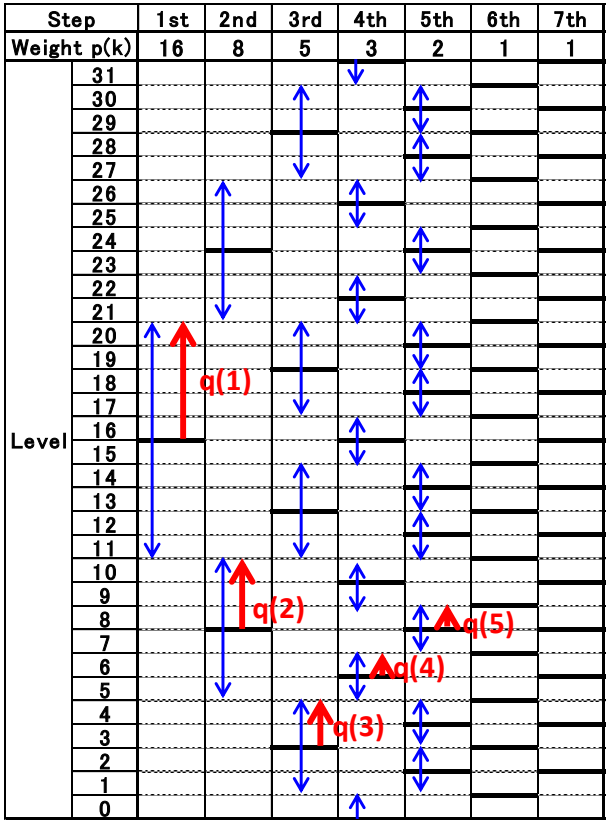


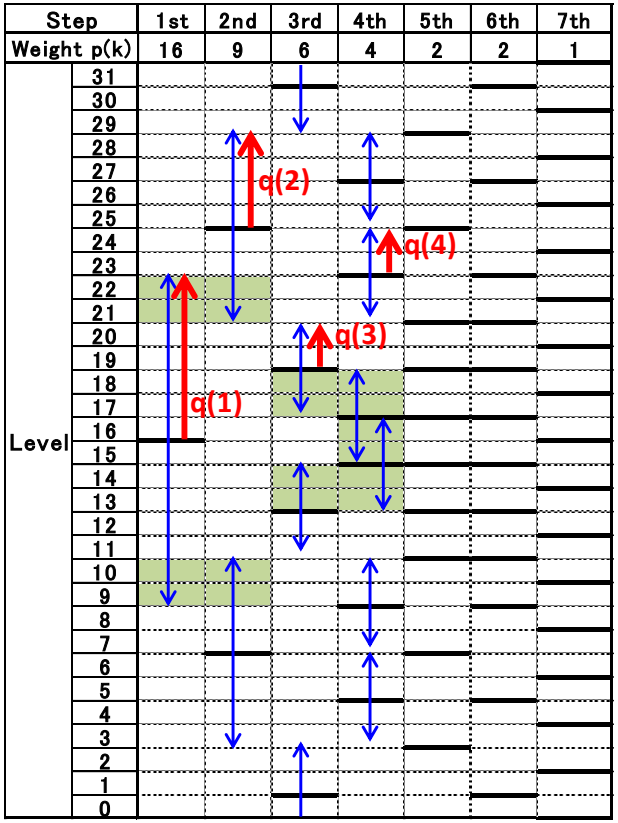
Comparison with Conventional Method

5bit SAR ADC

Conventional method	Proposed method	Conventional method
Radix=**1.7**	**1.62**	**1.55**
Radix is **bigger** than 1.62	**Standard !**	Radix is **smaller** than 1.62
⇨ **separated**		⇨ **overlapped**







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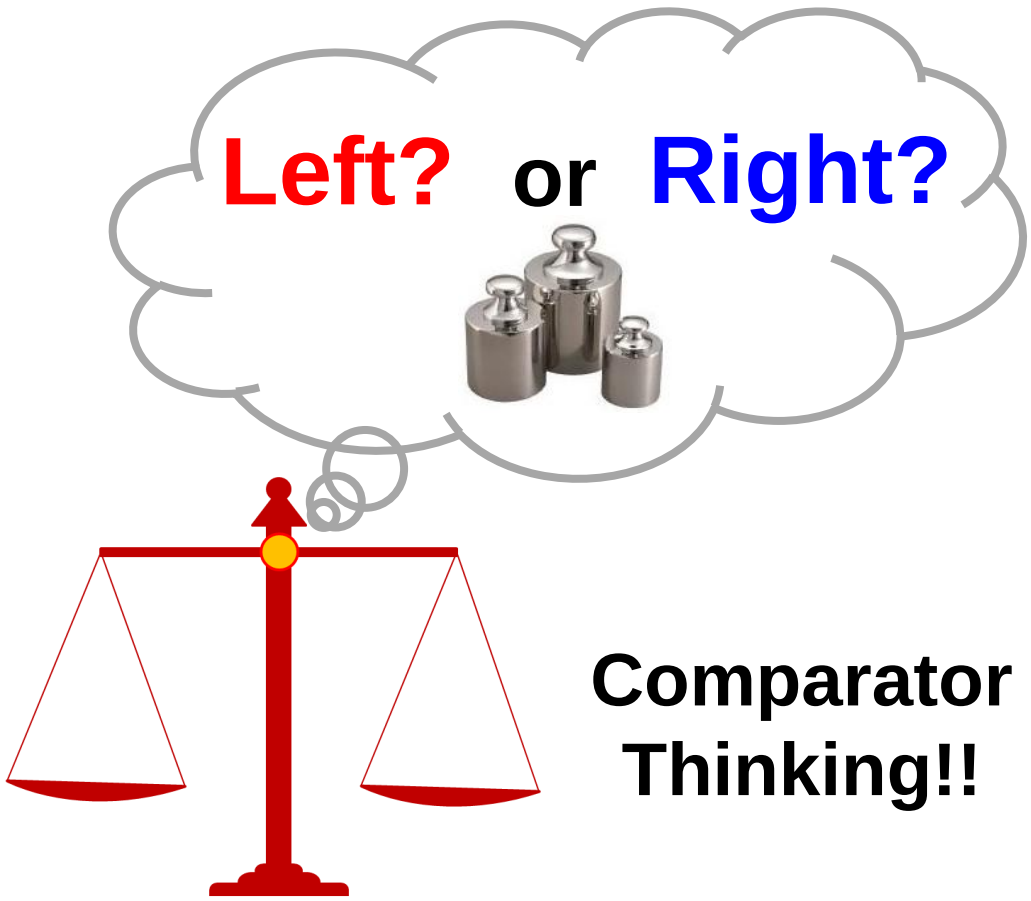
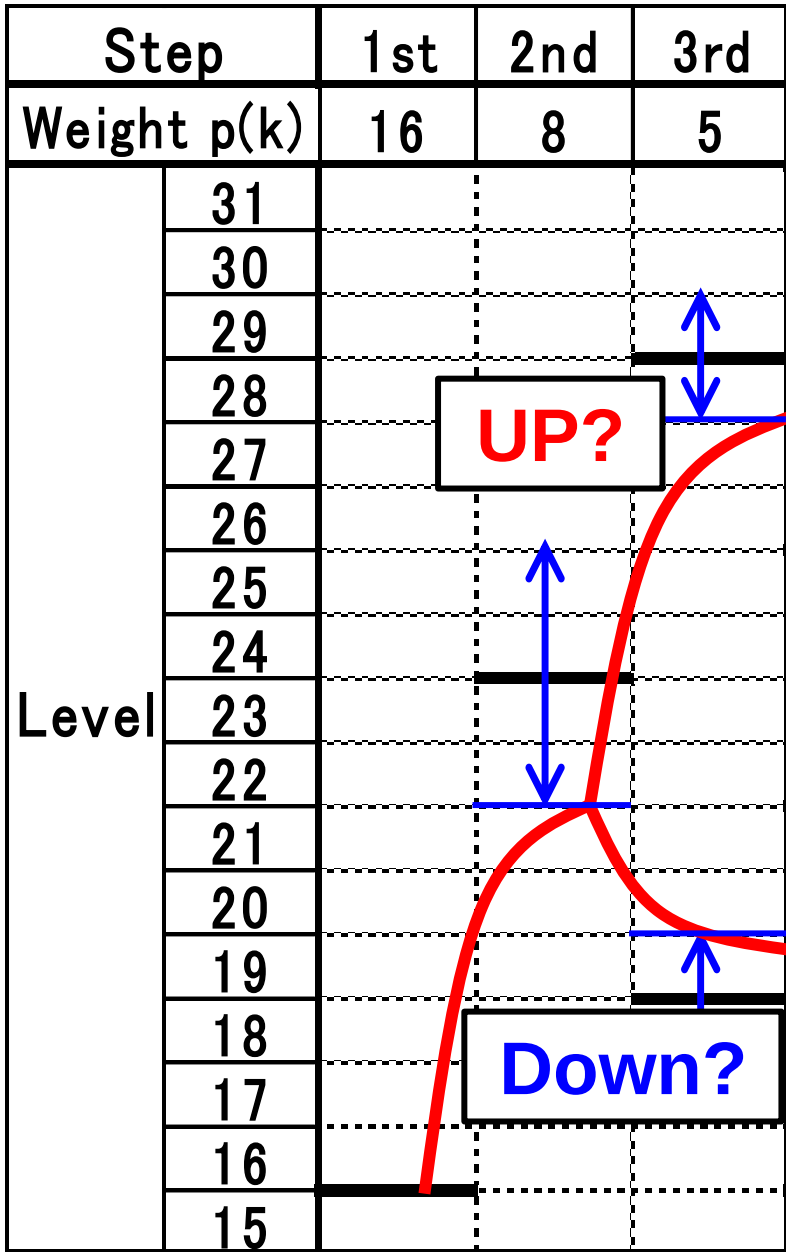
Settling Time

Settling Time

Transition time from kth step voltage to next step voltage

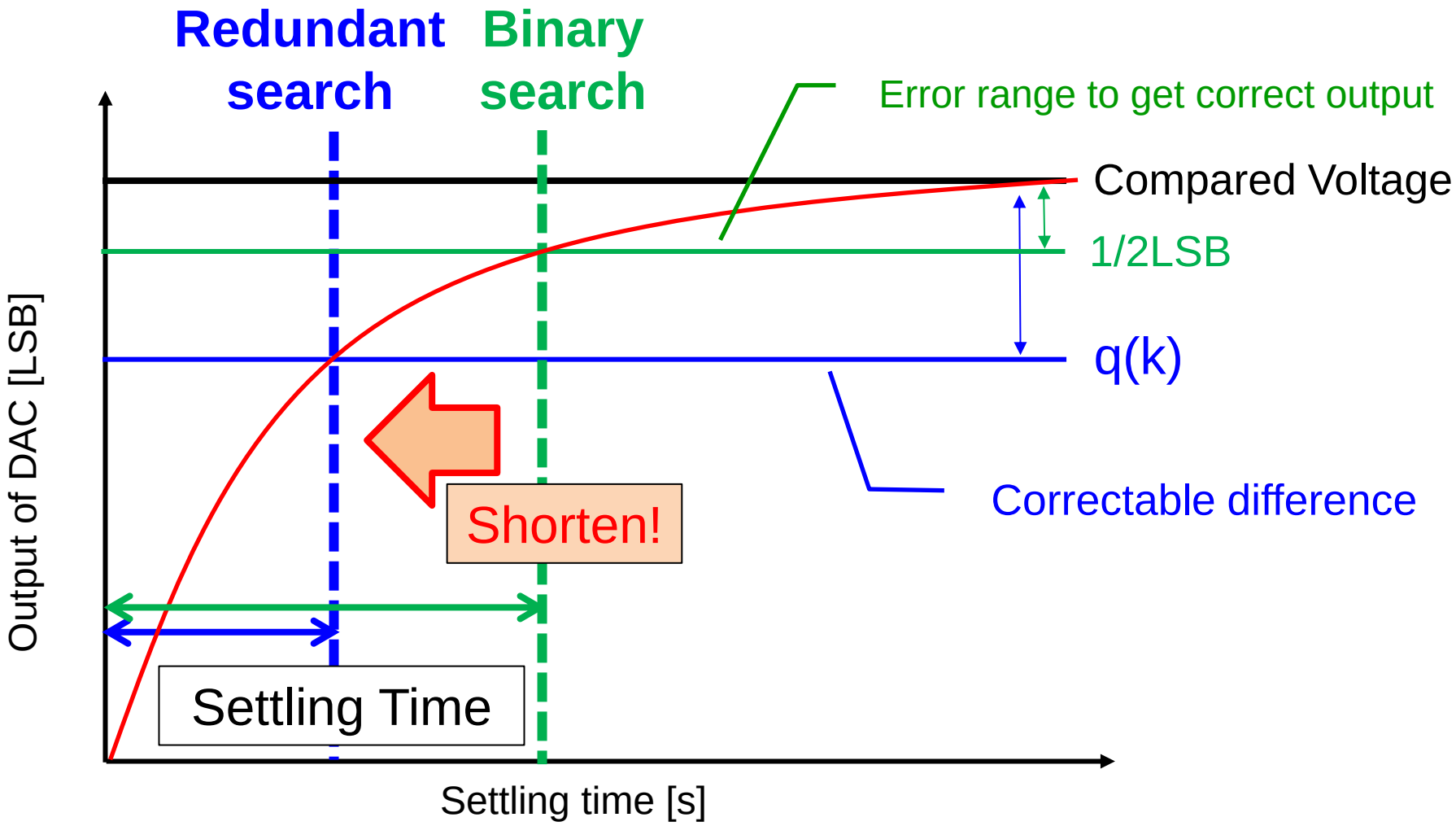


Comparator Thinking!!



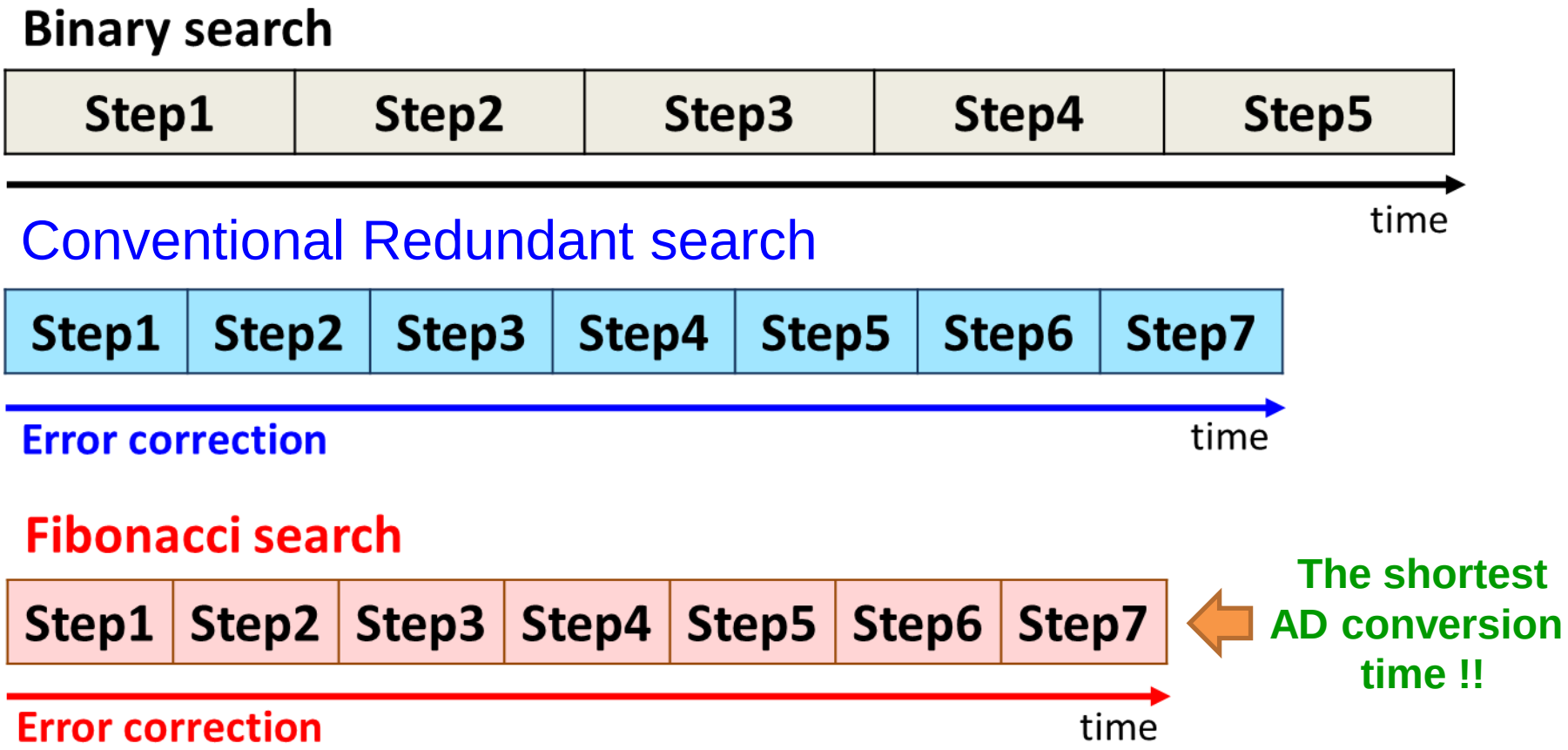
DAC Settling Time at Every Step

Shorten Conversion time

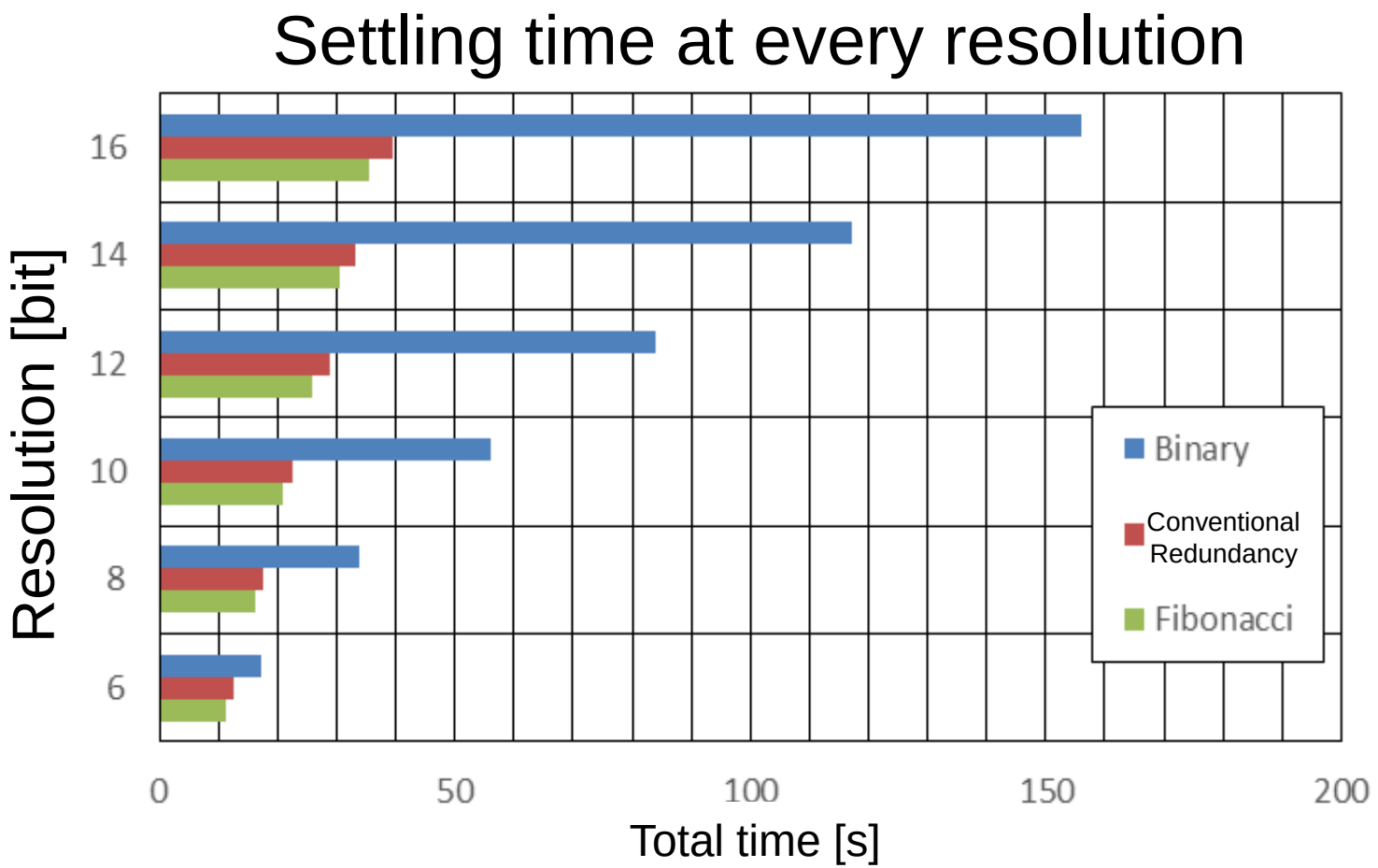


Reduction of Settling Time

5bit SAR ADC



Comparison of Incomplete Settling Time



At fixed clock,

Fibonacci ⇨ the shortest AD conversion time !!

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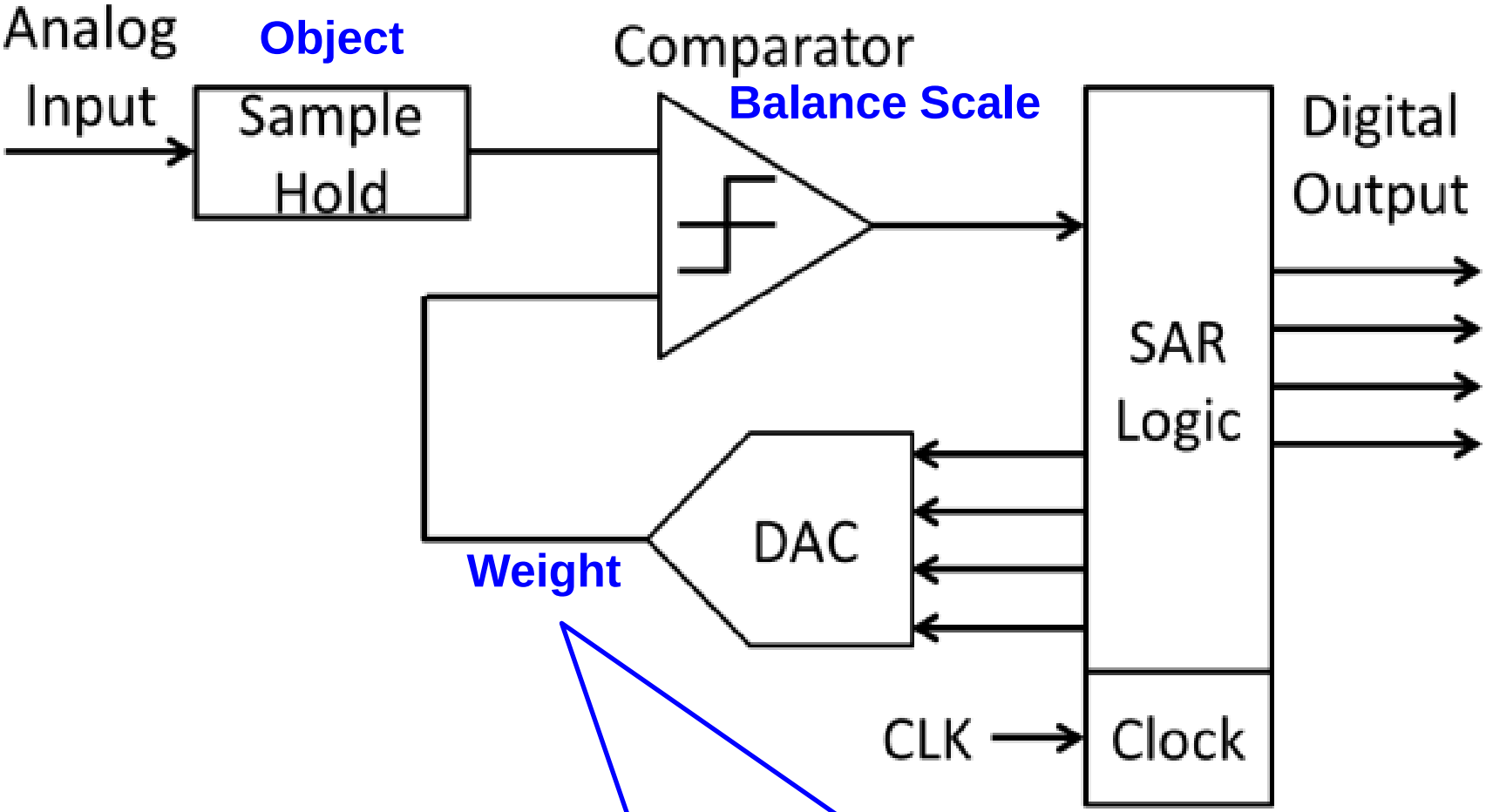
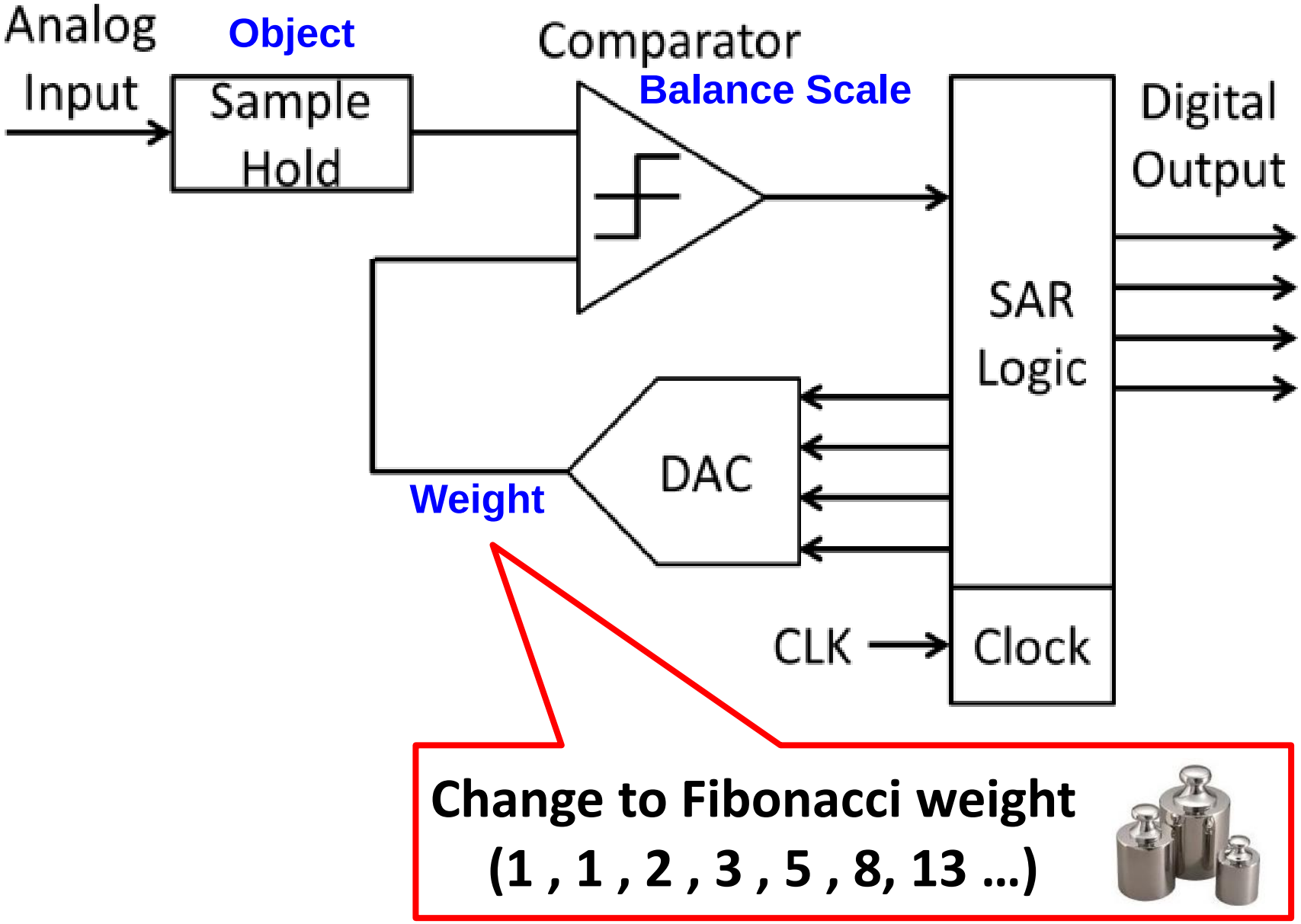
Binary SAR ADC Configuration

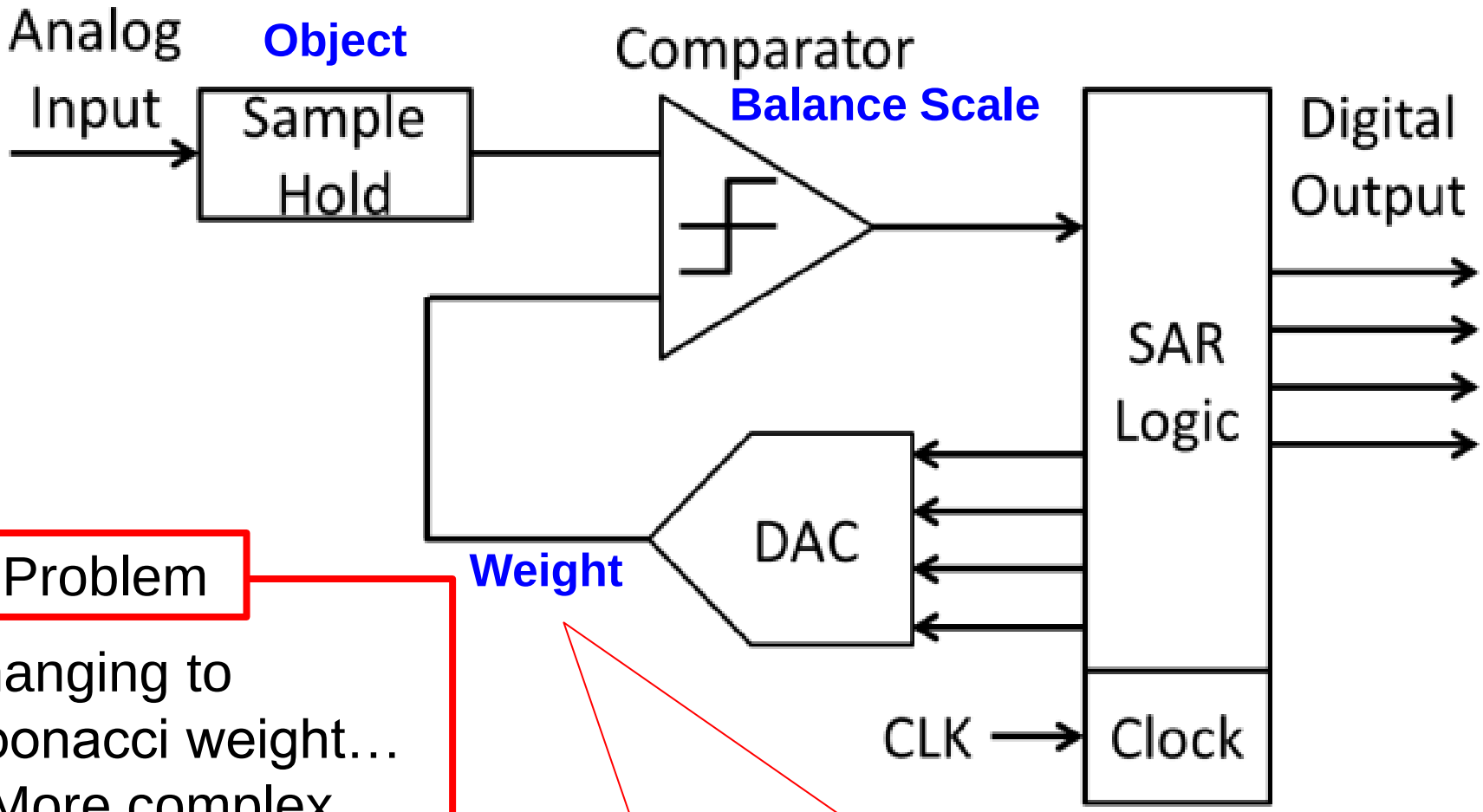


Generally use binary weight
(1 , 2 , 4 , 8 , 16 , 32, 64 …)

Fibonacci SAR ADC Configuration



Fibonacci SAR ADC Configuration



Problem

Changing to Fibonacci weight…

- More complex
- More large-scale

than conventional.

Change to Fibonacci weight

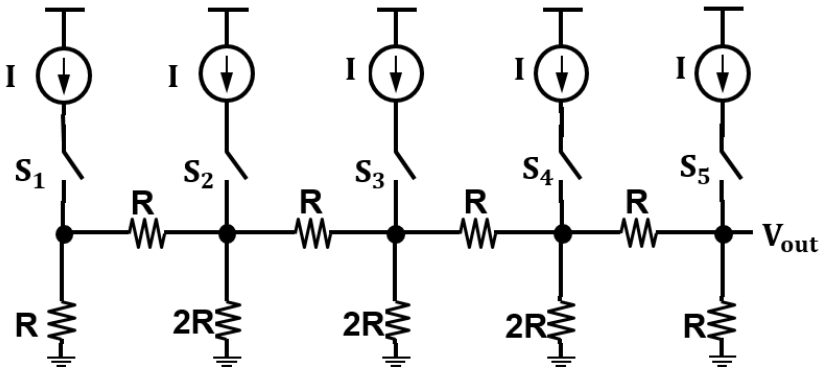
(1 , 1 , 2 , 3 , 5 , 8, 13 …)

Conventional and Proposal DAC

Conventional

R-2R resistor ladder

⇒Generate **binary** voltage



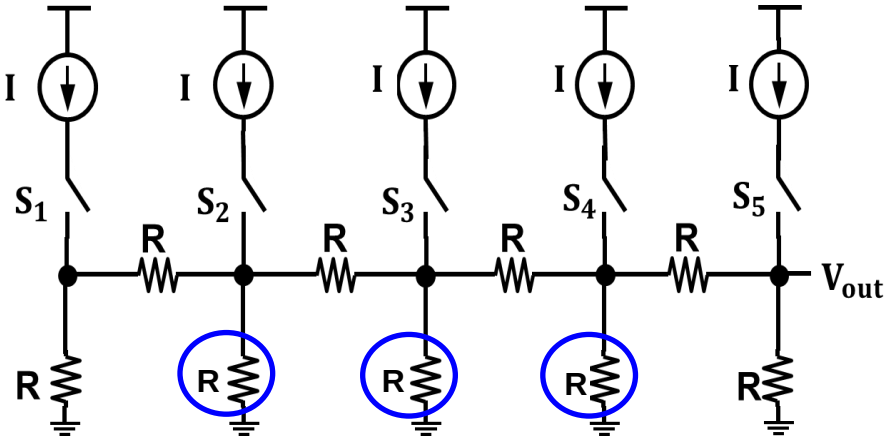
R-2R resistor ladder

Change all resistors to R

Proposal

R-R resistor ladder

⇒Generate **Fibonacci** voltage



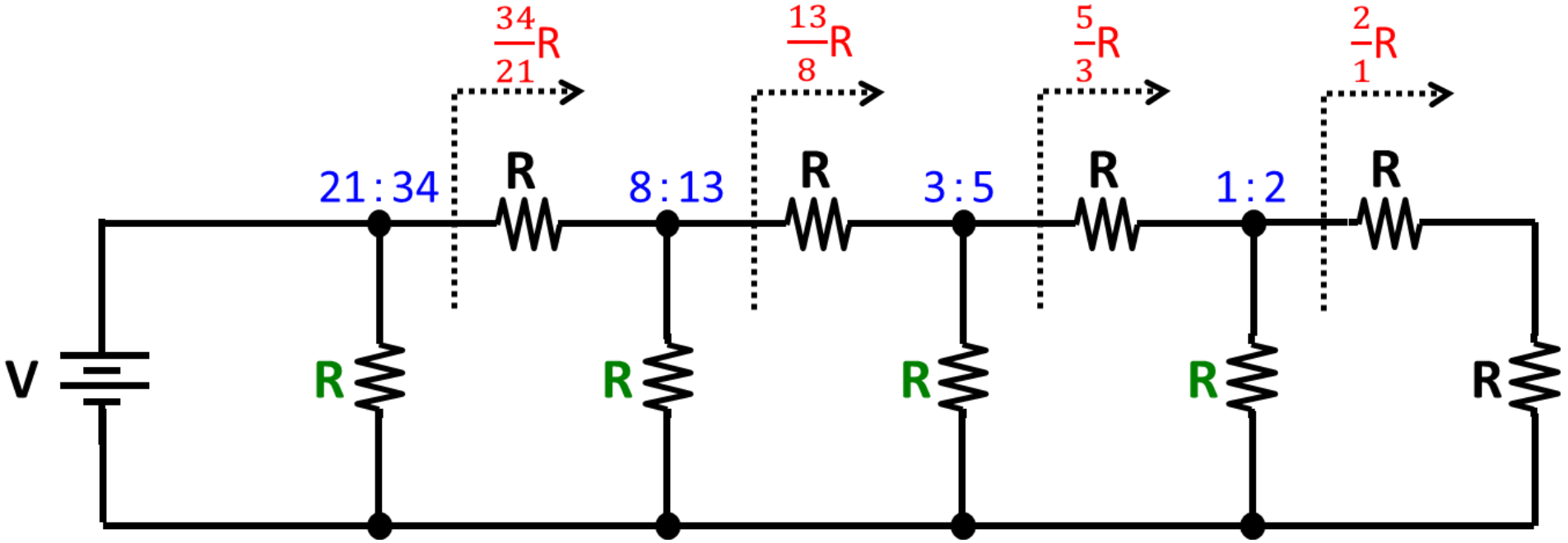
R-R resistor ladder

Realize Fibonacci DAC
by using simple circuit !

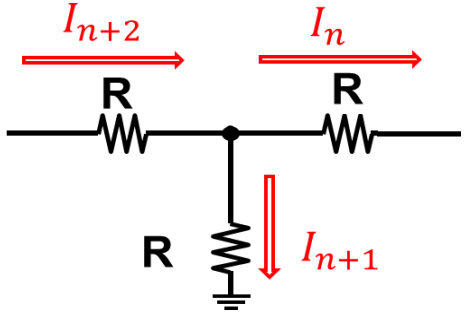
Principle of Fibonacci Voltage

New property

Divides current into **Fibonacci ratio** in each node



Principle



$$I_{n+2} = I_{n+1} + I_n$$

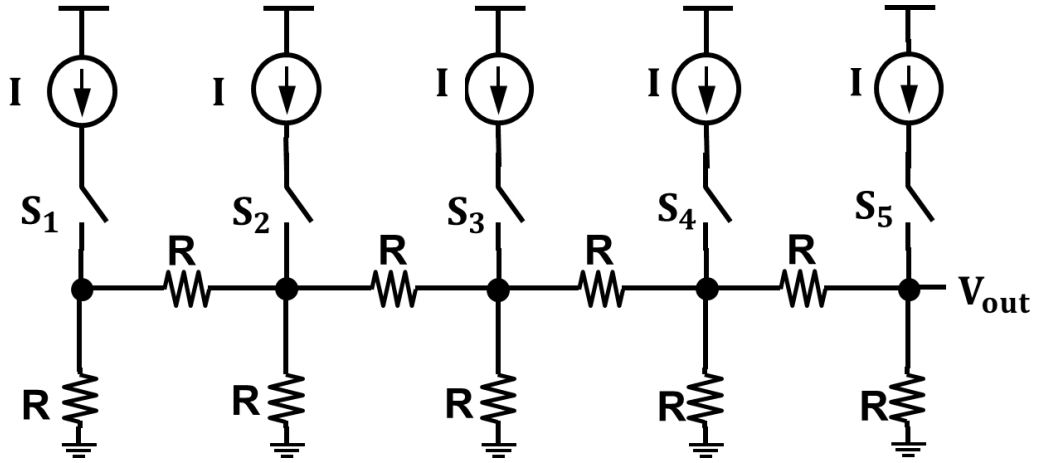
$$\Updownarrow$$

$$F_{n+2} = F_{n+1} + F_n$$

Proposal of R//R Fibonacci DAC

R-R resistor ladder

Generate
Fibonacci voltage
of **odd** term

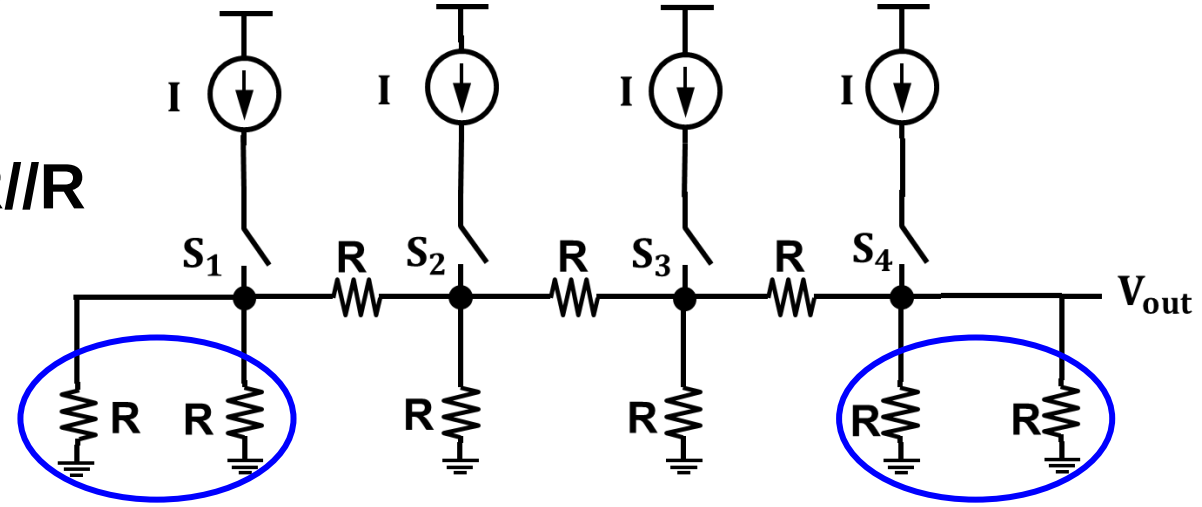


Change terminal resistors to
parallel resistors

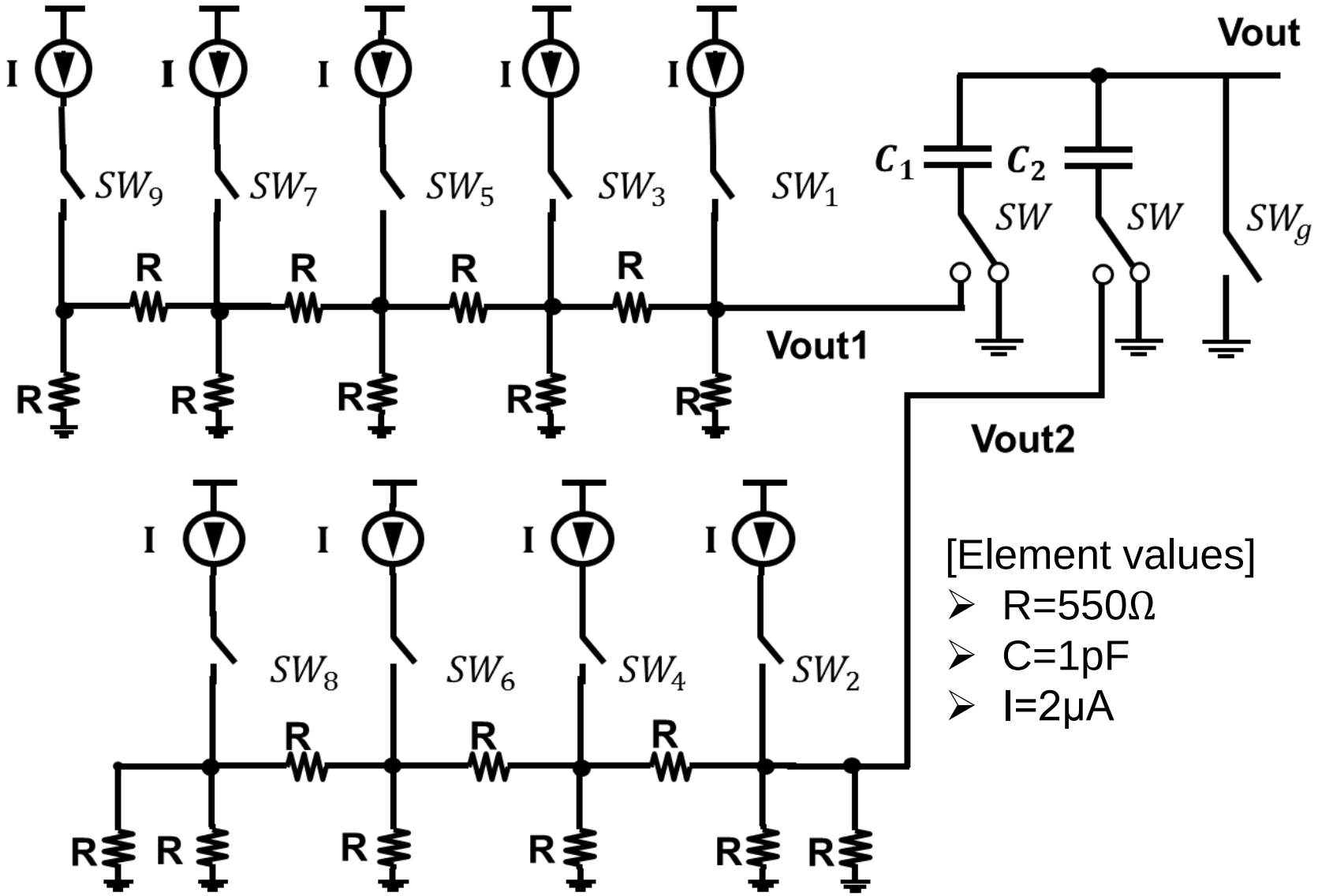
Proposal

R-R resistor ladder
with terminations of R//R

Generate
Fibonacci voltage
of **even** term



Fibonacci DAC simulation



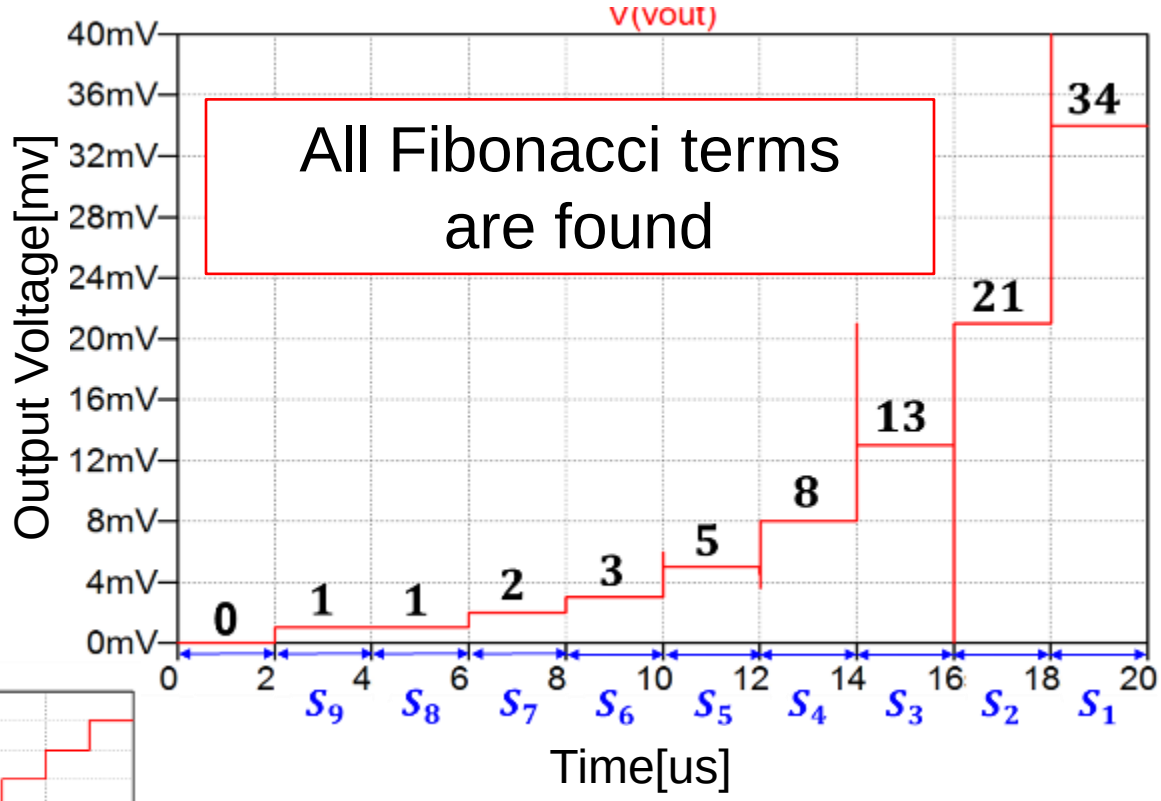
[Element values]

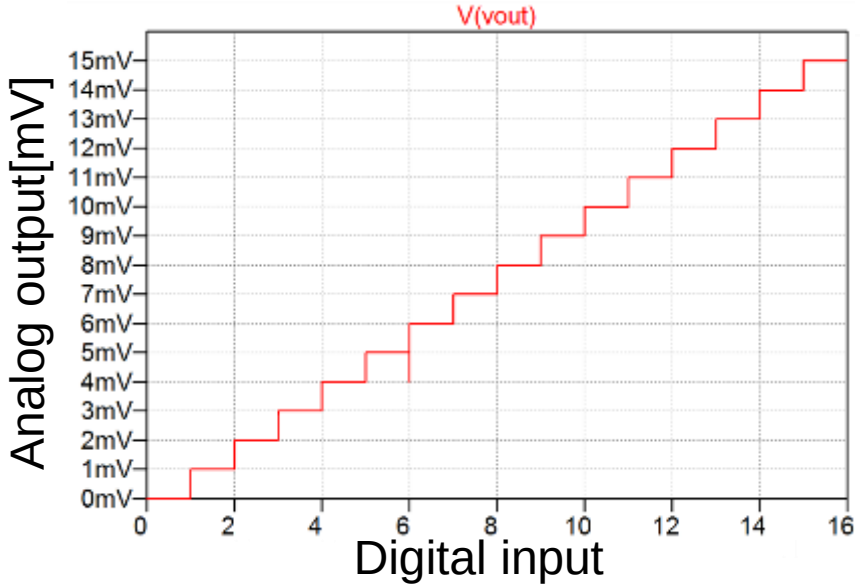
- R=550Ω
- C=1pF
- I=2μA

Simulation Result

Operation simulation

Each switch corresponds to a Fibonacci term





A-D conversion simulation

Combination of current sources realizes DAC function

Fibonacci DAC is realized ☺

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- **Conclusion**

Conclusion

- Propose redundant SAR ADC design methods

- Get important properties by using Fibonacci sequence
  - **Reliable**
    Correctable difference covers wide input range
  - **Shortest-Conversion**
    Conversion time is shortest in a fixed clock
  - **Radix-Standard**
    Golden ratio φ establish radix standard

- Propose beautiful DAC structures
  which generate Fibonacci voltages.

Final Statement

“The world is made of mathematics “

by Isaac Newton

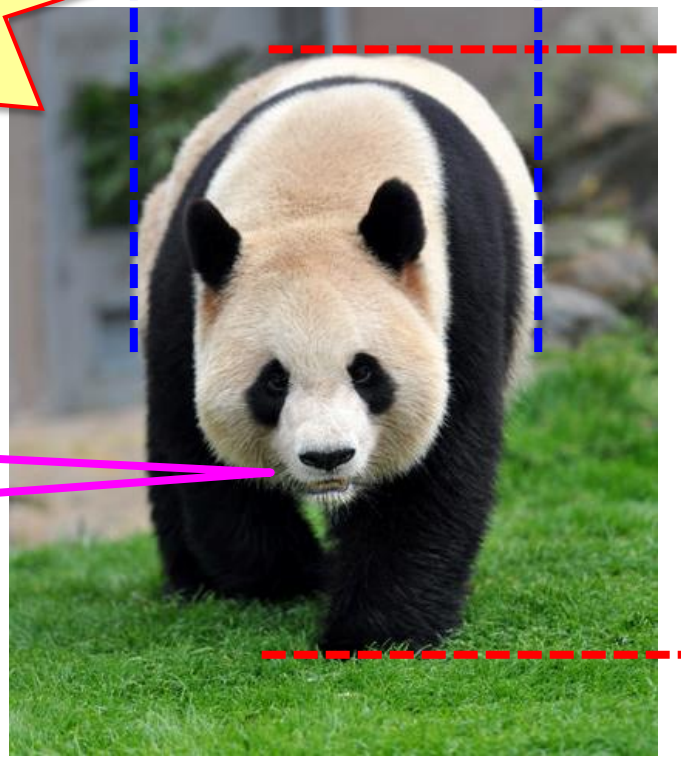
Isaac Newton
(UK:1642-1727)

ADC
DAC
+ Mathematics = New mysterious property

Beautiful mathematics leads to beautiful circuit.

Thank you for listening

Golden Ratio



謝謝