IEEE 11th International Conference on ASIC
November 3-6, 2015, Chengdu, China

Study on Maximum Electric Field Modeling Used for HCI Induced Degradation Characteristic of LDMOS Transistors

Masashi Higashino*, Hitoshi Aoki, Nobukazu Tsukizi,
Masaki Kazumi, Takuya Totsuka, Haruo Kobayashi

Gunma University, Japan

Supported by MoDeCH Inc.

OUTLINE

- Introduction
- Our Research
  - HCI Degradation Modeling
  - Maximum Electric Function Equation
- Conclusion

OUTLINE

- Introduction
- Our Research
  - HCI Degradation Modeling
  - Maximum Electric Function Equation
- Conclusion

Background and Object

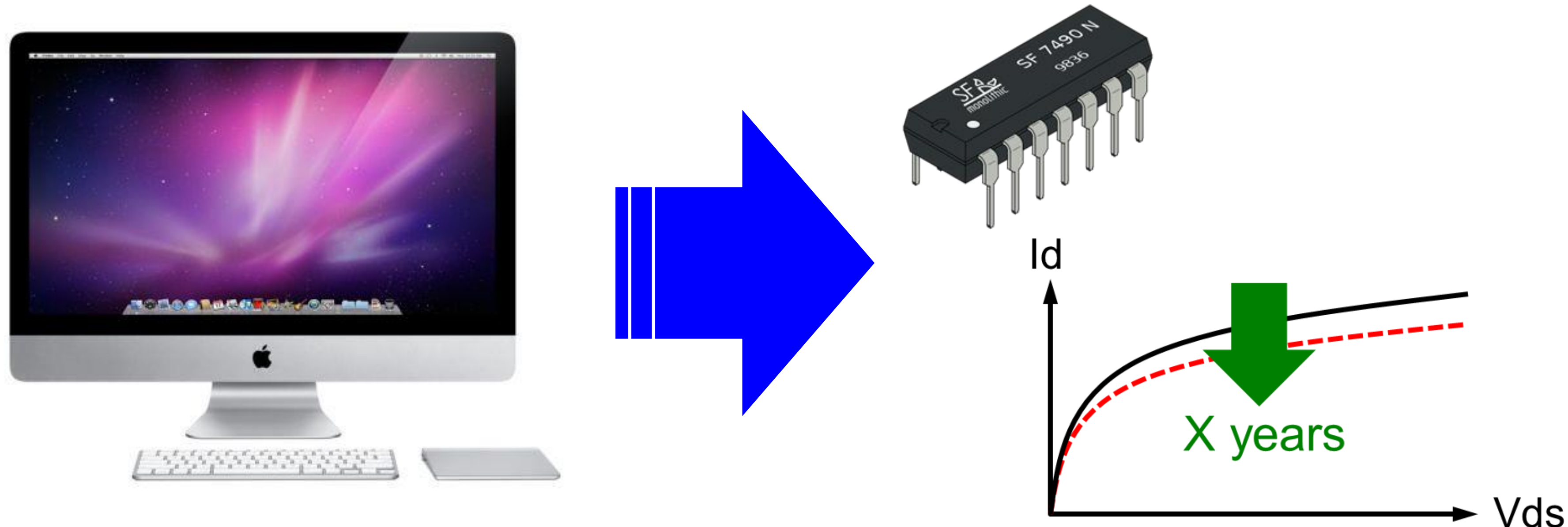
Reliability Test Problem in Circuit Design

Test Items	Conditions
High Temperature Operating Life	Ta=125℃ Vop_max, 1000h
Temperature Humidity Bias	Ta=85℃ 85%RH Vop_max, 1000h

Our object

Circuit design considering with reliability simulations

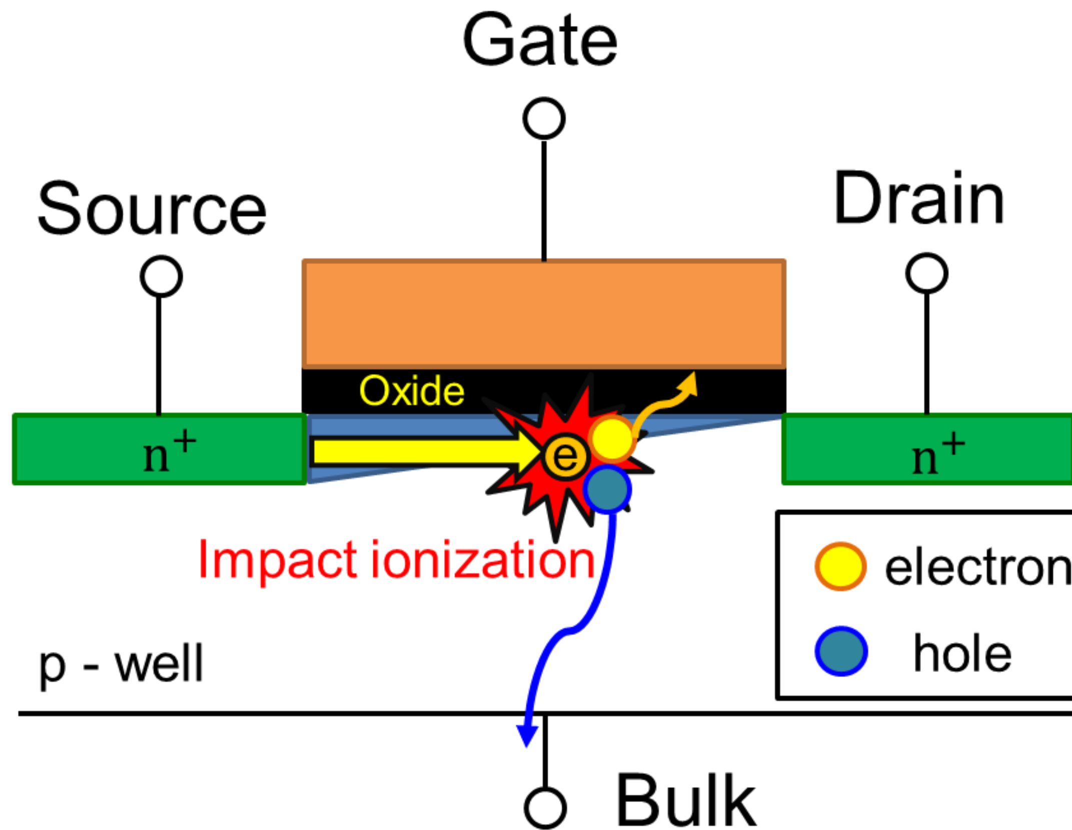
Research Purpose

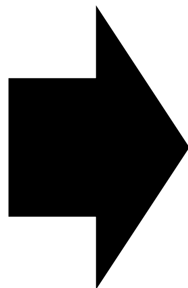


- **Degradation modeling** by HCI of n-channel LDMOS'
- **Maximum electric field modeling** for reliability circuit simulations

HCI : Hot Carrier Injection, LDMOS : Laterally Diffused MOSFET

Degradation by Hot Carrier Injection

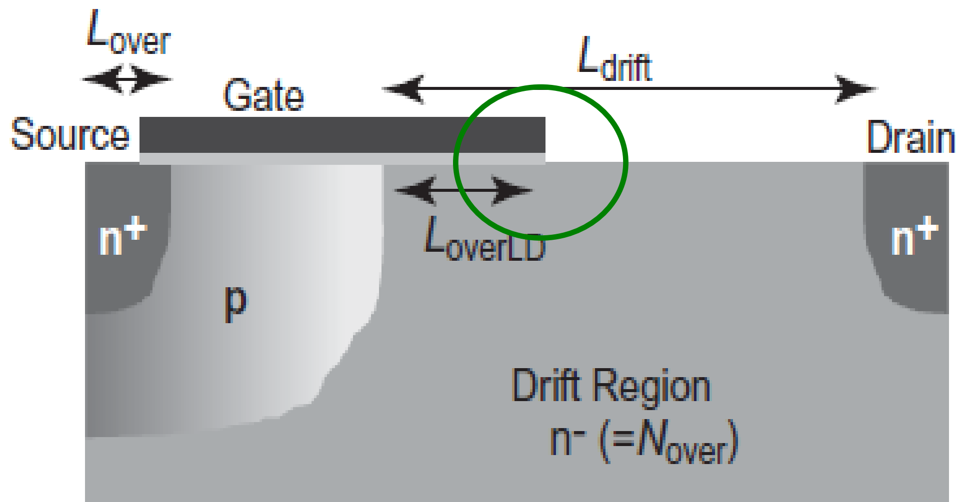




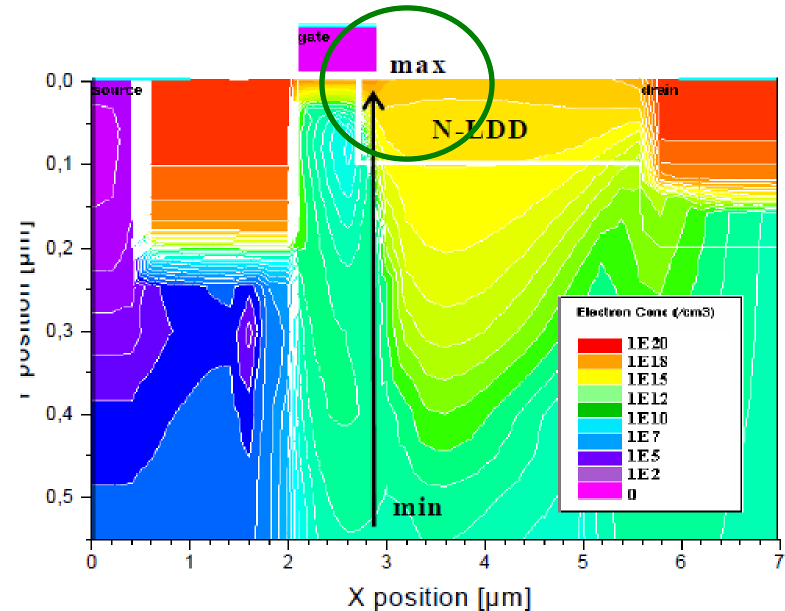
Important parameters

- Threshold voltage
- Carrier mobility

Degradation of LDMOS Devices



Cross view section view of an the LDMOS [1]



Electric field distribution of n-channel LDMOS [2]

High lateral electric field at the gate edge

Maximum Electric Field Model should be developed !!

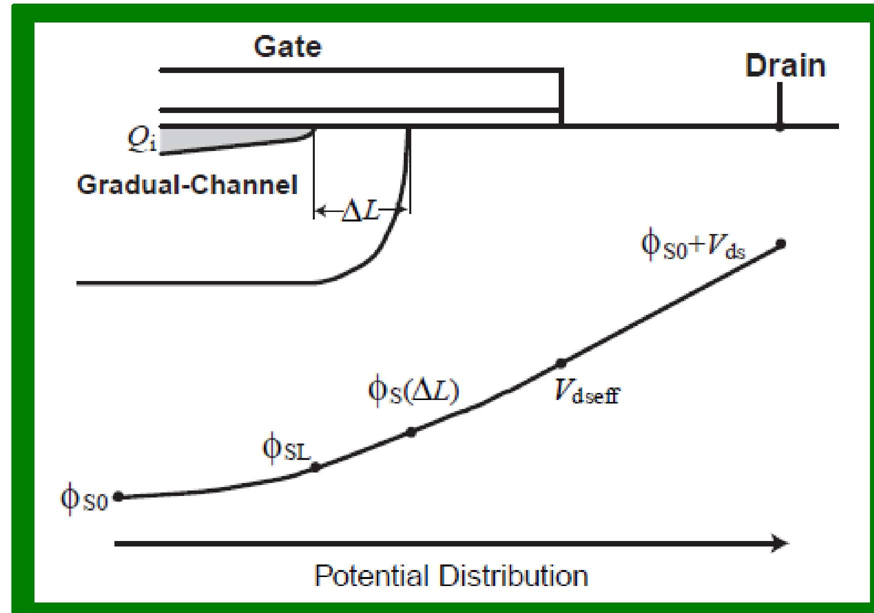
OUTLINE

- Introduction
- Our Research
  - HCI Degradation Modeling
  - Maximum Electric Function Equation
- Conclusion

HiSIM-HV Model for Modeling Vehicle

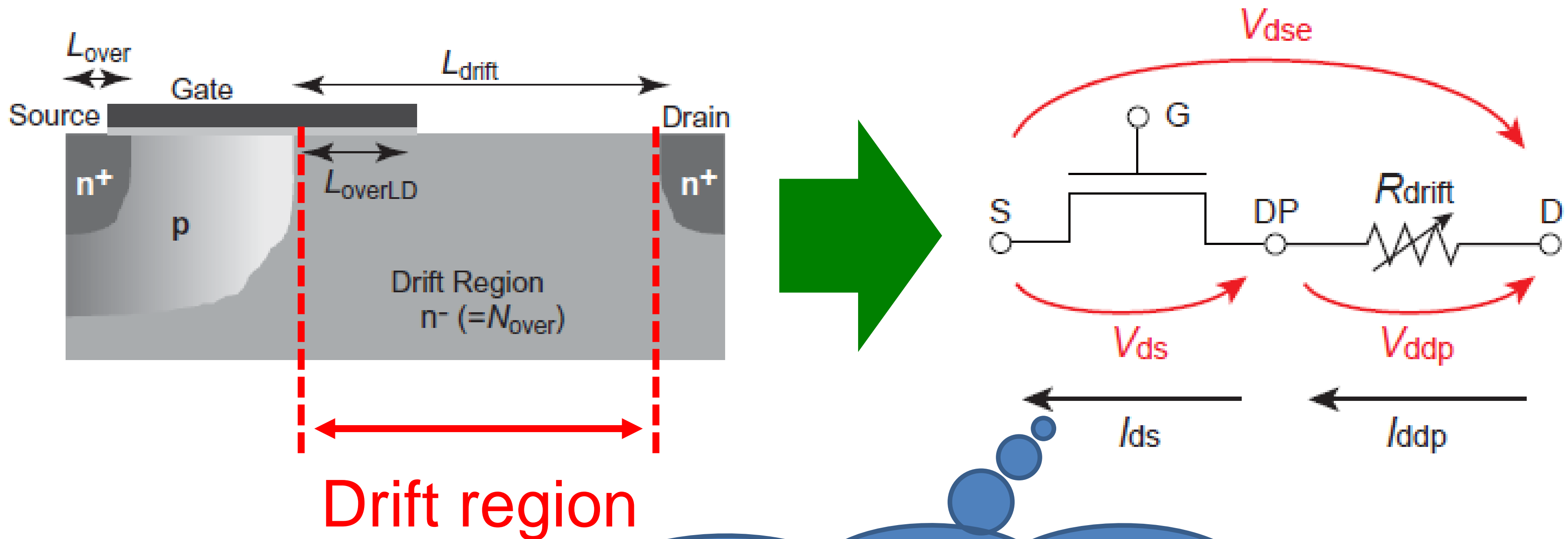
- Hiroshima-University STARC IGFET Model-High Voltage

- International Industry Standards Model
- Based on Surface-Potential



[1] HiSIM-HV 2.2.0 User's manual

HiSIM-HV Model used for LDMOS

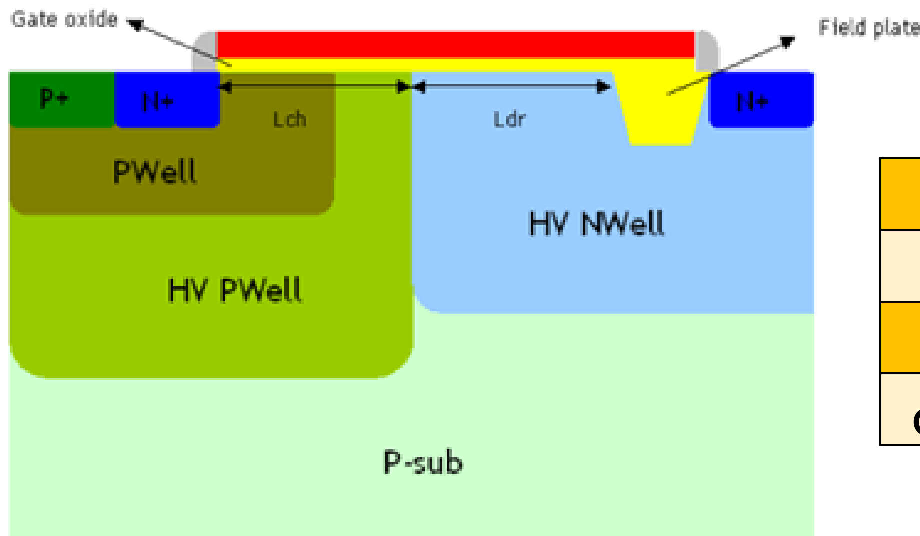


- Voltage drop at drift region
- Represent as an internal variable R_{drift}

[1] HiSIM-HV 2.2.0 User's manual

Model Parameter Extraction and Simulations

■ Used measured data



Cross section view of
an n-channel LDMOS [3]

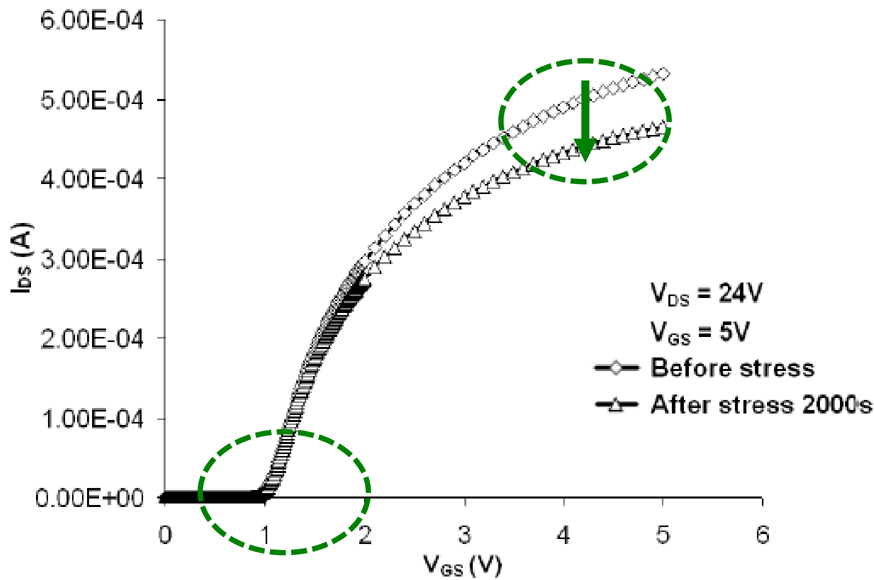
Process data [3]

process size	0.18 um
gate lenth	0.4 um
gate width	20 um
oxide thickness	11.5 nm

[3] N. Soin.S.S.Shahabudin and K.K.Goh, et al,: “Measurement and Characterization of Hot Carrier Safe Operating Area (HCI-SOA) in 24V n-type Lateral DMOS Transistors”,10th IEEE International Conference on Semiconductor Electronics, pp.659-663 (2012)

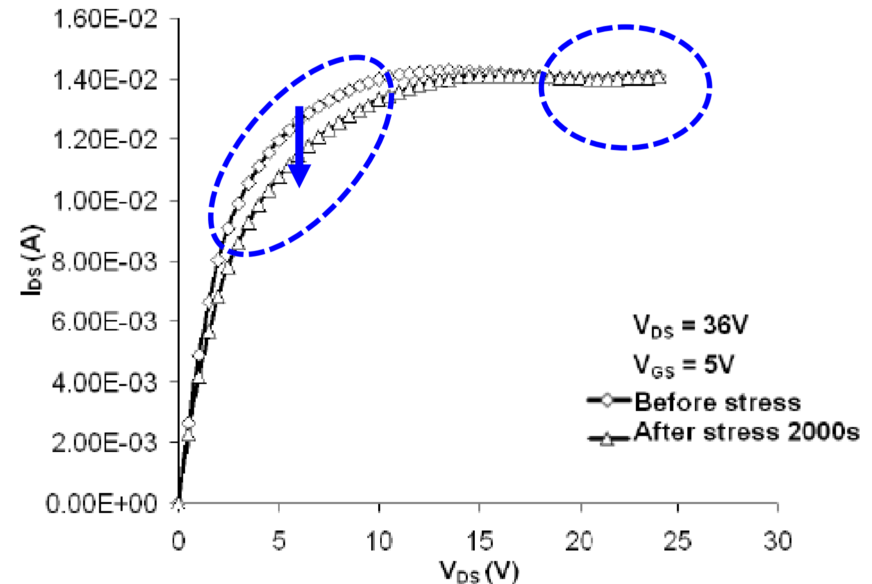
Analysis of Stress Measurement Results

Ids-Vgs characteristics



- Vth is not changed
- Decreasing Ids

Ids-Vds characteristics



- Ids in saturation region is Not changed
- Ids in pinch-off region is decreased

[3] N. Soin.S.S.Shahabudin and K.K.Goh, et al,: "Measurement and Characterization of Hot Carrier Safe Operating Area (HCI-SOA) in 24V n-type Lateral DMOS Transistors",10th IEEE International Conference on Semiconductor Electronics, pp.659-663 (2012)

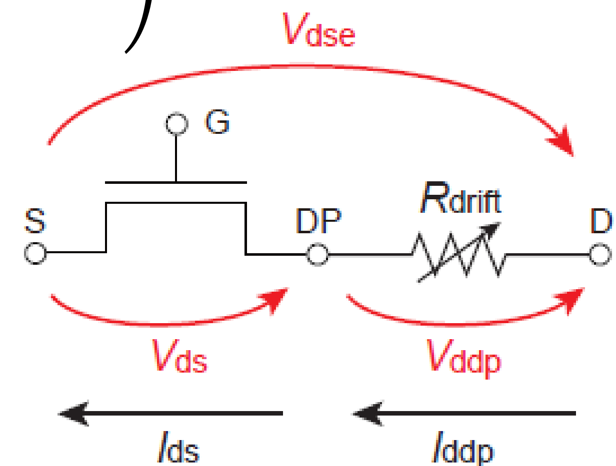
Parameter Selection of HiSIM-HV

$$R_{drift} = (R_d + V_{ds}R_{DVD})\left(1 + RDVG11 - \frac{RDVG11}{RDVG12}V_{gs}\right)$$

$$(1 - V_{bs}RDVB)\left(\frac{LDRIFT1 + LDRIFT2}{DDRIFT - W_{dep}}\right)$$

$$R_d = \frac{R_{d0}}{W_{eff,LD}NF}\left(1 + \frac{RDS}{(W_{gate}10^6 L_{gate}10^6)^{RDSP}}\right)$$

$$R_{d0} = (RD + R_{d0,temp})f_1 f_2$$

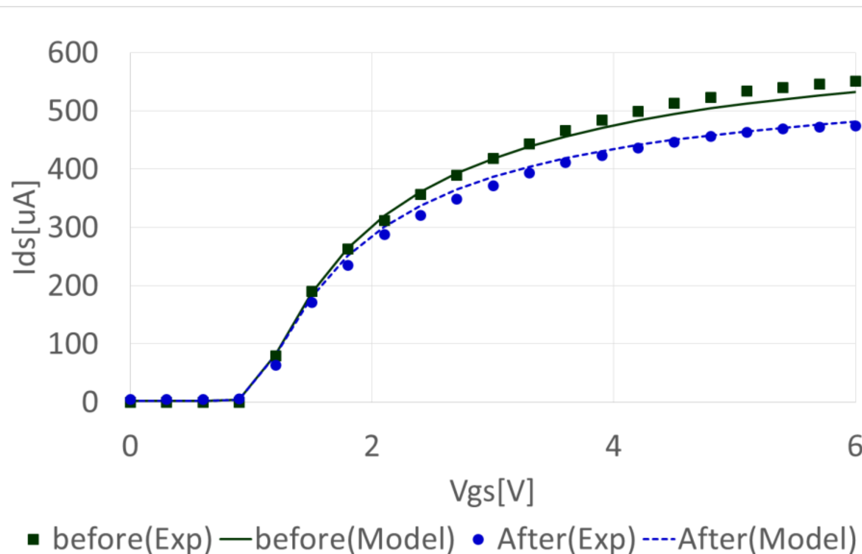


[1] HiSIM-HV 2.2.0 User’s manual

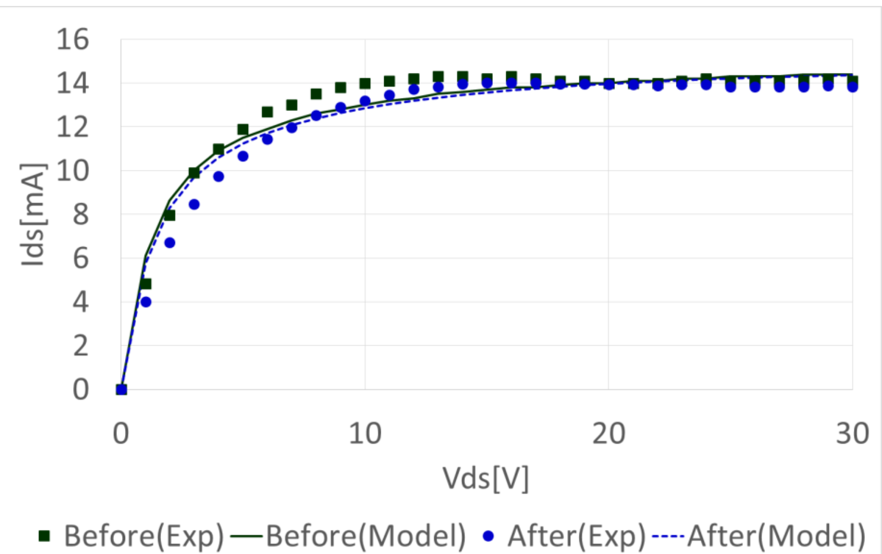
RD Degradation Model

RD : Before 1.1mΩ After 1.4mΩ

Ids-Vgs characteristic



Ids-Vds characteristic

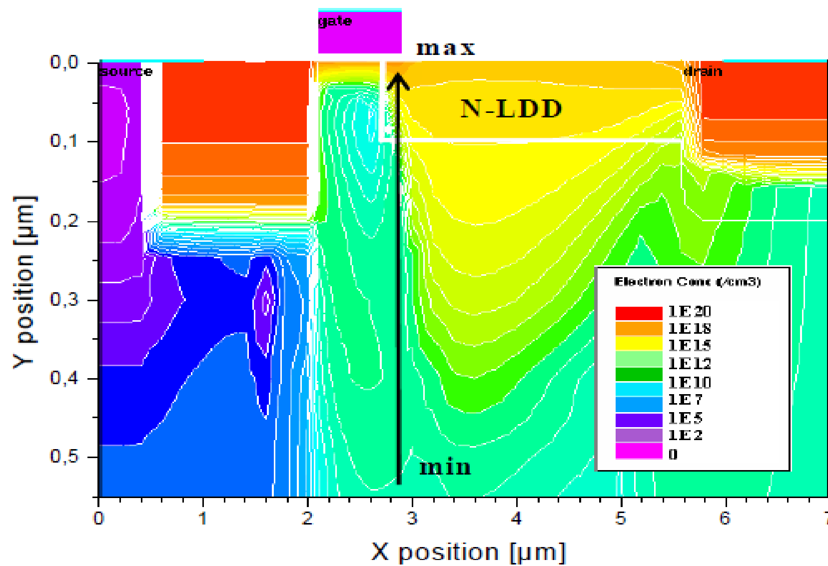


Increased R_{on} by decreasing carrier in drift region

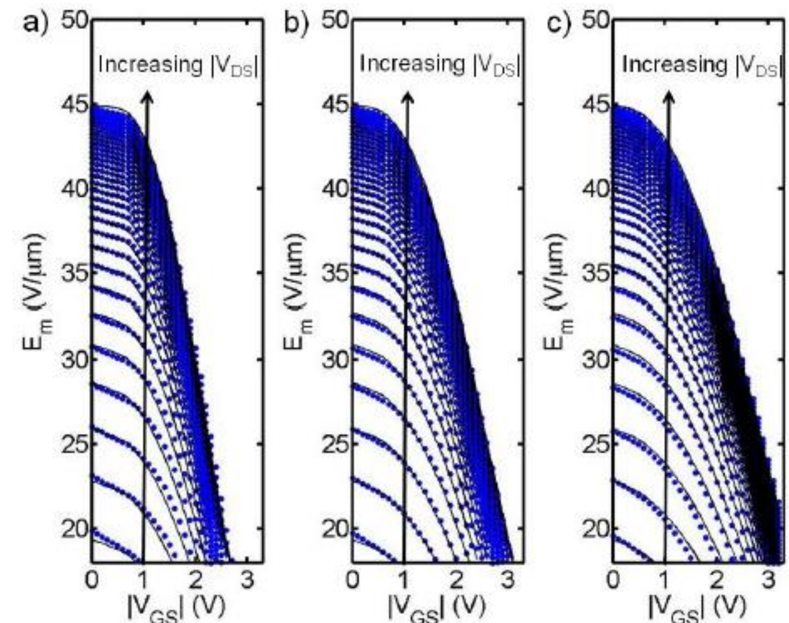
Maximum Electric field for the Degradation Model

$$\frac{\Delta R_{on}}{R} = A_1 \cdot \ln\left(1 + \frac{t}{\tau}\right) + A_2 \cdot \ln\left(1 + \frac{t}{\gamma\tau}\right)$$

$$\tau = \frac{\alpha \cdot W}{I_D} \cdot \frac{\phi_b}{E_m \lambda} e^{\frac{\phi_b}{E_m \lambda}}$$



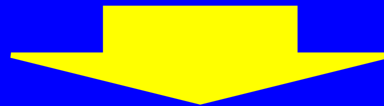
Electric field distribution of n-channel LDMOS [2]



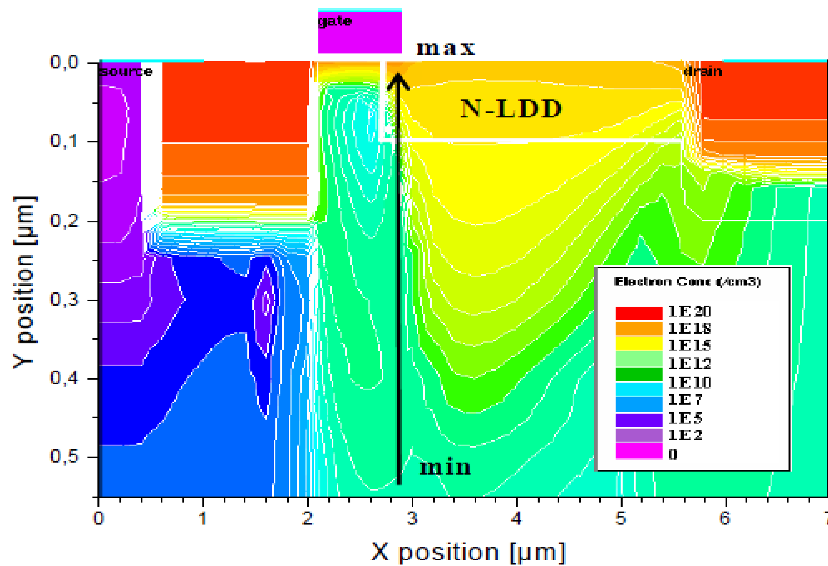
Referred by "An LDMOS hot carrier model for circuit reliability simulation"

Problems of the Referred Model

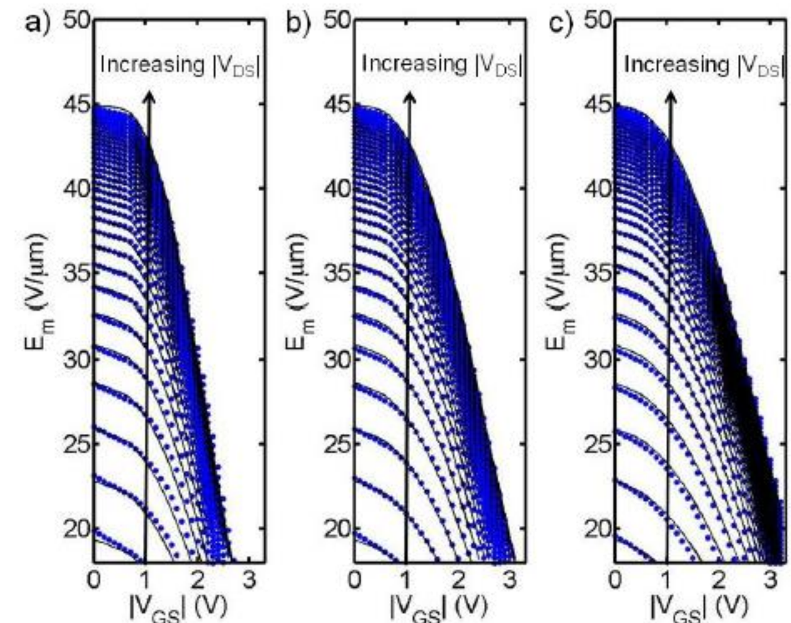
The maximum electric field is fitting functions, so far



We developed maximum electric field model equations



Electric field distribution of n-channel LDMOS [2]



Peak electric field of n-channel LDMOS [4]

Maximum Electric Field Function Equation

Function Eq.

$$E_m = A \cdot \exp[-\exp(-z) - z + 1]$$

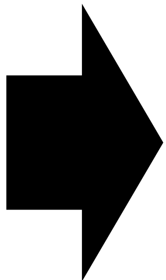
Amplitude

$$A = \alpha \frac{(V_{DS} - V_{DSAT})}{L_{eff}}$$

Peak location

$$z = \frac{(V_{GS} - V_{TH} - V_{GS_max})}{\beta}$$

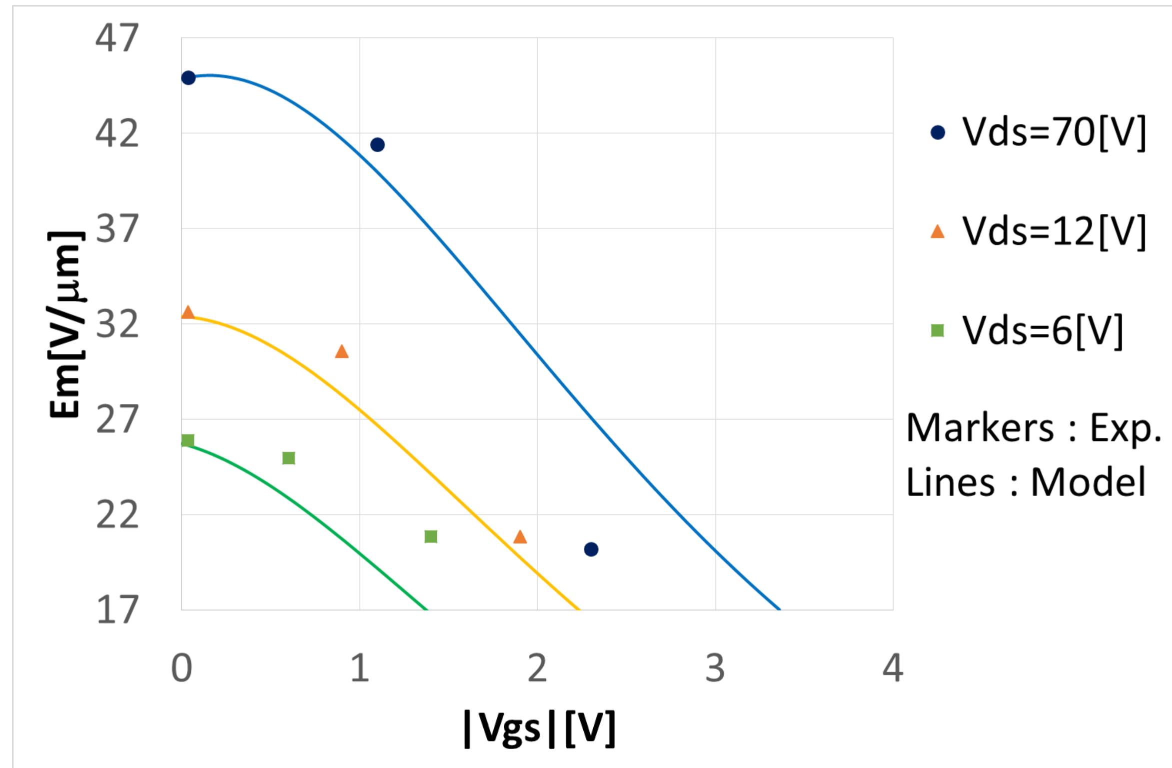
α , β : fitting parameter, V_{GS_max} : maximum V_{GS}, V_{TH} : threshold voltage



- Lateral electric field depends on Vds
- Flexible peak value and location

Function Model Evaluation

Comparison between simulation and proposed function model



- The peak value of electric field agrees with T-CAD simulation
- The shape of calculated curves is close to T-CAD simulation

OUTLINE

- Introduction
- Our Research
  - HCI Degradation Modeling
  - Maximum Electric Function Equation
- Conclusion

Conclusion

- We have characterized fresh and stressed n-channel LDMOS with measurement and simulations.

- We have derived the maximum electric field model equations and demonstrated the effectiveness.

References

[1]HiSIM-HV 2.2.0 User's manual
[2] M.A.Belaid and K.Ketata :"Hot-Carrier Effects on Power RF LDMOS Device Reliability" EDA Publishing THERMINIC 2008
[3] N. Soin.S.S.Shahabudin and K.K.Goh, et al,: "Measurement and Characterization of Hot Carrier Safe Operating Area (HCI-SOA) in 24V n-type Lateral DMOS Transistors",10th IEEE International Conference on Semiconductor Electronics, pp.659-663 (2012)
[4] Guido T. Sasse, Jan A.M.Claes and Bart Dev Vries : "An LDMOS hot carrier model for circuit reliability simulation" (2014)

Thank you for your kind attention

謝謝

Q & A

- 発表に使っているLDMOSのプロセスはどこのものか
  → 論文のデータなので、詳細は不明です

- 電界モデルは、SPICEに入れる予定なの？
  （のようなことを聞かれたと思う）
  →今後の課題として取り組みます。
  （上手く伝わりませんでした）