A Study on HCI Induced Gate Leakage Current Model Used for Reliability Simulations in 90nm n-MOSFETs

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Outline

- Research Background
- Purpose of This Work
- Conventional HCI degradation model
- Model Derivations
- Measurement and Model Verifications
- Summary and Future Research

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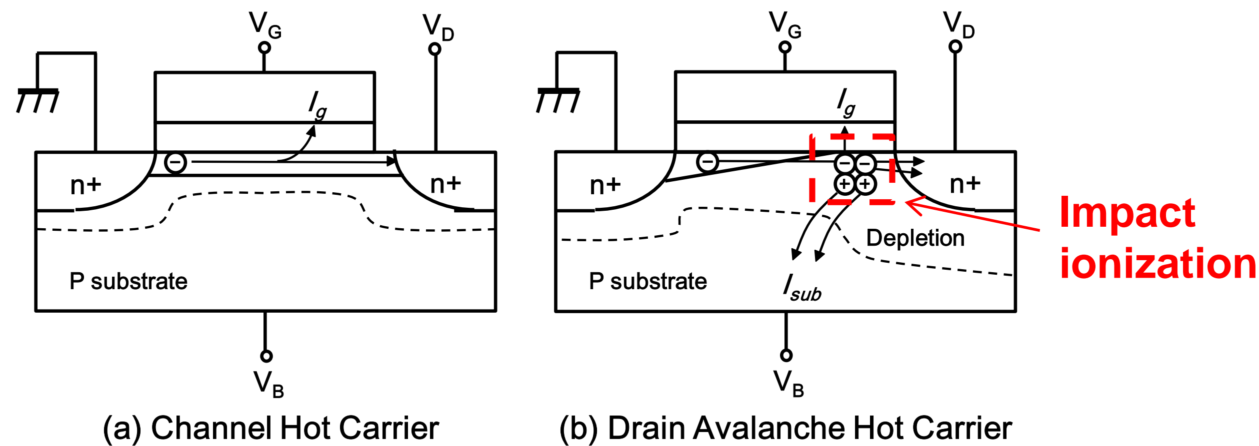
Research Background(1)

- There is an increasing interest
  in the reliability issues of CMOS transistors.
- Especially, HCI degradation is
  the most important phenomenon
  in high electric fields.
- Reliability simulation using the degradation models
  is needed in order to develop
  robust analog and digital CMOS LSI designs.

Research Background(2)

- CHC: Channel Hot Carrier ($V_G=V_D$)
- DAHC: Drain Avalanche Hot Carrier ($V_G<V_D$)
  - a large amount of hot electrons is injected more than in the CHC phenomenon



(a) Channel Hot Carrier (b) Drain Avalanche Hot Carrier

Two different hot carrier injection mechanisms

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Purpose of This Work

- To develop
  HCI degradation model of n-MOSFETs
  that is not dependent on the structure.
- To develop parameter extraction method for the proposed model with 90nm n-MOSFETs.
- To implement the proposed model
  into BSIM4 source codes of our MDT-SPICE
  (SPICE3 fully compatible simulator).

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Conventional HCI Degradation Model

- Hu model

HCI is expressed in terms of the number of generated interface states ΔN_{it}

$$\Delta N_{it} = C_1 \left[t \frac{I_{DS}}{W} \exp\left(-\frac{\phi_{it}}{q \lambda E_m} \right) \right]^n$$

- E_m is difficult to obtain accurately with analytical models
- HCI stress is conventionally monitored as a function of the substrate current I_{sub}

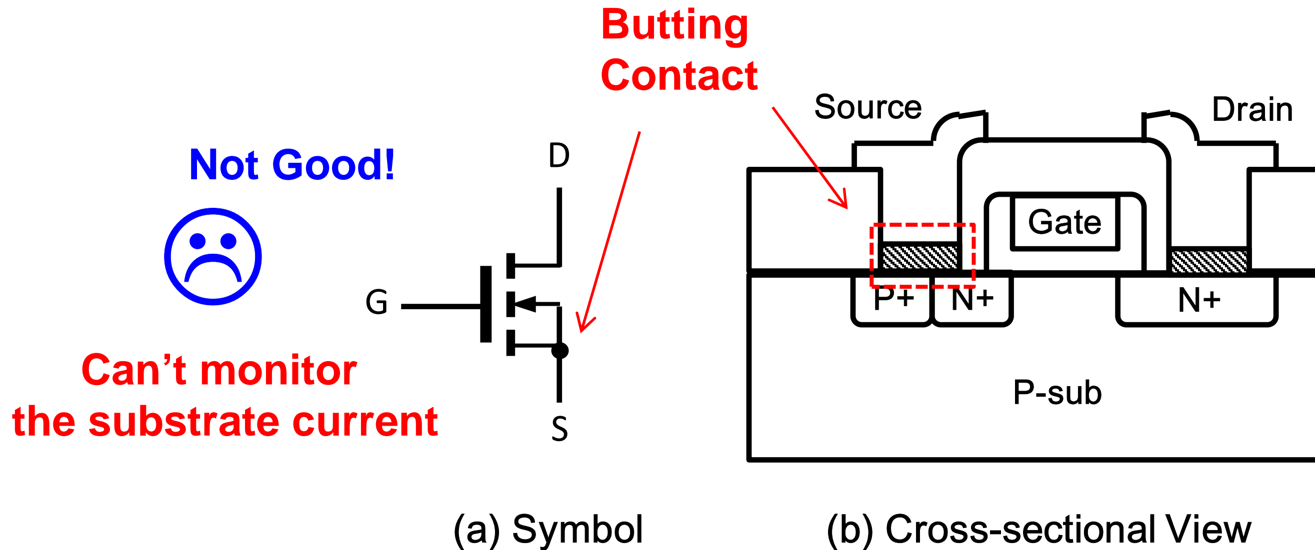
$$\Delta N_{it} = C_2 \left(\frac{I_{sub}}{W} \right)^{\alpha} t^n$$

ΔN_{it} changes the threshold voltage (V_{th}) and the carrier mobility (μ)

$$V_{th} = V_{th0} + \frac{q \Delta N_{it}}{C} \qquad \mu = \frac{\mu_0}{1 + \beta \Delta N_{it}}$$

Disadvantage of I_{sub} Model

- Conventional models cannot be applied for any circuit simulations without using the substrate terminal

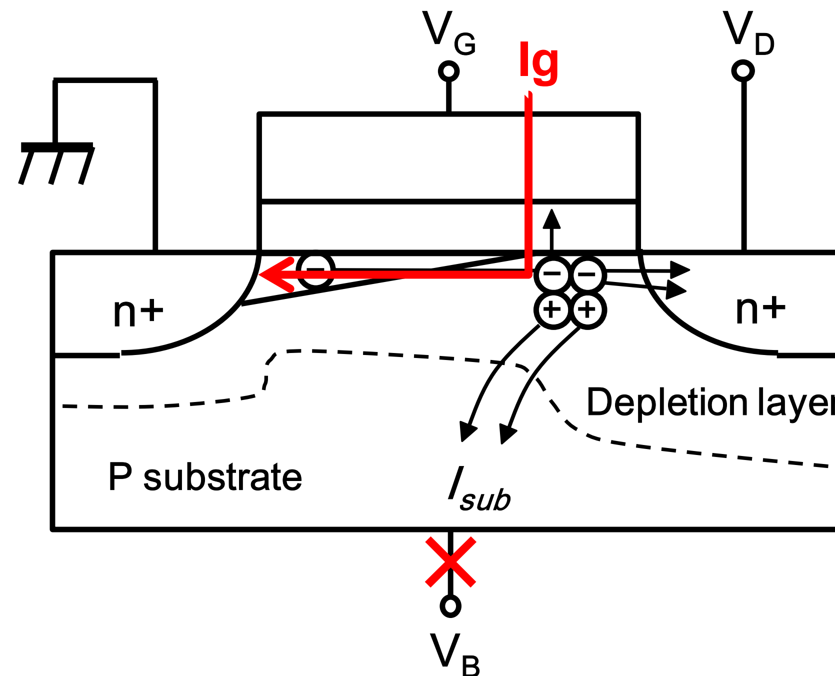


(a) Symbol (b) Cross-sectional View

An n-MOSFET with Butting Contact structure

Concept of Proposed Model

- The proposed model is an attempt to extract the HCI current from the gate terminal



HCI induced Gate Leakage Current Model

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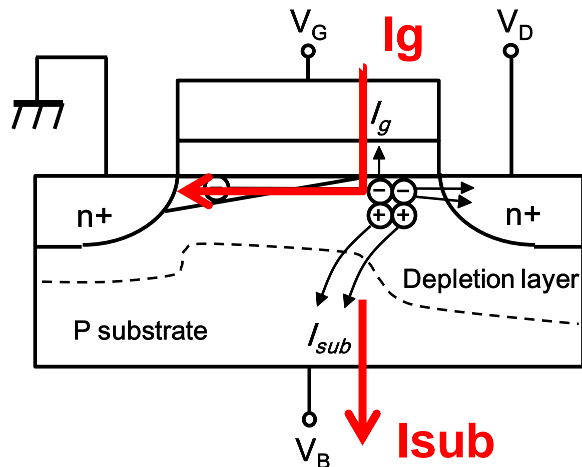
Model Derivations(1)

The gate and substrate currents in HCI model by Chenming Hu are written as

$$I_{sub} = C_1 I_{ds} e^{\frac{-\varphi_i}{q\lambda E_m}} \qquad \textbf{(1)}$$

$$I_g = C_2 I_{ds} e^{\frac{-\varphi_b}{q\lambda E_m}} \qquad \textbf{(2)}$$



I_g depends on the probability of electrons which traverse the Si-SiO_2 interface

I_{sub} depends on the probability of the occurrence of impact ionization

Model Derivations(2)

BSIM4 model supports substrate current induced body effect (SCBE) caused by the impact ionization effect as

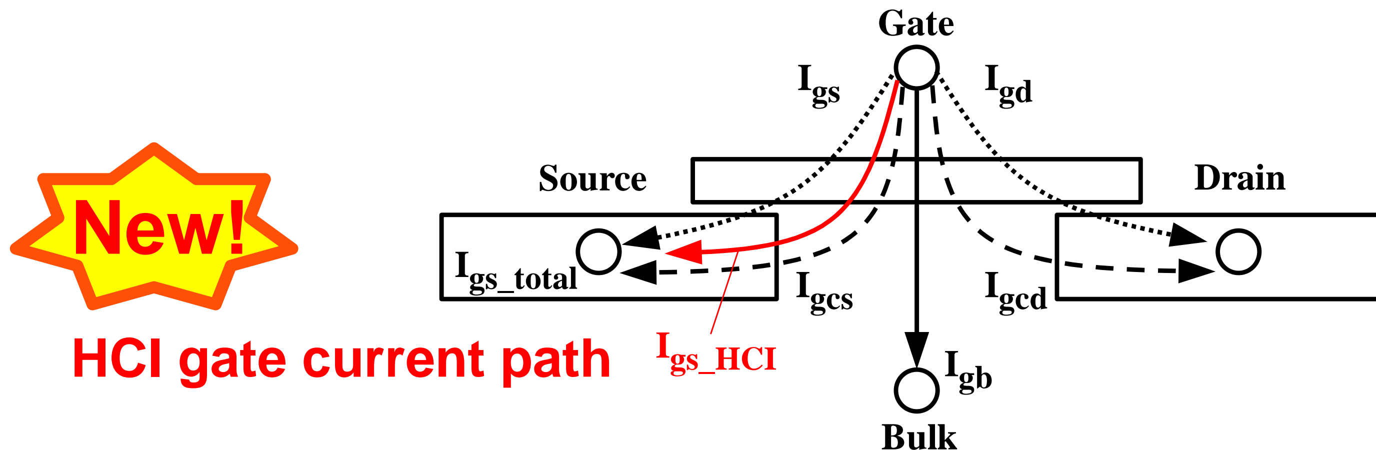
$$I_{sub} = \frac{A_i}{B_i} I_{ds}(V_{ds} - V_{dsat}) e^{\frac{-B_i \cdot litl}{V_{ds} - V_{dsat}}} \quad \textbf{(3)}$$

To modify the ionization ratio between the substrate and the gate currents, the gate current due to HCI is simply written in eq. (4) as referred to eqs. (1) and (2)

$$I_{gs_HCI} = \frac{GA_i}{GB_i} I_{ds}(V_{ds} - V_{dsat}) e^{\frac{-GB_i \cdot litl}{V_{ds} - V_{dsat}}} \quad \textbf{(4)}$$

Model Derivations(3)

Gate Direct Tunneling Current Model in BSIM4



I_{gb}, I_{gd}, I_{gcd} are modeled in advance

Model parameters, GAi and GBi are extracted with eqs. (4) and (5)

$$I_{gs_HCI} = I_{gs_total} - I_{gs} - I_{gcs} \tag{5}$$

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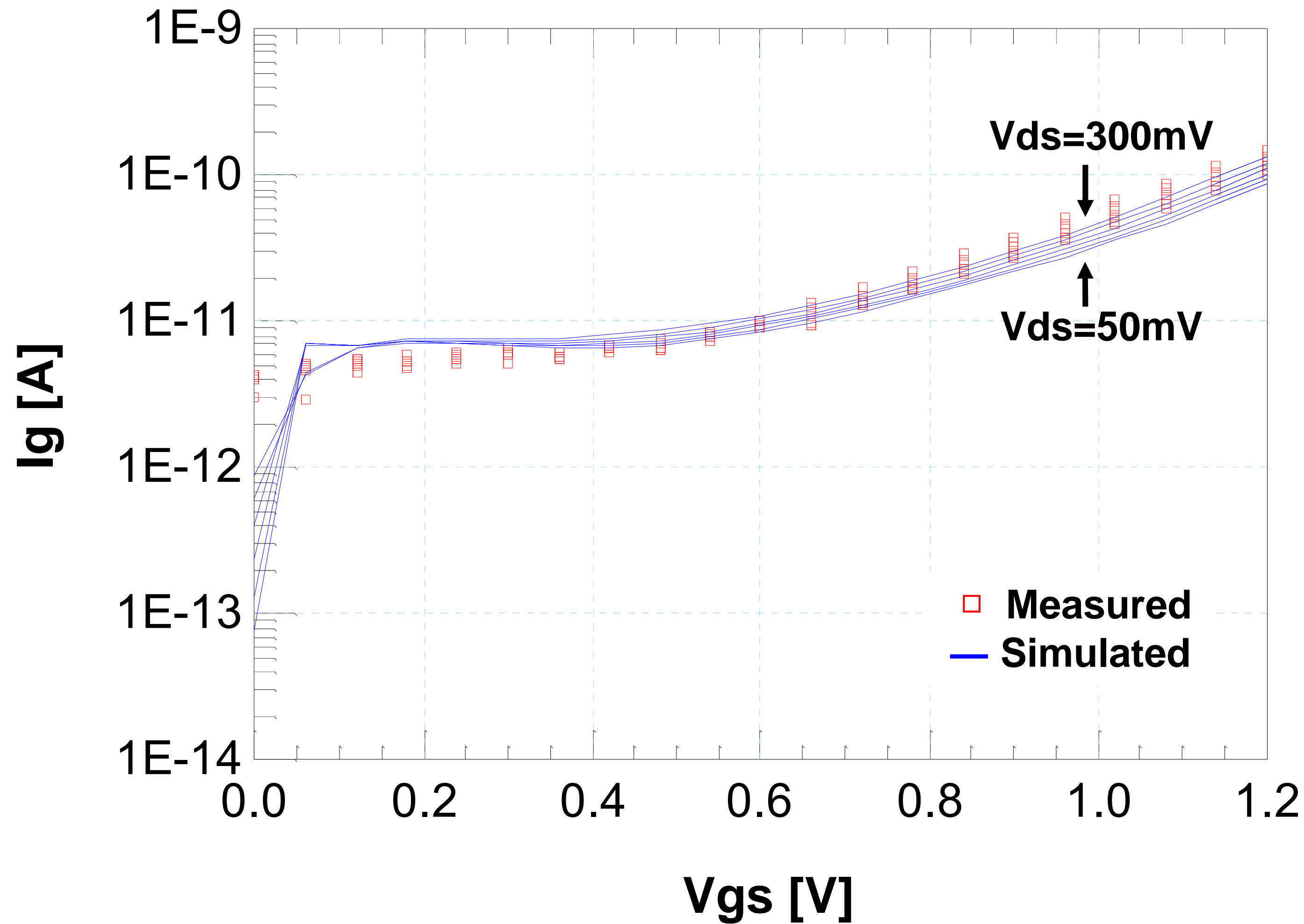
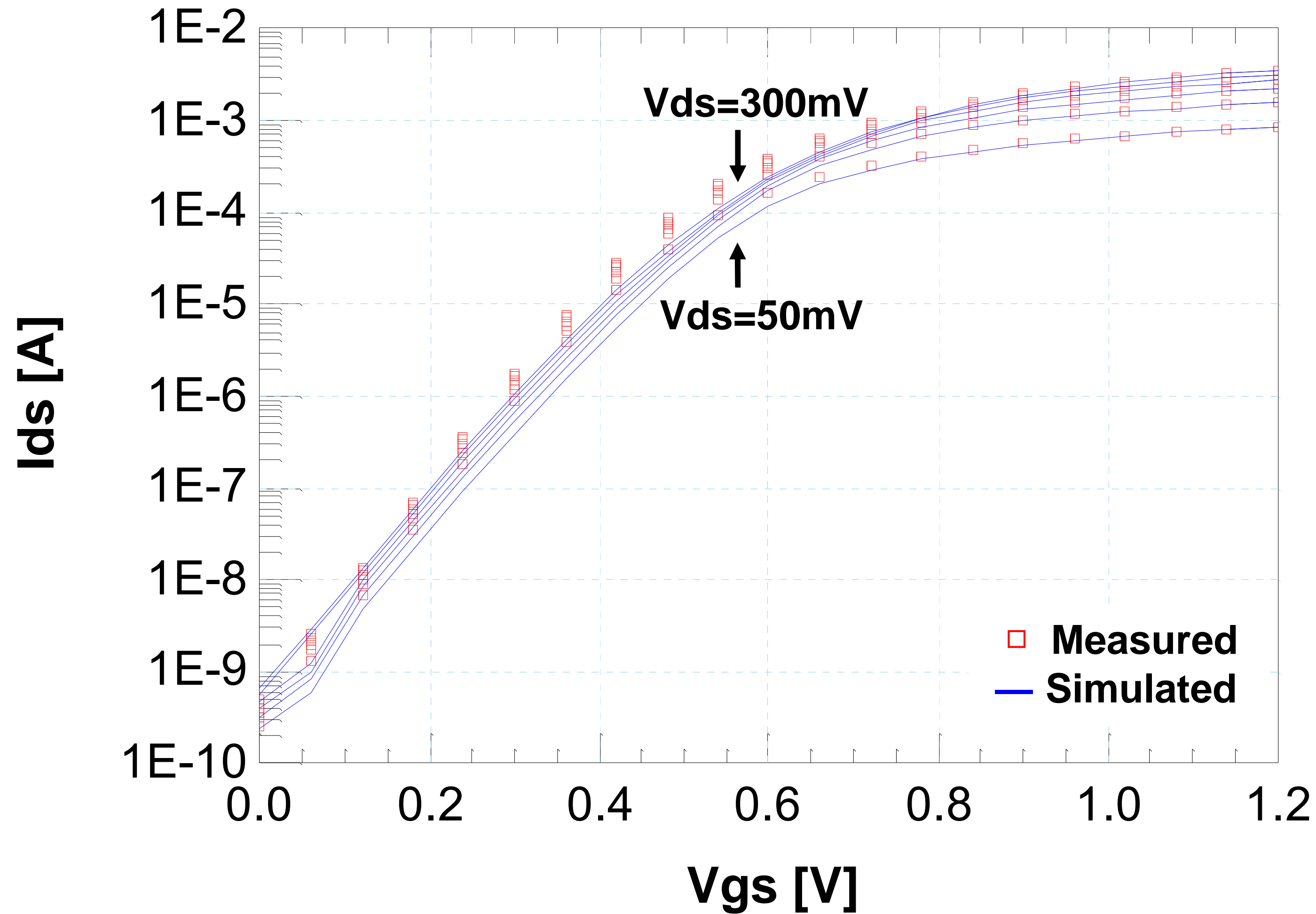
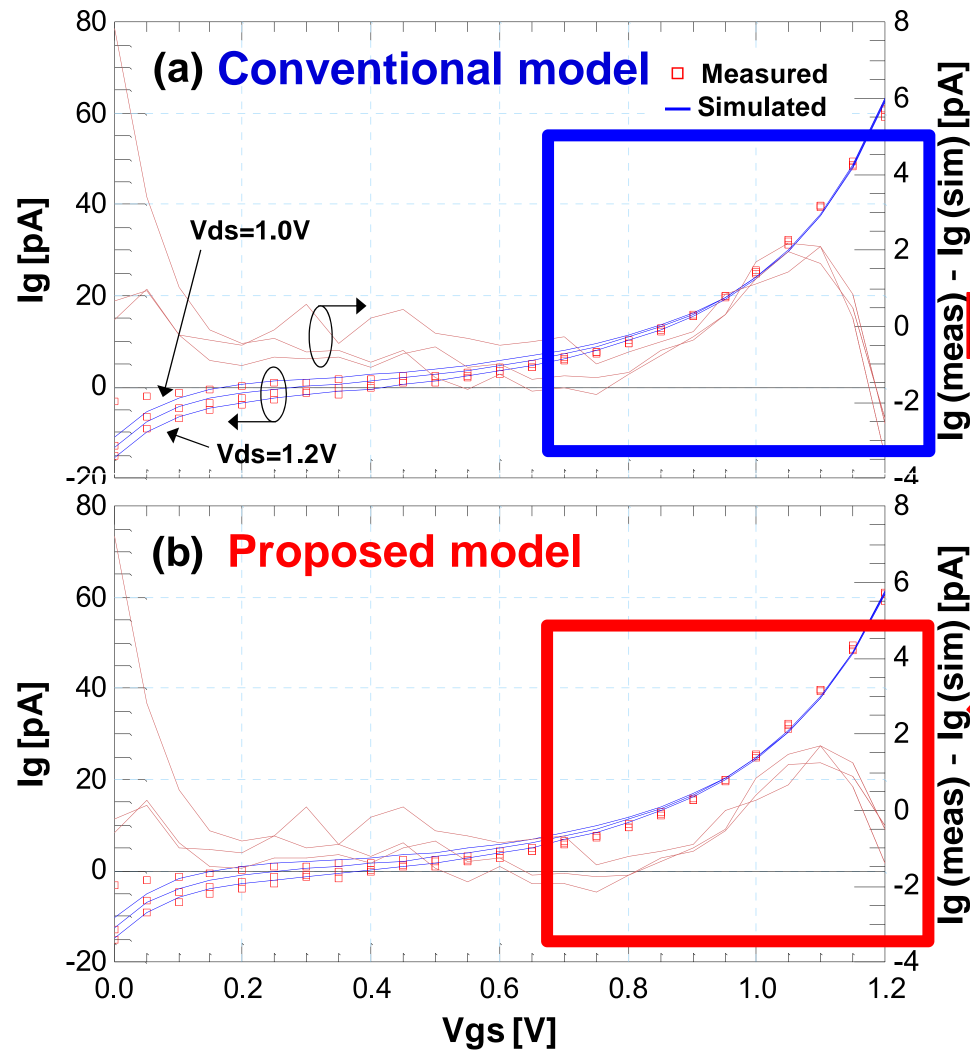
Characteristic of Gate Leak Current Under Non-HCI Condition



Characteristic of Drain Leak Current Under Non-HCI Condition



Characteristic of Total Gate Leak Current Under HCI Condition



Simulation accuracy is improved in the region of drain avalanche HCI phenomena (Vgs=1/2Vdd~Vdd)

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Summary

- We presented a new model and its extraction method to estimate the HCI current from the gate terminal without using the substrate terminal
- Simulation with the proposed model accurately agreed with 90 nm n-MOSFET measurements under the HCI conditions.
- It is also found that HCI induced gate leakage current is so small (few pico-amps) that

  accurate measurement is not easily performed

Future Research

- We continue this work
  to complete the degradation model
  to be used in EDA environments
- We will also focus on reliability modeling
  for high power MOSFETs

質疑応答

- 質問1
  - なぜ90nmのプロセスを選んだのか？
- 回答1
  - 選んだわけではない。90nmの試作チャンスを得たので90nmになった。
- 質問２
  - 90nmプロセス以外にもこの方法は有効か？
- 回答２
  - 提案モデルは他のプロセスにも応用可能。
    しかし、HCIのゲート電流は小さいので、正確に測定することは容易ではない。