A Study on HCI Induced Gate Leakage Current Model Used for Reliability Simulations in 90nm n-MOSFETs

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Abstract

In this paper, we propose a Hot Carrier Injection (HCI) induced gate leakage current model used for reliability simulations in 90nm n-channel MOSFETs (n-MOSFETs). As far as we have investigated, existing papers and reports regarding on HCI degradation model equations are based on the substrate current induced by the impact ionization effect. These degradation models cannot be applied for any circuit simulations without using the substrate terminal of n-MOSFETs. Since the proposed model and extraction method estimate the HCI current from the gate terminal, substrate terminals of n-MOSFETs are not necessary for simulating degradations in any circuit. The proposed HCI gate leakage model is implemented in BSIM4 source codes of our SPICE3 fully compatible simulator (MDT-SPICE). Model parameters including BSIM4 and our models are accurately extracted with DC current measurements of 90nm n-MOSFETs. It is confirmed that the proposed model showed more accurate gate current simulations than BSIM4 model comparing with the measurement of the gate current.

1. Introduction

In recent years, CMOS integrated circuits are used in many electronic devices, and are realized as core function of the electronic devices in many cases. Therefore, high reliability is the key specification for CMOS integrated circuits. There is an increasing interest in the reliability issues of CMOS transistors in accordance with the recent advanced process technology. Especially, HCI degradation is the most important phenomenon in high electric fields. For this reason, reliability simulation using the degradation models is needed in order to develop robust analog and digital CMOS integrated circuit designs.

There are two major effects in the degradation of n-MOSFETs. One is the Positive Bias Temperature Instability (PBTI), which arises from positive voltage stress for a long time. The other is the HCI, which arises from high drain currents in saturation region. We focus on HCI phenomenon for our characterizations because it is more dominant than PBTI especially in analog circuit design.

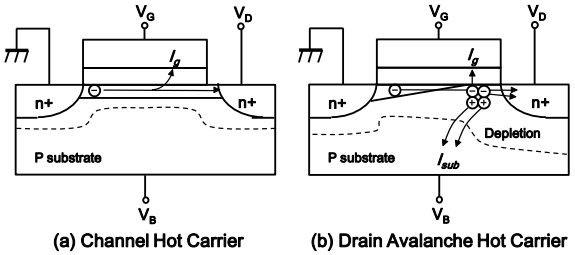

Fig. 1. Schematics of the HCI mechanism in n-MOSFETs: (a) channel hot carrier; (b) drain avalanche hot carrier.

In this study, our goal is to develop the HCI degradation model of n-MOSFETs that is not dependent on the structure. The proposed model is an attempt to extract the HCI current from the gate terminal and it is implemented in BSIM4 source codes of our SPICE3 fully compatible simulator (MDT-SPICE) [1]. Model parameters including BSIM4 and our models are accurately extracted with DC current measurements of 90nm n-MOSFETs.

The organization of the paper is as follows: Section II presents the basic HCI mechanism and conventional HCI degradation model. Problems of the conventional HCI degradation model are also described. Section III presents our proposed model and the HCI induced current extraction method. Section IV discusses the measurement and simulation results, and the paper summarizes in Section V.

2. Conventional HCI degradation models

In general, there are two different hot carrier injection mechanisms [6] in an n-MOSFET: channel hot carrier (CHC) injection, drain avalanche hot carrier (DAHC). The mechanism of each mode is shown in Fig.1. When the gate voltage is approximately equal to the drain voltage, the CHC injection effect is at its maximum. So-called ‘lucky electrons’ gain sufficient energy to surmount the Si/SiO_2 barrier at the drain end of the channel, without losing energy due to collisions with atoms in the channel (see Fig. 1(a)). At stress conditions with high drain voltage and low gate voltage, electron-hole pairs can be created due to impact

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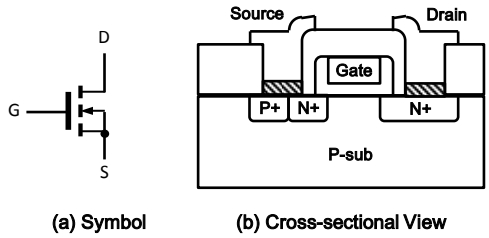

Fig. 2. Butting contacted n-MOSFET structures.
(a) the circuit symbol; (b) the cross sectional view.

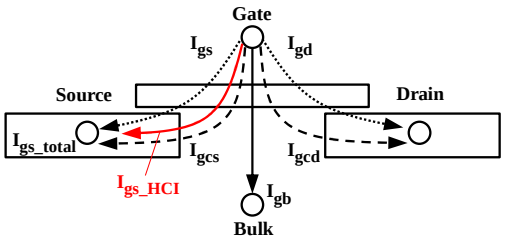

Fig. 3. Basic concept of the gate leakage current flow.

ionization of the channel current near the drain terminal. Each of these electrons and holes can then accelerate in trapped the channel electric field and can potentially surmount the Si/SiO_2 barrier to get trapped or to create interface state. This phenomenon is known as avalanche multiplication and results in drain avalanche hot carrier generation (DAHC) (see Fig. 1(b)). Additionally, some of the generated carriers lead to a bulk current. The DAHC injection mechanism causes the most stringent device degradation because a large amount of hot electrons are injected into the gate oxide at the same time.

Most HCI compact models available in literature are based on the 'lucky electron' model (LEM) by Shockley. The concept was first introduced by Shockley in 1961 to explain bulk phenomena and later became very popular as the underlying mechanism in a lot of HCI models. Chenming Hu was one of the first to introduce a HCI model based on the lucky electron concept [2]. Most of recently published HCI models are based on the same theory. In this model, HCI is expressed in terms of the number of generated interface states ΔN_{it}:

$$\Delta N_{it} = C_1 \left(t \frac{I_{ds}}{W} e^{\frac{-\varphi_{it}}{q\lambda E_m}} \right)^n , \qquad (1)$$

where I_{ds} is the drain-source current, q is the electric charge, E_m is the peak lateral electric field, φ_{it} is the critical energy for electrons to create an interface trap, λ is the hot-electron mean-free path, W is the transistor channel width, t is the stress time, C_1 and n are the process-dependent constants, respectively. In Eq. (1), E_m is the most important parameter, but it is difficult to obtain accurately with an analytical model. Therefore, especially in earlier models, HCI stress is typically captured as a function of the substrate current I_{sub}:

$$\Delta N_{it} = C_2 \left(\frac{I_{sub}}{W} \right)^{\alpha} t^n , \qquad (2)$$

where C_2, α, and n are the process-dependent constants, respectively. Eventually, the number of generated interface states, can be related to a shift in transistor parameters such as the threshold voltage V_{th} and the carrier mobility μ [5]:

$$V_{th} = V_{th0} + \frac{q\Delta N_{it}}{C_{ox}} \quad \text{and} \qquad (3)$$

$$\mu = \frac{\mu_0}{1 + \beta \Delta N_{it}} , \qquad (4)$$

where C_{ox} is the oxide capacitance per unit area, V_{th0} and μ_0 are the threshold voltage and carrier mobility for an unstressed transistor respectively, β is a process dependent parameter.

However, these degradation models cannot be applied for any circuit simulations without using the substrate terminal of n-MOSFETs such as structure of shown in Fig.2. Therefore, in this paper, we propose a new model and the extraction method to estimate the HCI current from the gate terminal. Substrate terminals of n-MOSFETs are not necessary for simulating degradations in any circuit with the model.

3. HCI induced gate leakage current model

The gate current and the substrate current in HCI model by Chenming Hu are expressed as follows [3]:

$$I_{sub} = C_1 I_{ds} e^{\frac{-\varphi_i}{q\lambda E_m}} \quad \text{and} \qquad (5)$$

$$I_g = C_2 I_{ds} e^{\frac{-\varphi_b}{q\lambda E_m}} , \qquad (6)$$

where φ_i is the minimum energy that a hot electron must have in order to create an impact ionization, φ_b is the barrier energy at the $Si\text{-}SiO_2$ interface, and C_1 and C_2 are process-dependent constants, respectively. Since the substrate current depends on the probability of the occurrence of impact ionization, the gate current is dependent on the probability of electrons which traverse the $Si\text{-}SiO_2$ interface. Difference between the Eqs (5) and (6) is the difference of probability. BSIM4 model is employed to obtain accurate gate leakage current simulations. The model supports substrate current induced body effect (SCBE) caused by the impact

ionization effect as shown in the following equation [4]:

$$I_{sub} = \frac{A_i}{B_i} I_{ds}(V_{ds} - V_{dsat}) e^{\frac{-B_i \cdot litl}{V_{ds} - V_{dsat}}}, \qquad (7)$$

where parameters, A_i and B_i, are extracted with measurement, V_{ds} is the drain-source voltage, V_{dsat} is the saturation voltage, and *litl* is the characteristic drain field length, respectively. To modify the ionization ratio between the substrate and the gate currents, the gate current due to HCI is simply written in Eq. (8) as referred to Eqs (6) and (7).

$$I_{gs\_HCI} = \frac{GA_i}{GB_i} I_{ds}(V_{ds} - V_{dsat}) e^{\frac{-GB_i \cdot litl}{V_{ds} - V_{dsat}}}. \qquad (8)$$

Fig. 3 shows the gate leakage current flow when HCI effect is occurred. The HCI gate current path is newly added to the gate leakage current model of BSIM4 [4]. Assuming that the gate leakage current flows only source side under the HCI condition ($V_{DS} \cong V_{DD}$) and the gate-to-bulk leakage current (I_{gb}) is negligible because sufficiently small in comparison to other leakage current in Fig.2, Model parameters, GA_i and GB_i are extracted with Eq. (9).

$$I_{gs\_HCI} = I_{gs\_total} - I_{gs} - I_{gcs}, \qquad (9)$$

where I_{gs_total} is the total gate leakage current, I_{gs} is the leakage current between gate and source, and I_{gcs} is the current between gate and source through the channel, respectively. These are obtained by static *I-V* measurements.

4. Simulation and measurements

In this experiments, the n-MOSFET, whose gate width and length are 10μm and 0.1μm, respectively, is fabricated with 90 nm CMOS process technology and then measured for parameter extractions of drain and gate leakage current models. The proposed model is implemented in BSIM4 source codes of our SPICE3 fully compatible simulator (MDT-SPICE).

Fig. 4 shows the simulation and measurement results of the gate leakage current (I_{gs} and I_{gcs}) versus gate-to-source voltage under non HCI condition. In order to consider the dependence on the drain source voltage of the gate leakage current, it is measured by varying the drain-to-source voltage in this measurement. As shown in Fig. 4, the simulation curve and the measurement results are in good agreement, including the drain source voltage dependence. This experiment yields that model parameters of a gate leakage current (I_{gs} and I_{gcs}) required to calculate the HCI current in Eq. (9).

Fig. 5 shows the simulation and measurement of the drain leakage current versus gate-to-source voltage under the same conditions as Fig. 4. We have also confirmed that the simulation and the measurement are in good agreement in the weak inversion region. As discussed above, these simulation results indicate that the model parameters of leakage current are accurately extracted with measurement in non HCI condition.

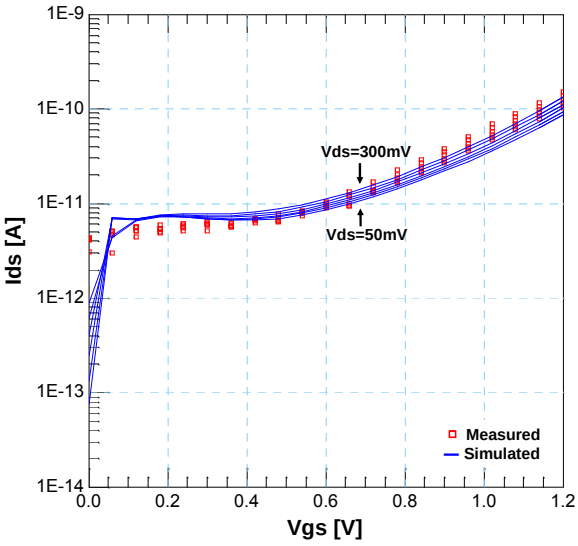

Fig. 4. Measurement and simulation results of the gate leakage current (Igs and Igcs) versus gate-to-source voltage under non HCI condition. Where, Vds is varied from 50mV to 300mV (50mV step).

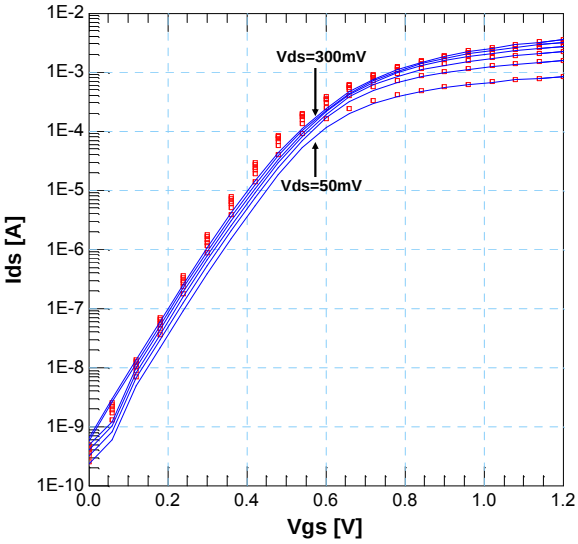

Fig. 5. Measurement and simulation results of the drain leakage current versus gate-to-source voltage under non HCI condition. Where, Vds is varied from 50mV to 300mV (50mV step).

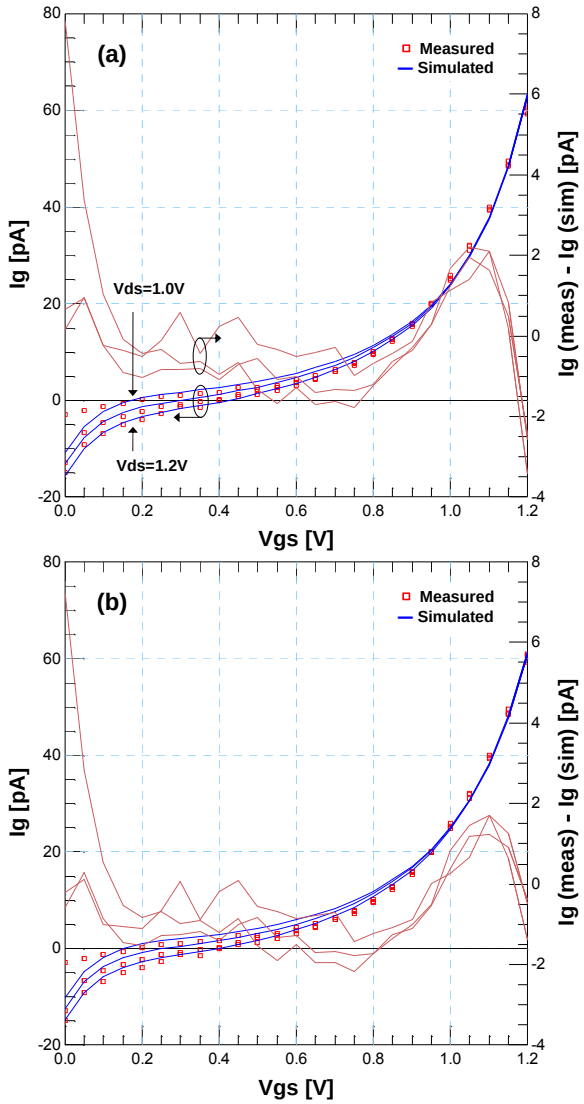

Fig. 6. Measurement and simulation results of the total gate leakage current versus gate-to-source voltage under HCI condition: (a) conventional model; (b) proposed model. Where, Vds is varied from 1.0V to 1.2V (0.1V step).

Finally, we show the simulations and measurement results of the total gate leakage current under the HCI conditions in Fig. 6(a) and Fig. 6(b). The right hand side of Y-axis in the figure shows the absolute value of the difference between the experimental results and the simulation value. Although the HCI induced gate leakage current is very small (few pico-amps), the simulation accuracy is improved in the region of occurrence of the drain avalanche HCI phenomena where V_{GS} is set from a half of *VDD* to *VDD* in the proposed model (Fig. 6(b)).

5. Summary and Future Work

In this paper, we propose an HCI induced gate leakage current model used for reliability simulations in 90nm n-MOSFETs. We presented a new model and its extraction method to estimate the HCI current from the gate terminal without using the substrate terminal. The proposed HCI induced gate leakage model is implemented in BSIM4 source codes of our SPICE3 fully compatible simulator (MDT-SPICE). Model parameters including BSIM4 and our models are accurately extracted with DC current measurements of 90nm n-MOSFETs.

The simulation with the proposed model accurately agreed with 90 nm n-MOSFET measurements under the HCI conditions. It is also found that HCI induced gate leakage current is so small (few pico-amps) that the accurate measurement is not easily performed.

The proposed model is applicable to estimate time and temperature degradations of n-MOSFETs without using the substrate terminal.

We continue this work to complete the degradation model to be used in EDA environments.

Acknowledgments

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