# Study on Maximum Electric Field Modeling Used for HCI Induced Degradation Characteristic of LDMOS Transistors

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**Abstract**

This paper reports a maximum electric field model of laterally diffused MOSFET (LDMOS) transistors under the condition of high current injection effect used for reliability simulations. LDMOSs operate under high-voltage and large-current biases, where electric field increases with biases at the gate edge. We present the investigation, formulations, and verifications of our maximum electric field model.

## 1. Introduction

Laterally Diffused MOSFETs (LDMOS) are widely used in RF applications where high voltages and large currents are supplied. The important characteristic of LDMOS is dominated by low on-resistance ($R_{on}$) in high voltages. To reduce the amount of $R_{on}$, the drift doping concentration needs to be increased as much as possible. The heavy doping concentration, leads to high lateral electric fields in the device at gate edge. Since the lateral high electric field degrades the drain channel of the device, an important issue to be considered is the time and temperature degradation of LDMOS by the hot carrier injection (HCI) effect. It is extremely convenient to predict the amount of HCI in a LDMOS before producing the device with device modeling for reliability circuit simulations.

In this paper, we study the maximum electric field model to derive hot electron life time, which is a key parameter to calculate degradation time of an n-channel LDMOS. The time and temperature degradations of an LDMOS are mainly occurred by HCI under high drain voltage in saturation region and positive bias temperature instability (PBTI) caused by self-heat and positive bias stress. In n-channel MOSFETs, including bulk MOSFETs and LDMOS devices, HCI degradation phenomenon emerges more conspicuously [1]. Therefore, we focus only on the HCI effect for our analysis of an n-channel LDMOS.

The HCI degradation of n-channel LDMOS is to increase $R_{on}$ by decreasing carriers in the drift region [2]. The increased amount of $R_{on}$ is correlate with the lateral maximum electric field of the gate edge. Because of this mechanism, it is important to predict the maximum electric field to characterize the HCI induced degradation effect. Since the maximum electric field has modeled with table-lookup fitting functions in [2], we derive the model equations with empirical formulations. In this paper, we present the investigation, formulations, and implementation of the maximum electric field model equations.

## 2. Hot Carrier Degradation

Hot electrons can be created when a high-energy photon of electromagnetic radiation strikes a semiconductor. The energy from the photon can be transferred to an electron, exciting the electron out of the valence band, and forming an electron-hole pair. If the electron receives enough energy to leave the valence band, and to surpass the conduction band, it becomes a hot electron. Such electrons are characterized by high effective temperatures. Because of the high effective temperatures, hot electrons are very mobile, and likely to leave the semiconductor and travel into other surrounding materials.

In a MOSFET and an LDMOS, when a gate is positive, and the switch is on, the device is designed with the intent that electrons will flow through the conductive channel to the drain. These hot electrons do not contribute to the amount of current flowing through the channel as intended. These carrier can cause impact ionization, and in this way, both hot holes and hot electrons are generated that can damage the device. These hot carriers can generate new interface states, or the carrier can be trapped into the oxide (it is called as lucky electron). As a result, important transistor parameters, including threshold voltage and carrier mobility [7, 8], are changed from the fresh condition of the device.

## 3. HiSIM-HV Model used for LDMOS Modeling

Fig.1 is the structure of an LDMOS. Also, Fig.2 represents the illustration of the LDMOS concept equipped in HiSIM-HV [3]. The drift region between the gate and the drain is laterally extended to endure high voltages in an LDMOS. When positive biases are supplied to the gate and drain terminals of an n-channel LDMOS, carriers are emitted out from the source to drain in drift region. Voltage is dropped in drift region. HiSIM-HV model represents the voltage drop as a variable drift resistance [3]. The $R_{drift}$ shown in Fig. 2 is

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expressed in (1) through (3):

$$R_{drift} = (R_d + V_{ds} R_{DVD}) \left(1 + \mathrm{RDVG11} - \frac{\mathrm{RDVG11}}{\mathrm{RDVG12}} V_{gs}\right)$$

$$(1 - V_{bs}\mathrm{RDVB}) \left(\frac{\mathrm{LDRIFT1} + \mathrm{LDRIFT2}}{\mathrm{DDRIFT} - W_{dep}}\right) \quad (1)$$

$$R_d = \frac{R_{do}}{W_{eff,LD} \cdot \mathrm{NF}} \left(1 + \frac{\mathrm{RDS}}{(W_{gate} \cdot 10^6 \cdot L_{gate} \cdot 10^6)^{\mathrm{RDSP}}}\right) \quad (2)$$

$$R_{d0} = (\mathrm{RD} + R_{d0,temp}) f_1 \cdot f_2 \quad (3)$$

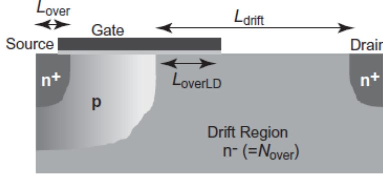


Figure 1. Cross section view of the LDMOS [3]

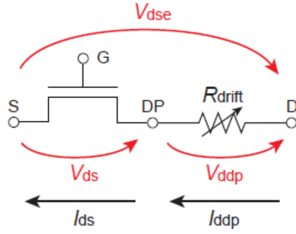


Figure 2. Illustration of the LDMOS concept equipped in HiSIM-HV [3]

## 4. Model parameter extraction and simulation

We digitized I-V characteristics in [4], and used it for measured data. Fig.3 is the cross section of the n-type LDMOS transistor used in [4]. The device is fabricated in 0.18μm process, whose length, width, gate oxide thickness are 0.4μm, 20μm, and 11.5nm, respectively.

### 4.1 $I_d$ -$V_{gs}$ measured data analysis

When we compare fresh with stressed measured drain current $I_d$ in Fig. 4, drain current decreases without increasing threshold voltage, $V_{th}$. The phenomenon is predicted that $I_d$ decreases with increasing the drain resistance and with decreasing the effective mobility. According to the observation, we take these two physical parameters into account to analyze the functions of HiSIM-HV model. Then, we choose the model parameter *RD* for degradation characteristics. Fig.4 shows fresh and stressed $I_{ds}$-$V_{gs}$ characteristic that compares between measured and simulated data after extracting model parameters with measurement. As shown in the graph, simulations agree with measured data before and after the stress. It is clear that the drift resistance parameter, *RD*, of the HiSIM-HV model represents the deterioration of drain currents.

### 4.2 $I_d$ - $V_{ds}$ measurement data analysis

When we compare fresh with stressed measured drain current in Fig. 5, drain current in the saturation region does not change. However, drain current in the pinch-off region decreases. In Fig.5 shows fresh and stressed $I_{ds}$-$V_{ds}$ characteristic that compares between measured and simulated data after extracting model parameters with measurement. *RD* has been skewed to agree with the stressed measured data from the *RD* value for fresh measured data. The resultant of stressed simulation showed poor agreement with measured data. However, it is confirmed that drain current in the saturation region does not change and only drain current in the pinch-off region decreases. As a result, it is proved that *RD* can be used for a degradation parameter in HiSIM-HV model.

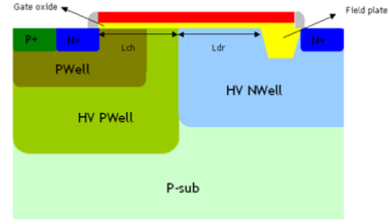


Figure 3. Cross section view of the n-type LDMOS transistor used in [4]

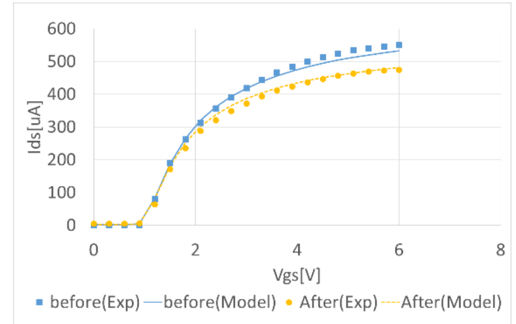


Figure 4. $I_{ds}$ -$V_{gs}$ characteristics of n-type LDMOS before and after hot-carrier induced degradation

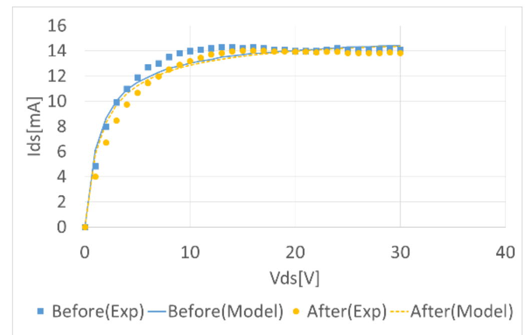


Figure 5. $I_{ds}$-$V_{ds}$ characteristics of n-type LDMOS before and after hot-carrier induced degradation

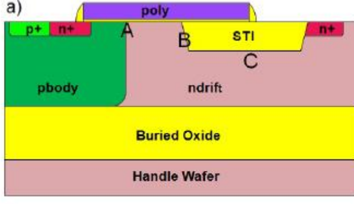


Figure 6. Cross section view of the n-type LDMOS [2]

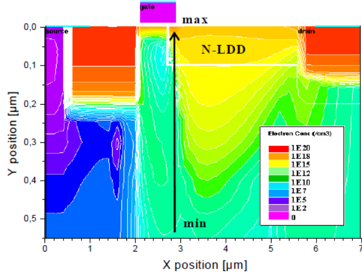


Figure 7. Electric field distribution of the n-type LDMOS [6]

## 5. Maximum electric field function model development

### 5.1 Correlation of on-resistance and electric field

The dependence on stress condition of $R_{on}$ degradation correlates with the maximum electric field [2]. The time dependence model equation of $R_{on}$ degradation is expressed in (4):

$$\frac{\Delta R_{on}}{R_{on}} = A_1 \cdot \ln\left(1+\frac{t}{\tau}\right) + A_2 \cdot \ln\left(1+\frac{t}{\gamma \cdot \tau}\right) \quad (4)$$

In this expression, parameters $A_1$, $A_2$, and $\gamma$ are device specific parameters. $t$ is the stress time. $\tau$ is characteristic time that it is a bias and geometry dependent parameter.

$\tau$ is expressed in (5):

$$\tau = \frac{\alpha \cdot W}{I_D} \cdot \frac{\emptyset_b}{E_m \cdot \lambda} e^{\frac{\emptyset_b}{E_m \cdot \lambda}} \quad (5)$$

Parameter $\alpha$ is a device specific empirical fitting parameter. $W$ is the device width, $E_m$ is the magnitude of the maximum electric field and $\emptyset_b$ is the energy needed for electrons to surmount the Si-$SiO_2$ energy barrier. Eq. (4) and (5) show that the degradation of $R_{on}$ correlates with the magnitude of the maximum electric field.

The analysis of electric field distribution by T-CAD simulations represents locations of field peaks as B in drift region [2] as shown in Fig.6. The peak electric field appears at gate edge in drift layer as shown in Fig.7 [6]. The maximum electric field has modeled with table-lookup fitting functions in [2]. Hence, it is difficult to analyze a HCI degradation phenomenon. Since the stress bias voltages dependencies of $V_{GS}$ and $V_{DS}$ on the peak electric field should be supported, we developed maximum electric field model equations.

### 5.2 Derivation of the maximum electric field

By solving 2-D Poisson's equation, the maximum electric field by HCI stress can be approximated as (6):

$$E_m(V_{DS}, V_{GS}) \approx \frac{V_{DS}-V_{DSAT}}{l_t + w_d(V_{GS})} \quad (6)$$

$V_{DSAT}$ is the potential at the pinch-off or saturation point in the channel. $l_t$ is the characteristic length. $w_d$ is the width of depletion layer which depends on $V_{gs}$.

Here, we consider reaction-diffusion (RD) model [8]. It modelled the HCI degradation in DC model of the MOSFET, which is based on 'lucky electron' model. The RD model can be used to model the hot carrier effect since traps are only generated near the drain end of the transistor and therefore recovery effect is negligible. The RD model consists of a set of two differential equations describing the generation of hydrogen particles near channel/oxide interface and their diffusion towards the gate contact. In RD model, $V_{DSAT}$ is expressed in (7):

$$V_{DSAT} = \frac{E_{sat}L(V_{GS}-V_{TH})}{E_{sat}L+(V_{GS}-V_{TH})} \quad (7)$$

$E_{sat}$ is saturation electric field. According to BSIM's formulations [7], $E_{sat}$ is written in (8):

$$E_{sat} = \frac{2v_{sat}}{\mu_{eff}} \quad (8)$$

$v_{sat}$ is the carrier saturation velocity. $\mu_{eff}$ is the effective electron mobility.

By referring to RD model, threshold voltage degradation depends on the magnitude of lateral electric field. The theory of HCI is similar in LDMOS. Combining Eq.(6) and (7), maximum electric field is expressed in (9):

$$E_m(V_{DS}, V_{GS}) \approx \frac{V_{DS}-\frac{E_{sat}L(V_{GS}-V_{TH})}{E_{sat}L+(V_{GS}-V_{TH})}}{l_t + w_d(V_{GS})} \quad (9)$$

### 5.3 Function model development

We derive the maximum electric field model equations. In Eq.(6), $w_d$ is the width of the depletion layer. Since it is difficult to calculate the depletion layer width for LDMOS structure. We propose extreme function based approach. Because the extreme function is a kind of the peak functions, it can make a peak point at any position. The maximum $V_{GS}$ ($V_{GS_max}$) where an electric field become maximum has been successfully represented with the function. $E_m$ model equation is expressed in (10) through (12):

$$E_m(V_{DS}, V_{GS}) = Ae^{(-e^{-z}-z+1)} \quad (10)$$

$$A = \alpha \frac{(V_{DS}-V_{dsat})}{L_{eff}} \quad (11)$$

$$z = \frac{V_{GS}-V_{TH}-V_{GS_max}}{\beta} \quad (12)$$

$\alpha$ and $\beta$ are fitting parameter. $A$ is the amplitude of peak value of electric field.

Because the lateral electric field depends also on $V_{DS}$ [2], the effect is implemented in Eq.(15) through (17). Proposed model equations are flexible enough to change peak value and the location.

Fig.8 shows calculation results of $E_m$ by T-CAD [6]. It is the graphs of the peak electric field at B in Fig.2. We used 65nm MOSFET process data [1] to calculate $v_{sat}$ and $\mu_{eff}$. The channel width is fixed to 40μm, and then, channel length is set to 65nm for our experiment [8]. We digitized 3 points at $V_{DS}$ = 6, 12, 70 [V] in Fig.8 and-used them for measured data to extract our model parameters. Fig.9 shows comparison result between measured and the calculated values with our model equations. As shown in graph, the peak value of the electric field agrees with measured data when we changed the bias voltages. Also, the shape of the calculated curves is close to the one for the measurement.

As a result, the developed maximum electric model equations are applicable to be implemented in any n-channel LDMOS model.

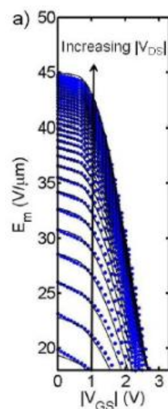


Figure 8. Peak electric field of the n-type LDMOS sample ($T_j$=233K). [2]

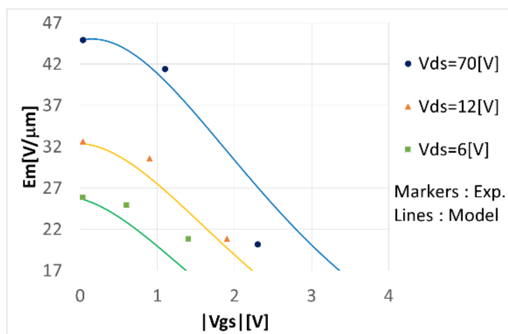


Figure 9. Comparison between measured and the proposed function model for the maximum electric field of n-channel LDMOS's

## 6. Conclusion

We have studied a hot carrier LDMOS model that can be used for circuit reliability simulation. We have investigated the HCI degradation, and then, developed the maximum electric field model equations. We have extensively characterized fresh and stressed n-channel LDMOS with measurement and simulations in static I-V. This simulation yield that the HCI degradation of n-channel LDMOS is mainly occurred by increasing $R_{on}$ because of decreasing carriers in the drift region. The increased amount of $R_{on}$ correlates with the lateral maximum electric field of the gate edge. According to the observation, we have derived the maximum electric field model equations and show the effectiveness of model equations.

The function model can be useful to implement it to any LDMOS compact model for circuit simulations.


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