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Université Pierre et Marie Curie
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Timing Measurement BOST With Multi-Bit Delta-Sigma TDC

T. Chujo, D. Hirabayashi, T. Arafune
S. Shibuya, S. Sasaki, H. Kobayashi
M. Tsuji , R. Shiota, M. Watanabe, N. Dobashi
S. Umeda, H. Nakamura, K. Sato

Gunma University, STARC, Hikari Science

群馬大学
GUNMA UNIVERSITY

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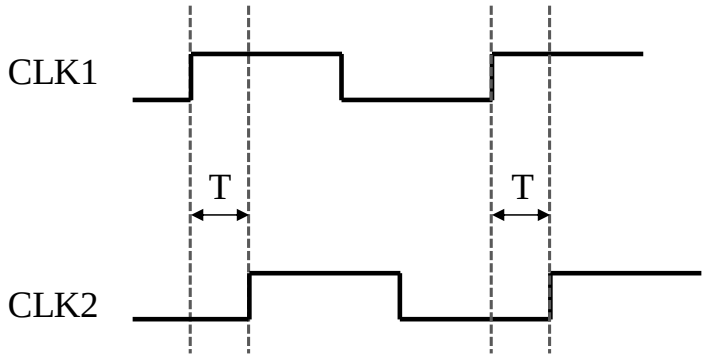
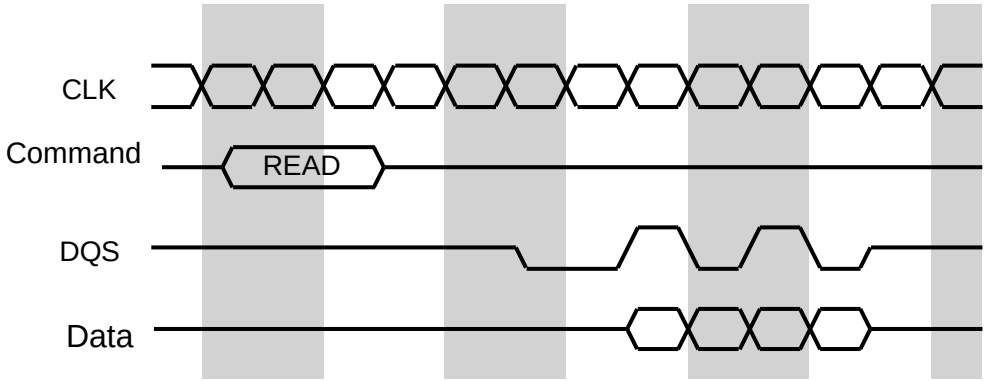
Research Objective

- Testing the timing
  between two repetitive digital signals
  Ex. Data and clock
  in Double Data Rate memory





- Short testing time
- Good accuracy

Implement BOST with small circuitry

BOST: Built-Out Self-Test

Our Work

Focus on Multi-bit ΔΣ Time-to-Digital Converter (TDC)

- Repetitive digital signals
  - ⇒ ΣΔ TDC can be used
- Simple circuit
- Fine time resolution
- Testing time
  - Single-bit ΣΔ TDC Long
  - Multi-bit ΣΔ TDC Short
- Linearity
  - Single-bit ΣΔ TDC Good
  - Multi-bit ΣΔ TDC Bad due to delay elements mismatches

⇓

For their compensation

DWA algorithm, BOST (FPGA) verification

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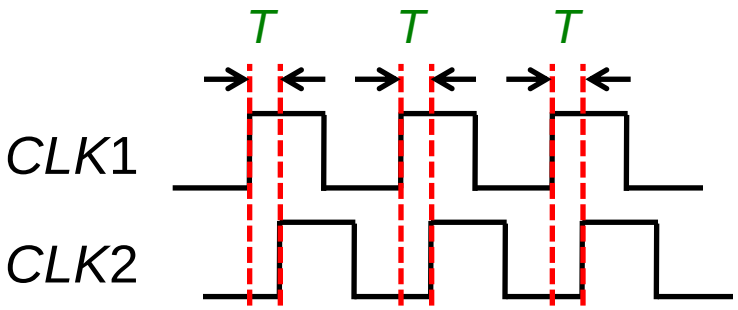
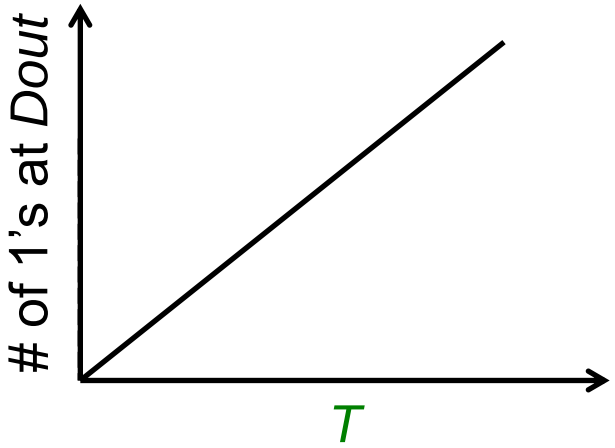
ΔΣ TDC Features

Timing *T* measurement between CLK1 and CLK2

ΔΣ Time-to-Digital Converter (TDC)

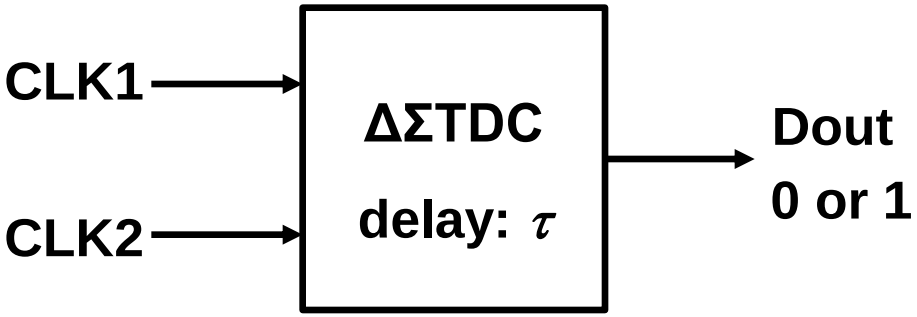


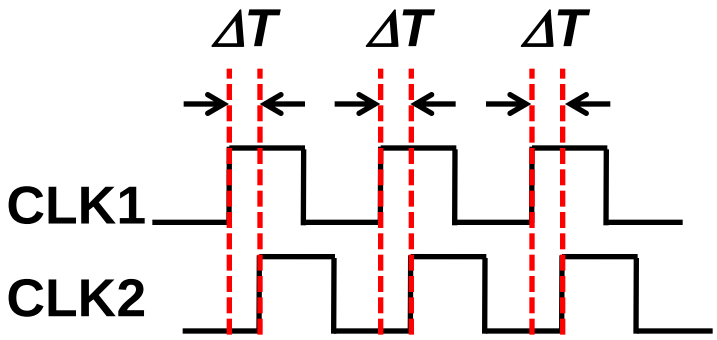


T ∝ # of 1' at *Dout*

- Simple circuit
- High linearity
- Measurement time → longer ⇒ time resolution → finer

Principle of ΔΣTDC





Dout # of 1's is proportional to ΔT

ΔT

# of 1's

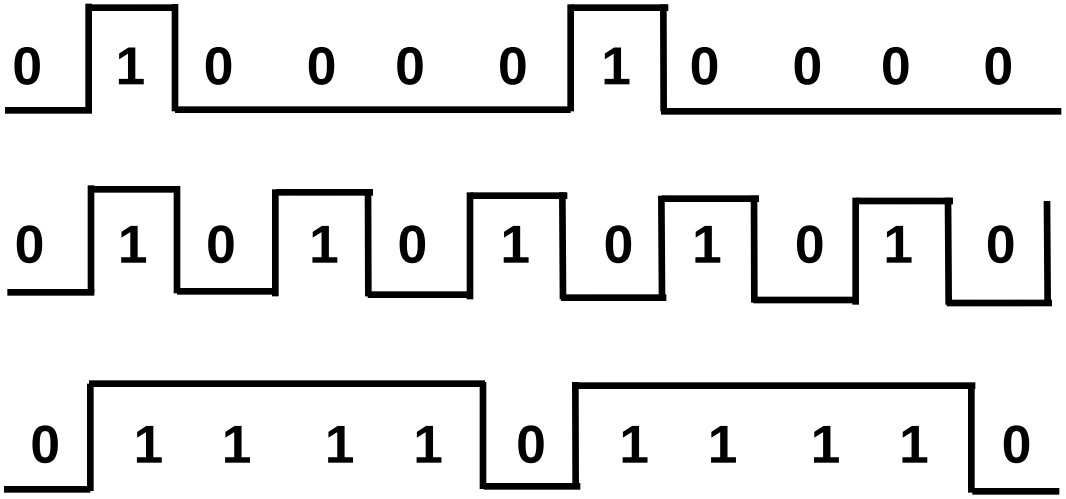
Dout

short

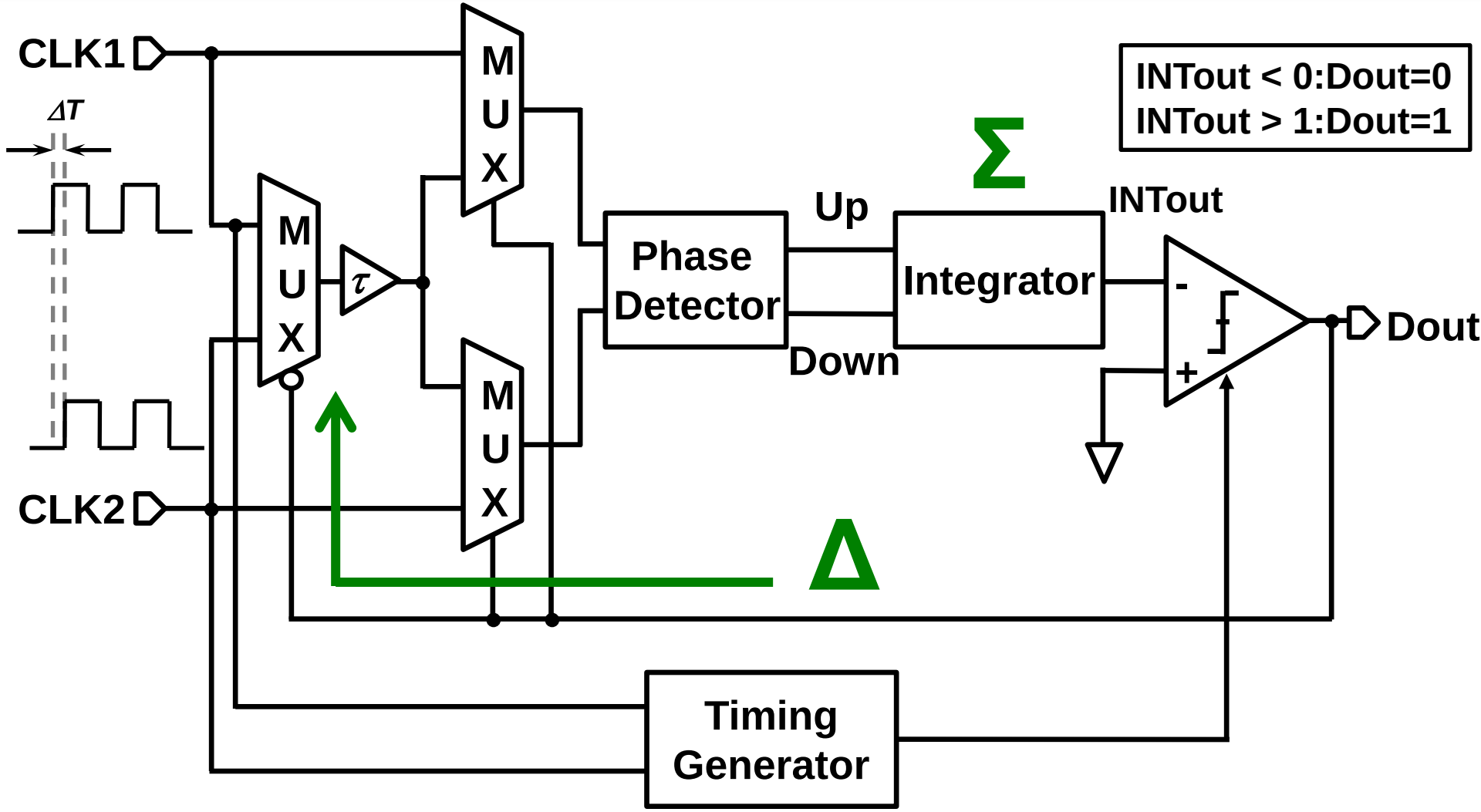
few

long

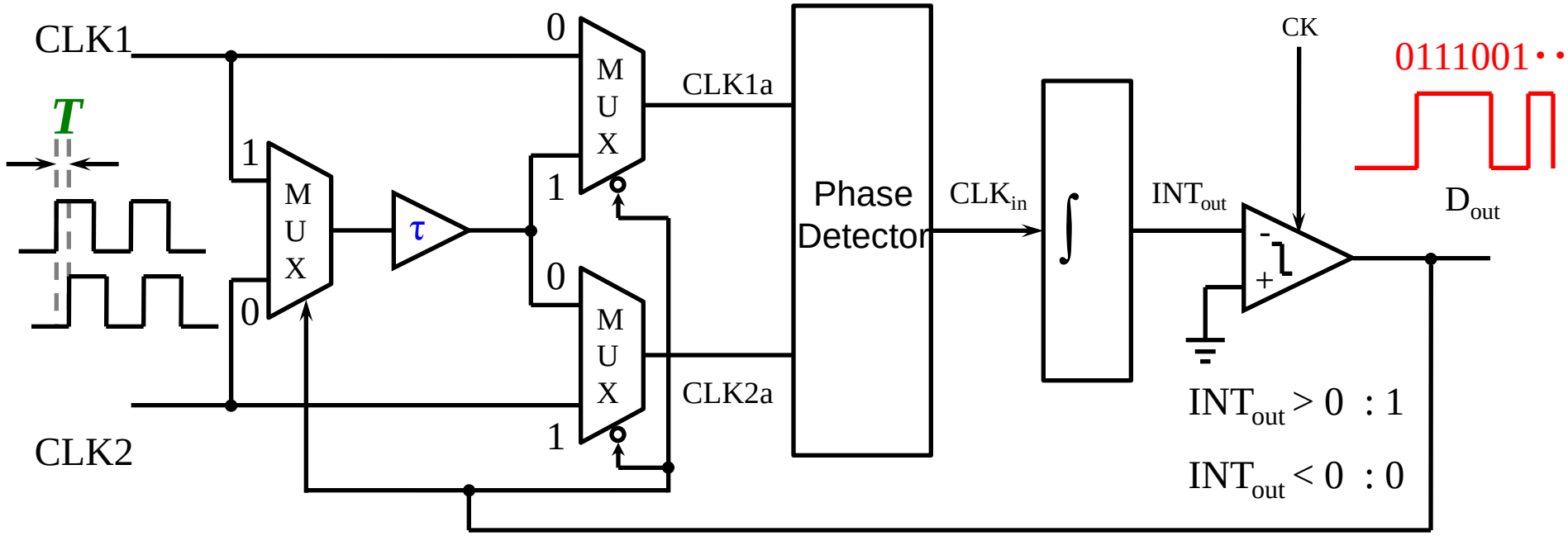
many



ΔΣTDC Configuration

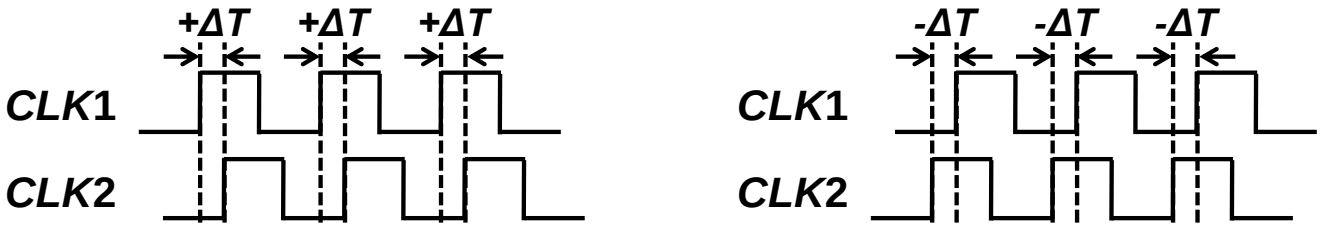


Single-Bit ΔΣ TDC



Time resolution : $\frac{2\tau}{\#\ of\ Dout \quad N_{DATA}}$

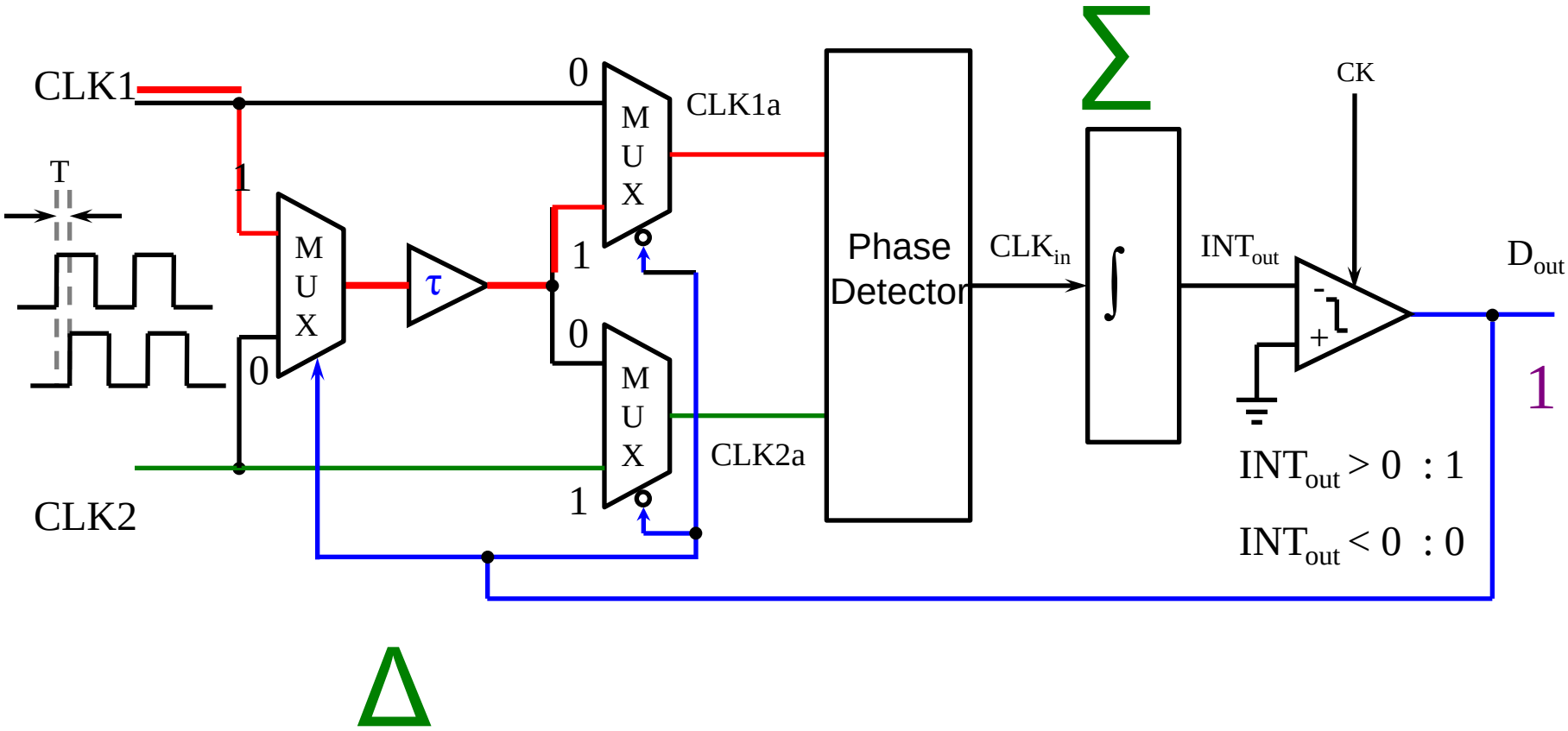
I : $-\tau < \Delta T < +\tau$



Delay line with 1bit digital input is inherently linear.

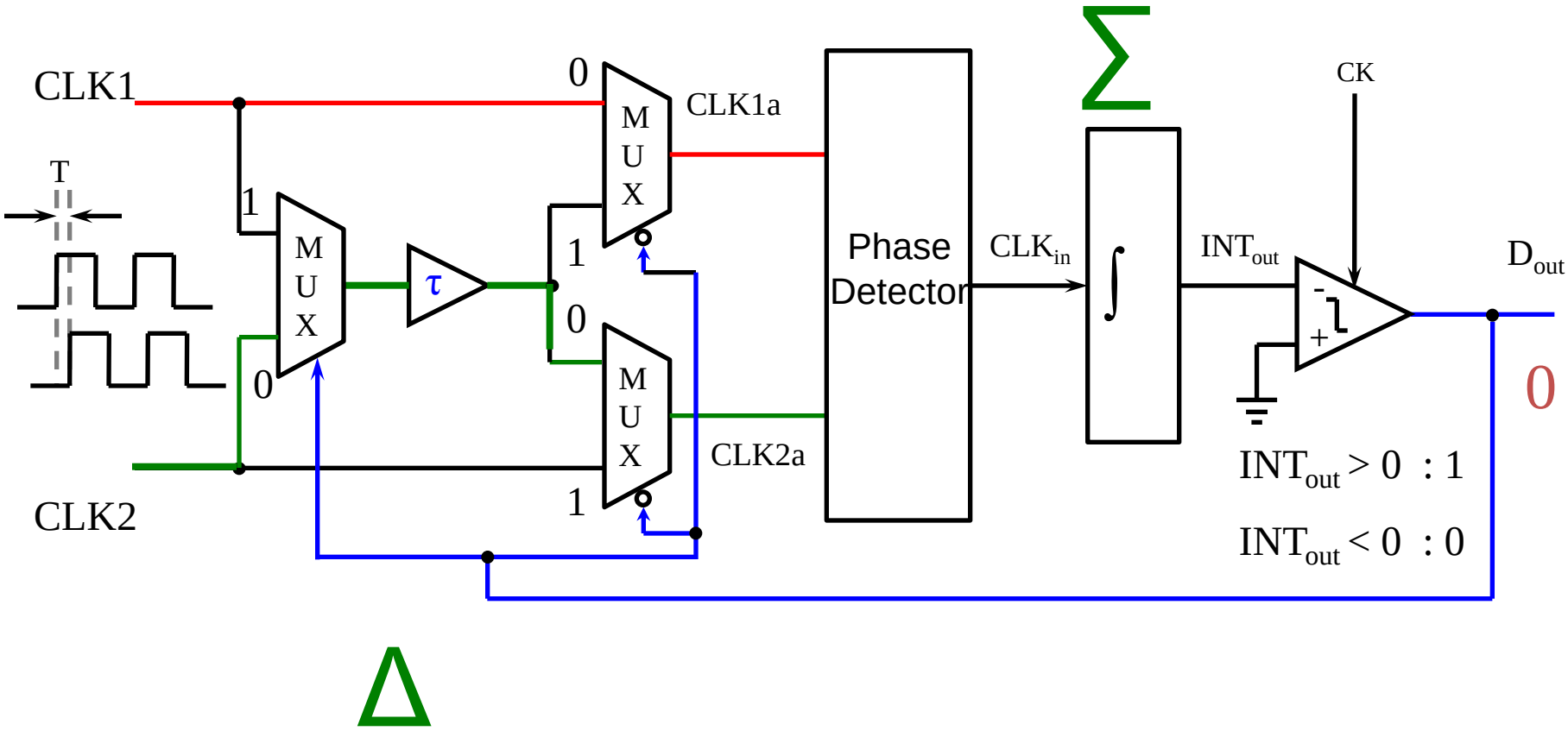
Operation of Single-Bit ΔΣ TDC

In case Dout =1



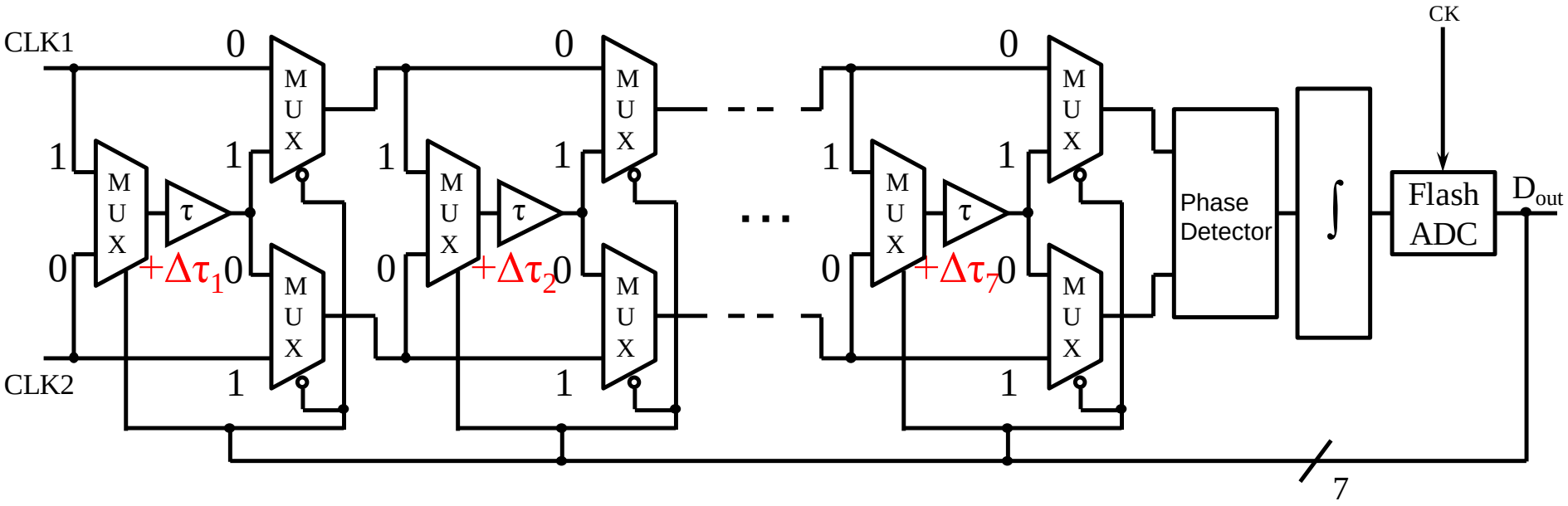
Operation of Single-Bit ΔΣ TDC

In case Dout =0



Contents

Multi-Bit ΔΣ TDC

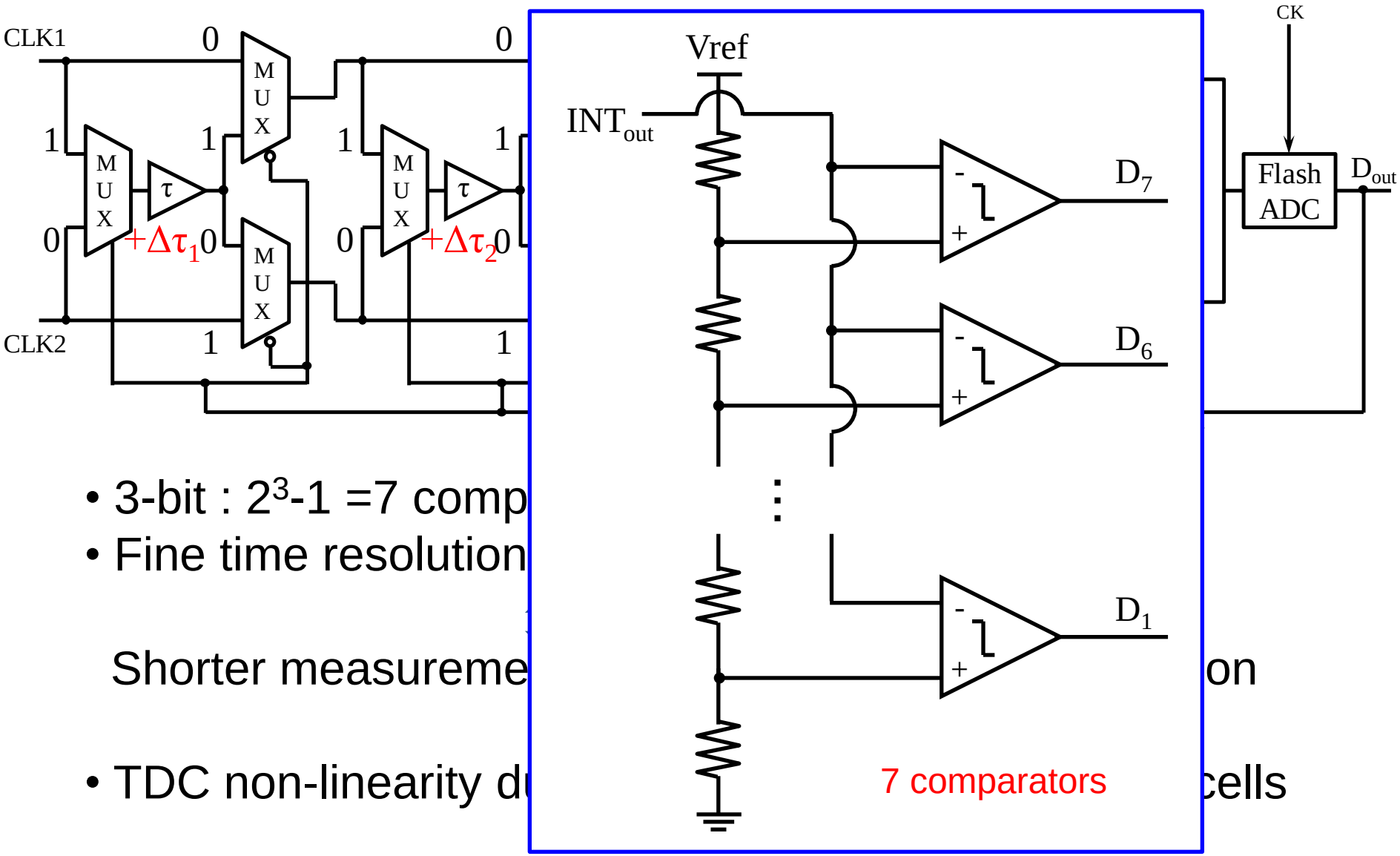


- 3-bit : 7 comparators and delays
- Fine time resolution with a given measurement time

Shorter measurement time with a given time resolution

- TDC non-linearity due to mismatches among delay cells.

Multi-Bit ΔΣ TDC

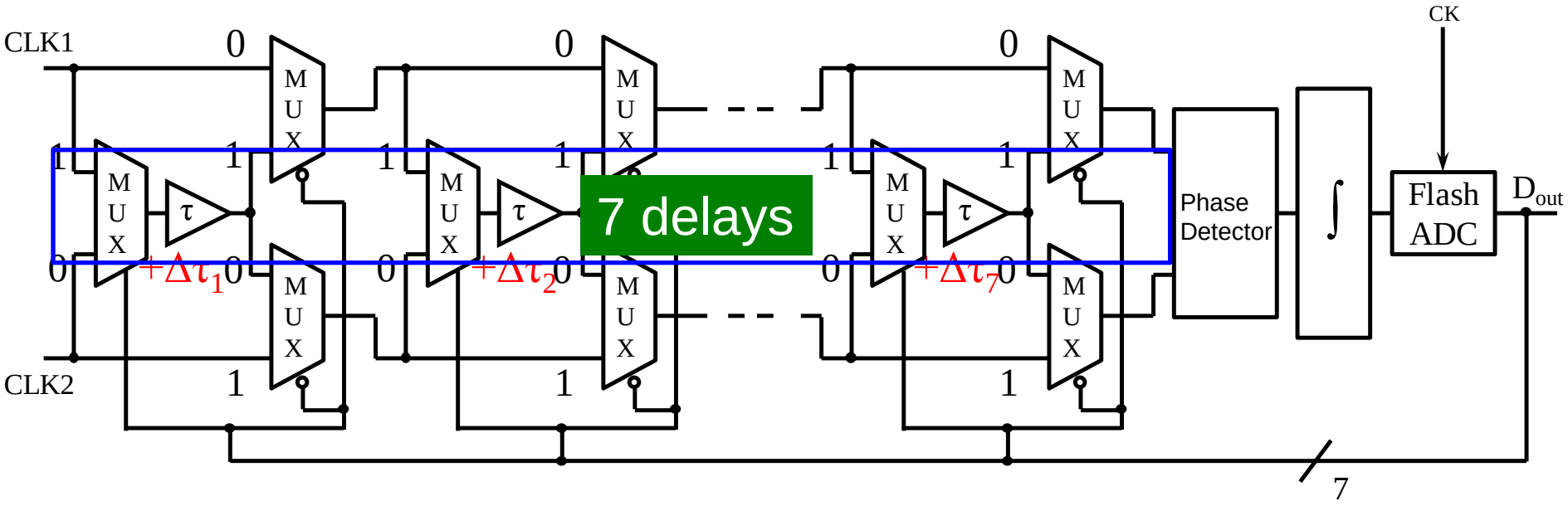


- 3-bit : 2^3-1 =7 comp
- Fine time resolution

  Shorter measureme on

- TDC non-linearity d cells

Multi-Bit ΔΣ TDC



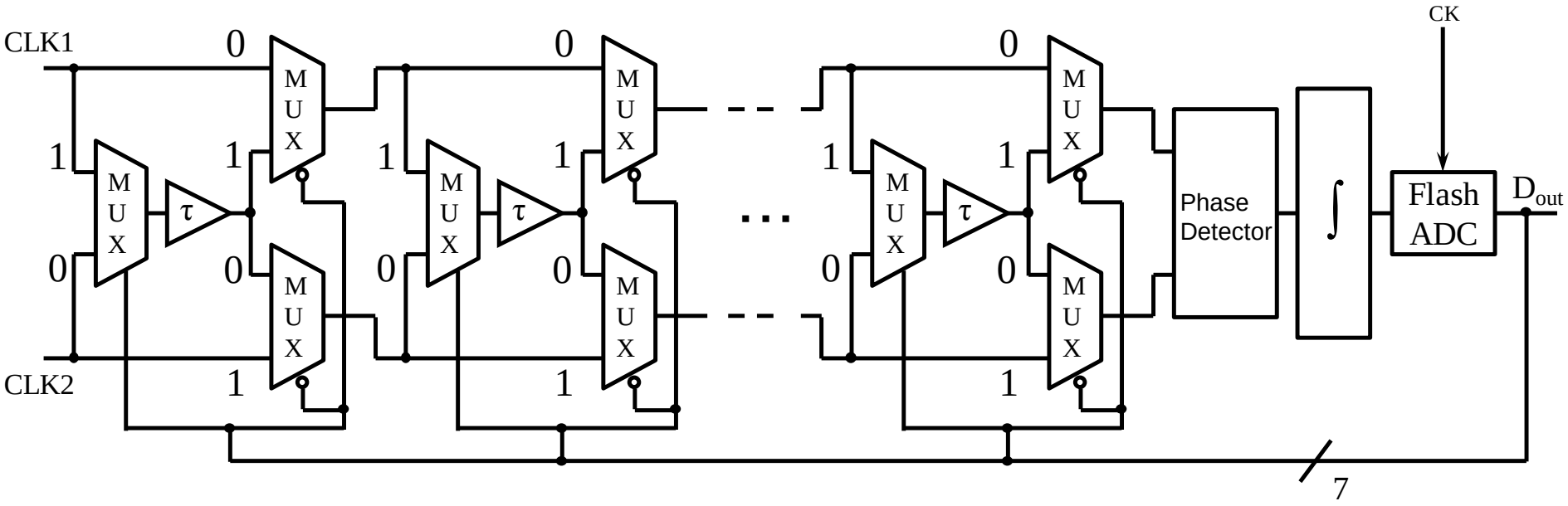
- 3-bit : 2^3-1 =7 comparators and delays
- Fine time resolution with a given measurement time

  ⇕

  Shorter measurement time with a given time resolution

- TDC non-linearity due to mismatches among delay cells

Multi-Bit ΔΣ TDC



- 3-bit : 2^3-1 =7 comparators and delays
- Fine time resolution with a given measurement time

  ⇕

  Shorter measurement time with a given time resolution

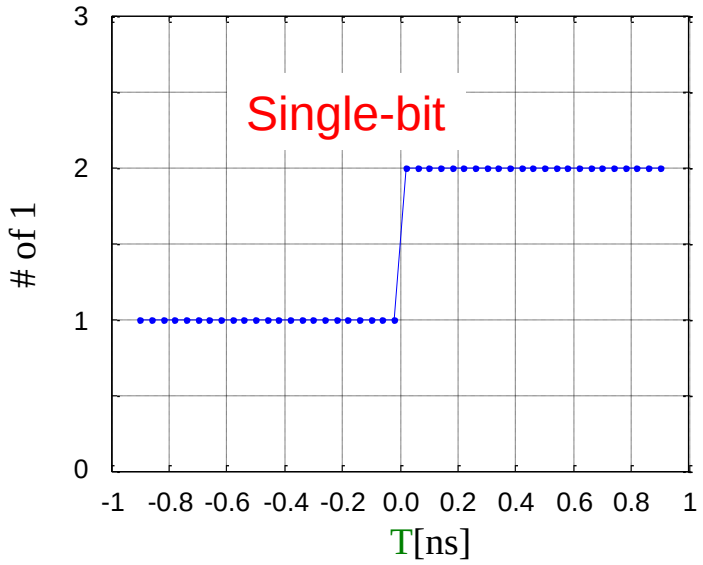
- TDC non-linearity due to mismatches among delay cells

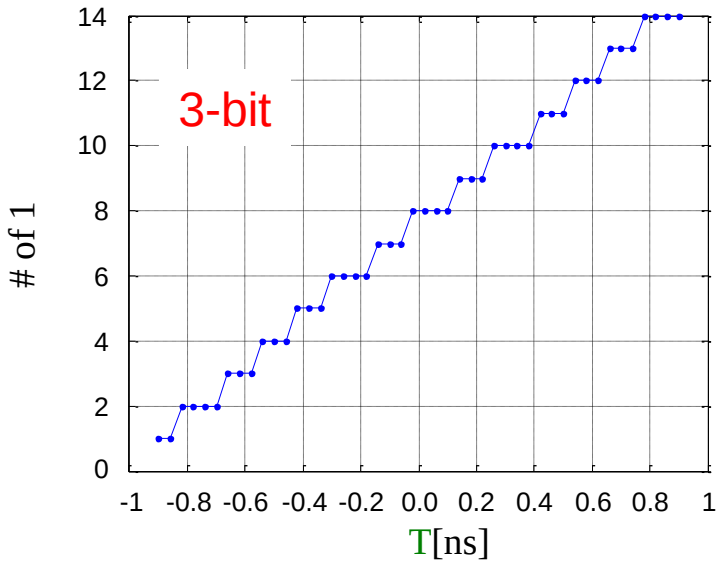
Time Resolution Comparison

- Simulation conditions

	1-bit ΔΣ TDC	3-bit ΔΣ TDC
Rising timing edge difference (T)	-0.9 ∼ 0.9 ns (Resolution : 0.04 ns)	-0.9 ∼ 0.9 ns (Resolution : 0.04 ns)
Delay time (τ)	1 ns	0.145 ns
The number of digital outputs	2	2

- A rising number of outputs for the interval T

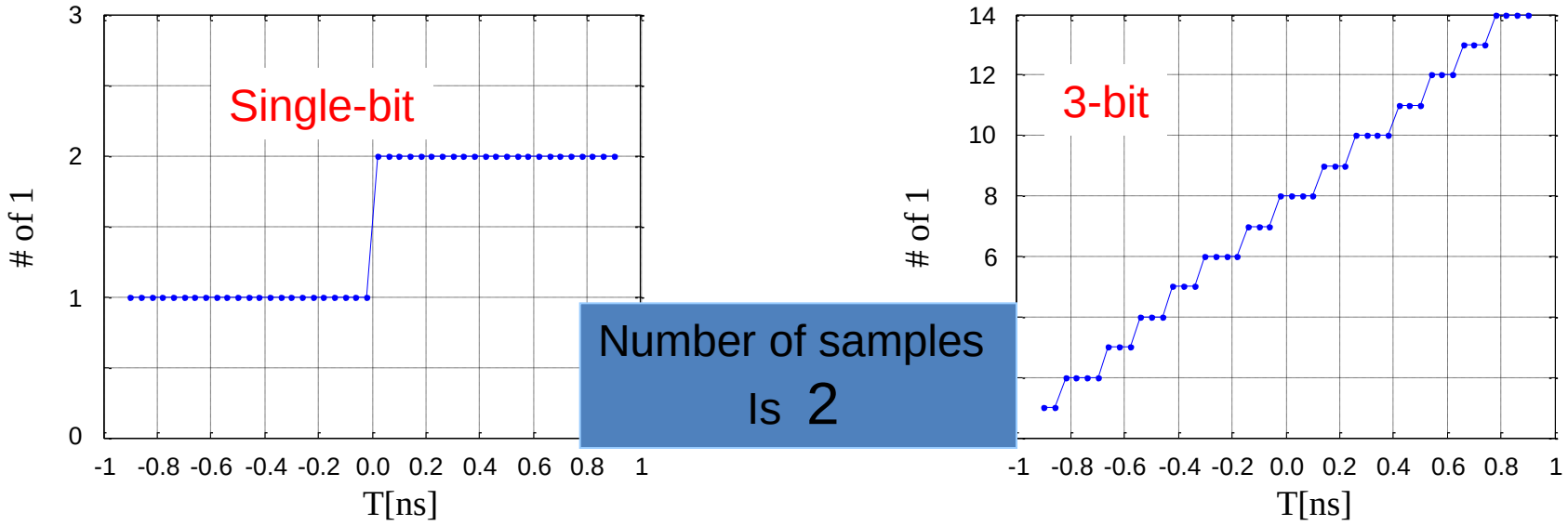




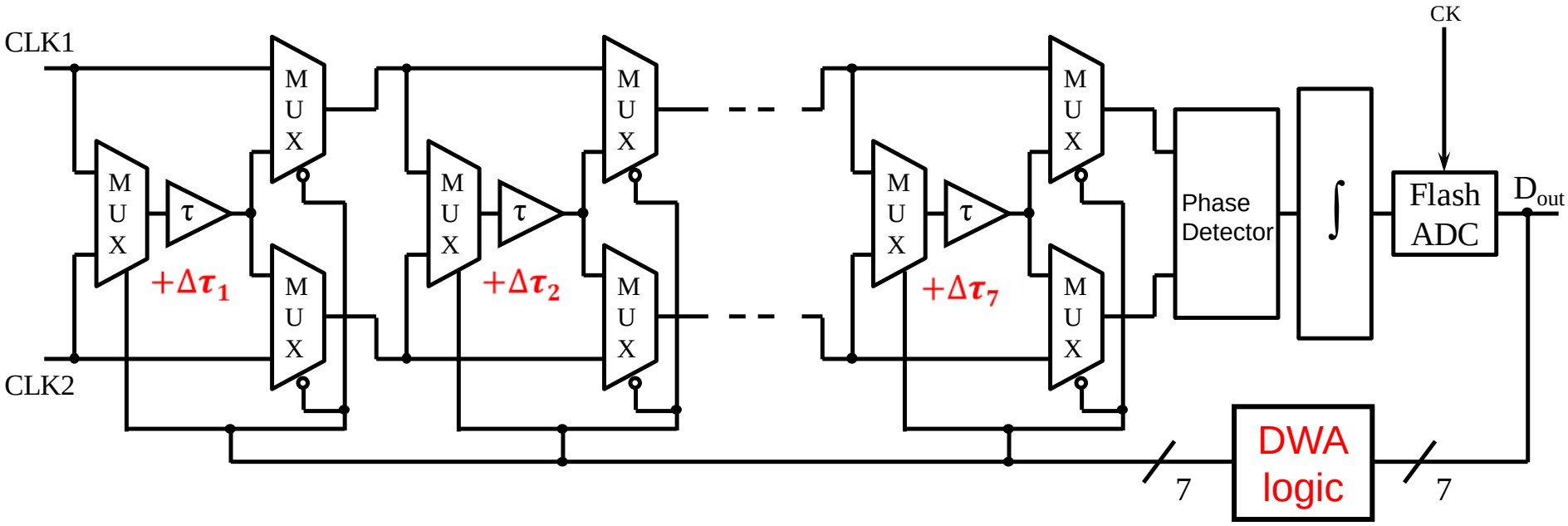
Measurement Time Comparison

✓Multi-bit takes short measurement time for a given time resolution

■ A rising number of outputs for the interval T



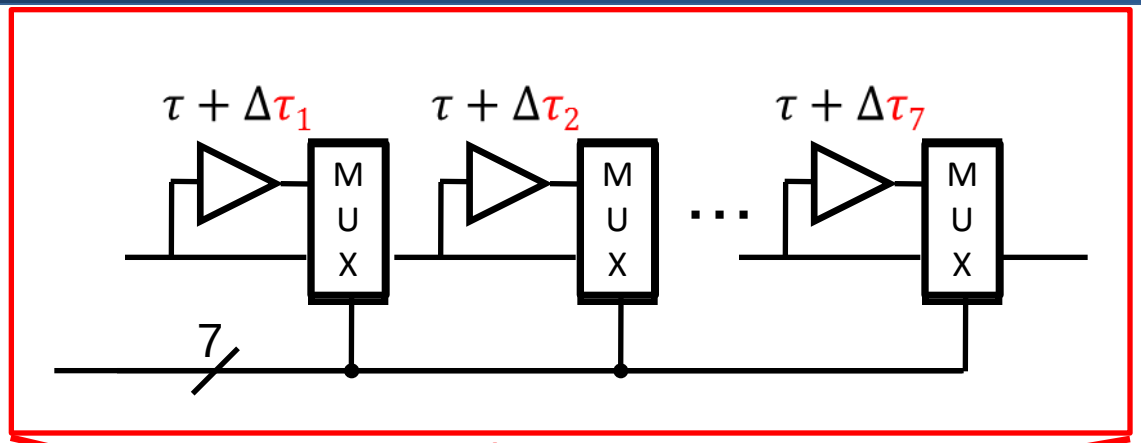
DWA (Data Weighted Averaging)

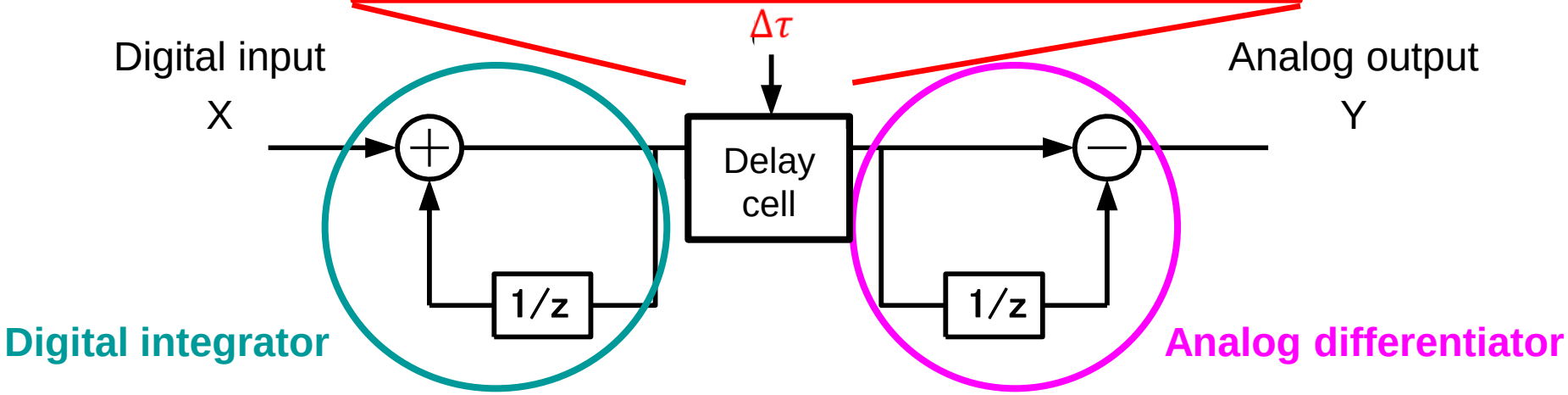


- Flash ADC outputs
  - ➡ shuffled by DWA logic,
    fed into MUXs as select signals

- Delay mismatch effects
  - ➡ moved to high-frequency (noise-shaping)

Noise-Shaping

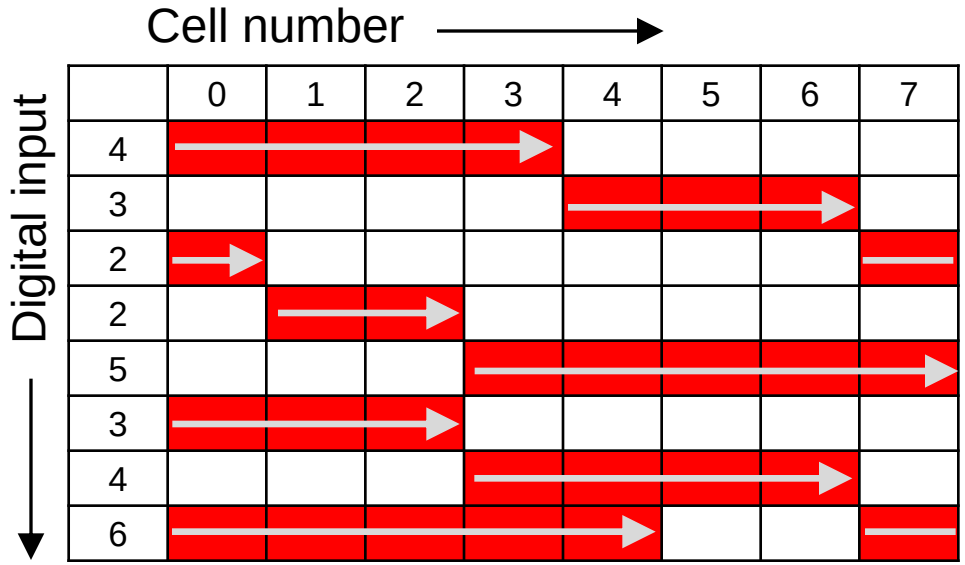




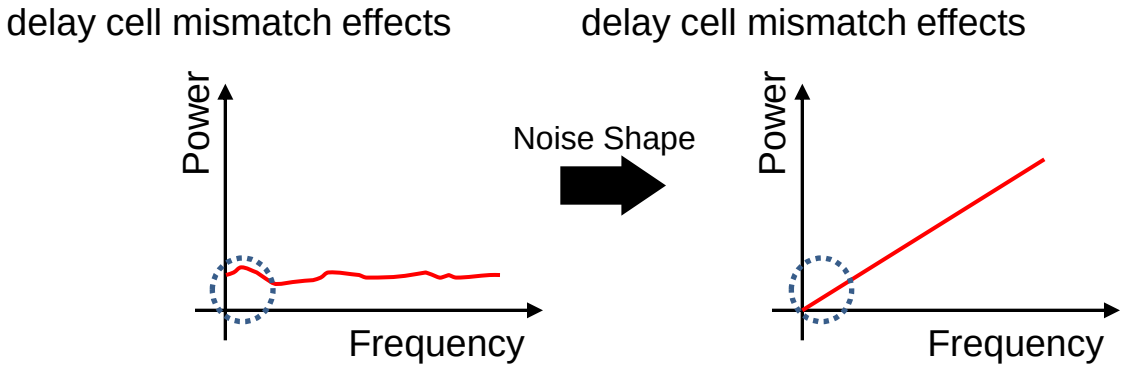
$$Y(z) = X(z) + (1 - 1/Z)\Delta\tau(z)$$

Delay mismatch $\Delta\tau$ is first-order noise-shaped.

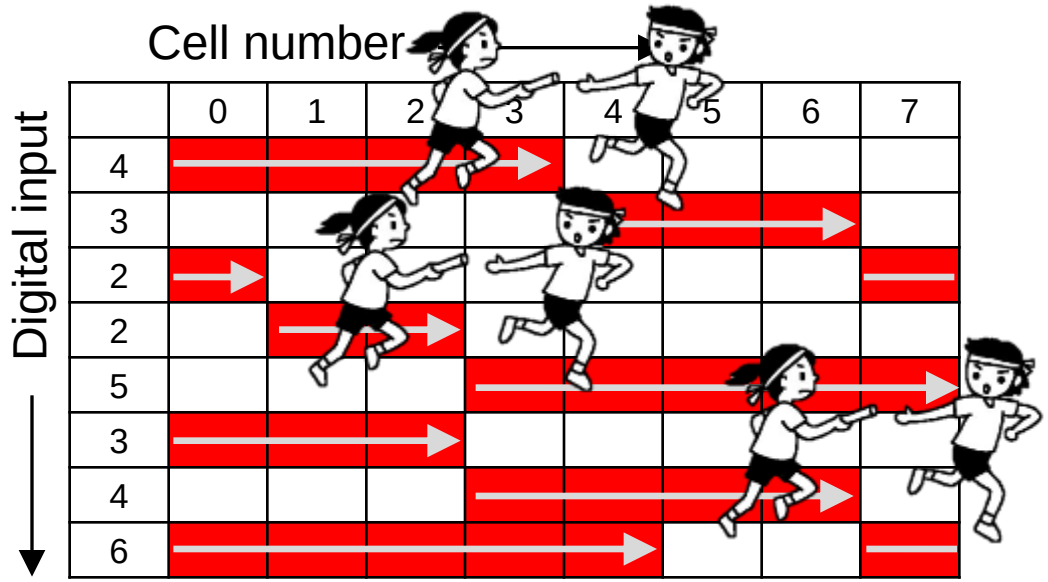
DWA & Noise Shaping



- Delay τ : integration & differentiation
- Delay mismatch $\Delta\tau$: differentiation

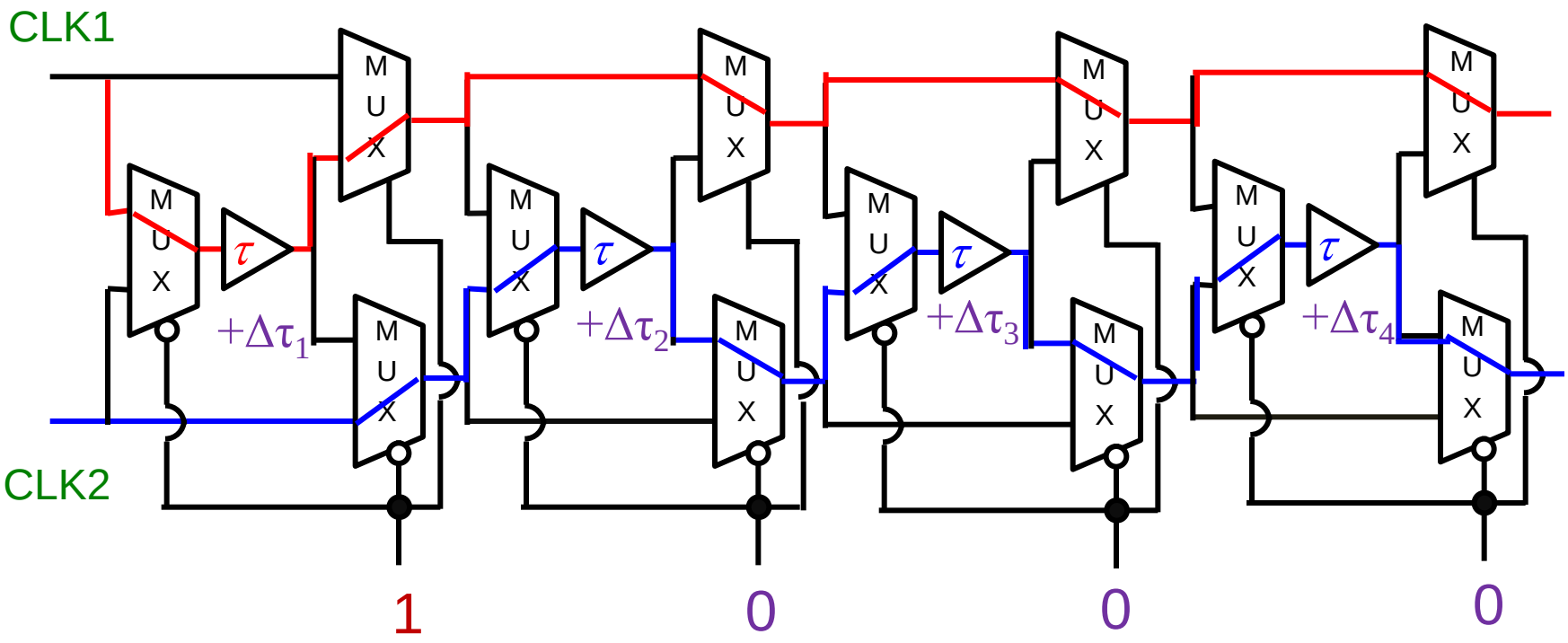


DWA Operation



Pass a baton in relay race !

No DWA Digital input 1 at time 1

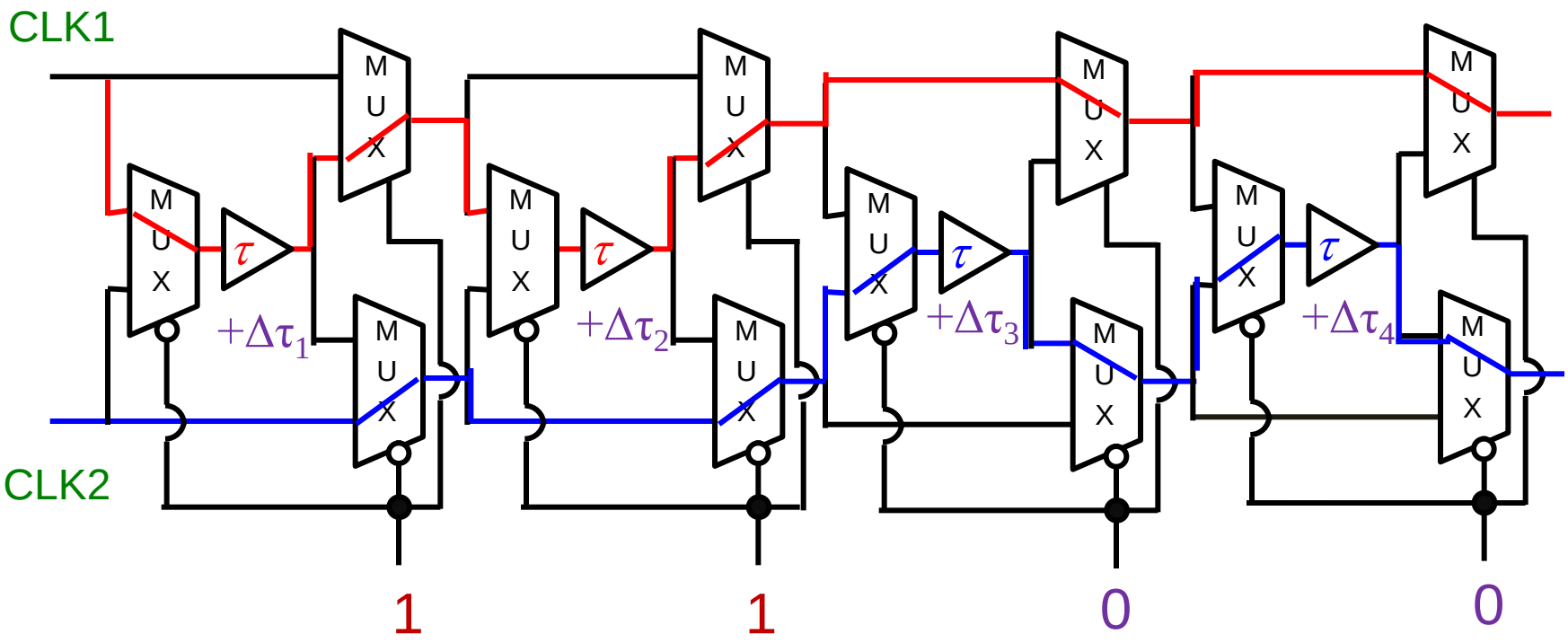


Delay cell selection

CLK1 $\tau+\Delta\tau_1$

7 comparators' outputs

No DWA Digital input 2 at time 2

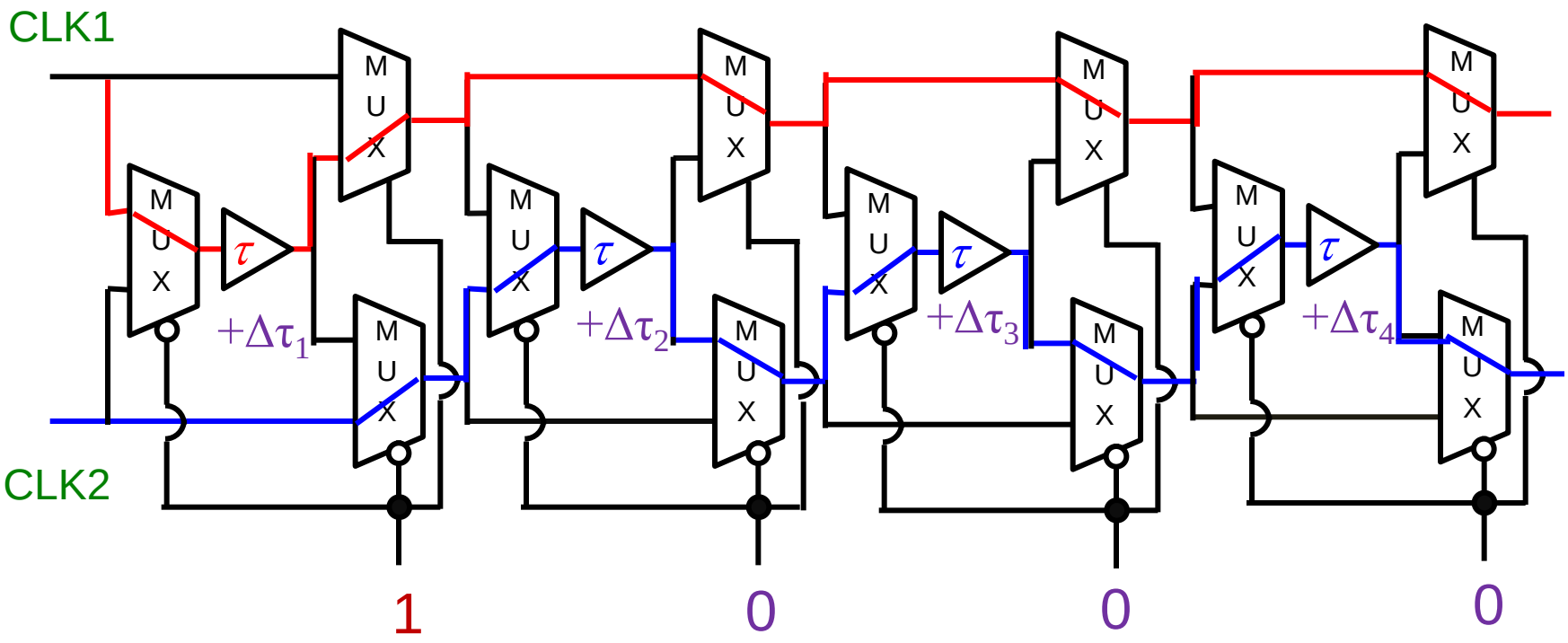


Delay cell selection

CLK1 $\tau+\Delta\tau_1$ $\tau+\Delta\tau_2$

7 comparators' outputs

No DWA Digital input 1 at time 3

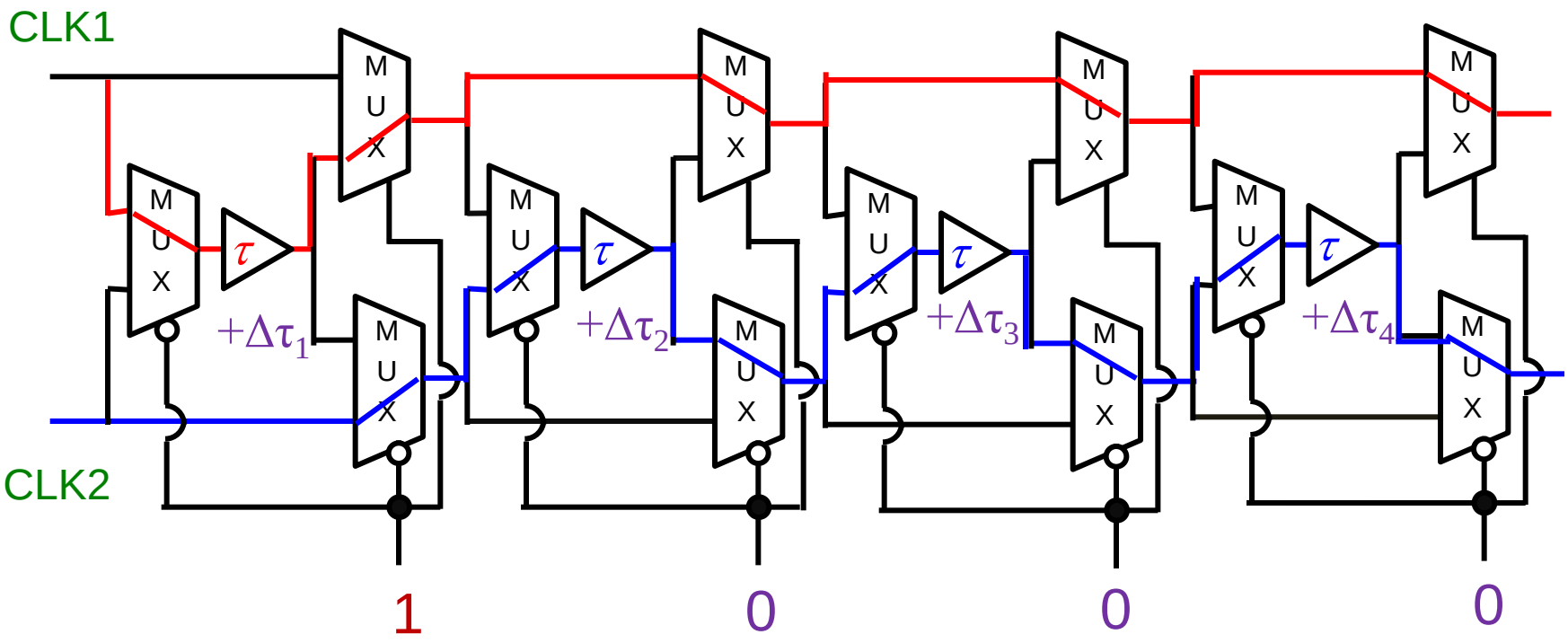


Delay cell selection

CLK1 $\tau+\Delta\tau_1$

7 comparators' outputs

DWA Digital input 1 at time 1



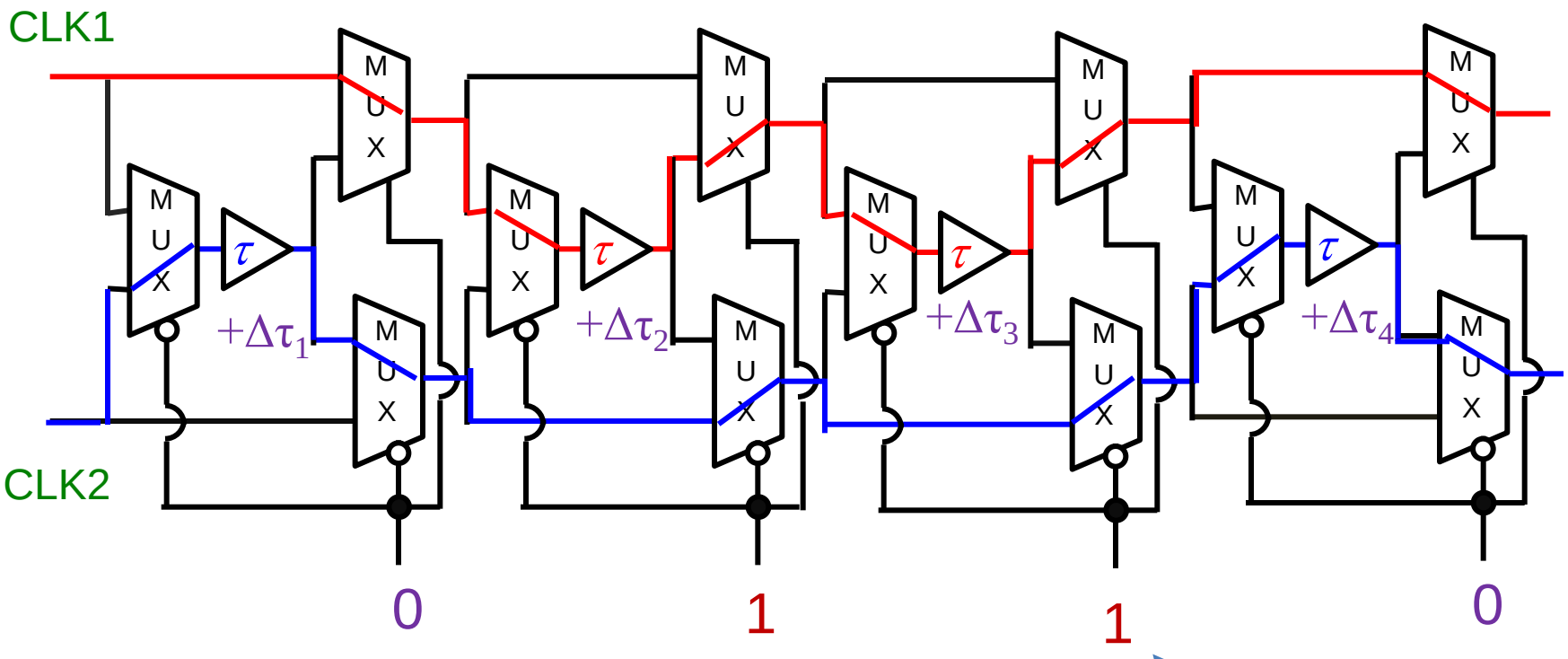
Delay cell selection

CLK1 $\tau+\Delta\tau_1$

DWA logic outputs

7 comparators' outputs

DWA Digital input 2 at time 2



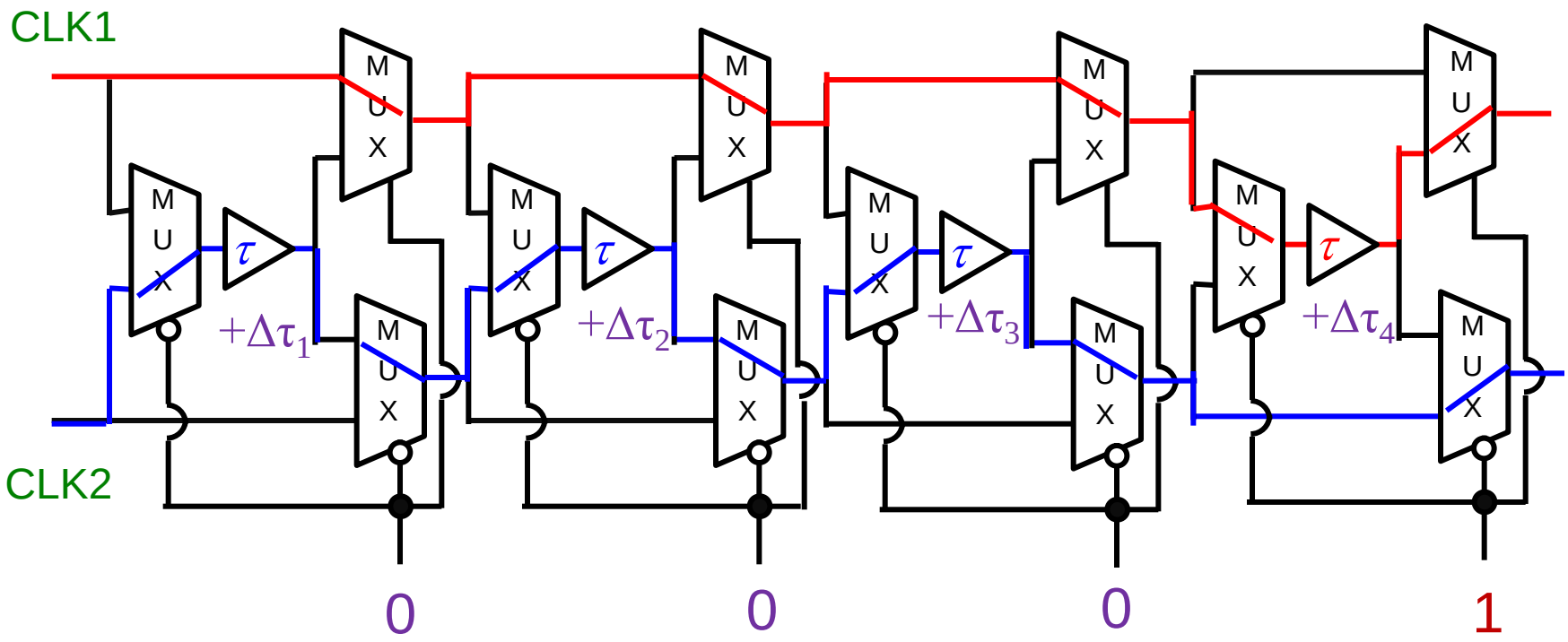
Delay cell selection

DWA logic outputs

CLK1 $\tau+\Delta\tau_2$ $\tau+\Delta\tau_3$

7 comparators' outputs

DWA Digital input 1 at time 3



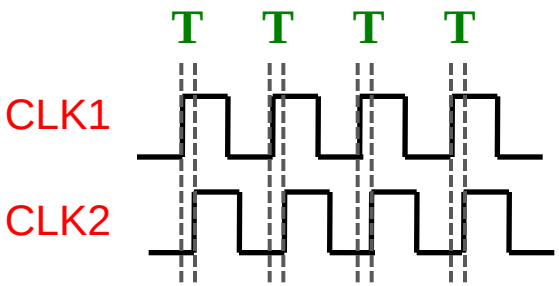
Delay cell selection

CLK1 $\tau+\Delta\tau_4$

DWA logic outputs

7 comparators' outputs

DWA Effectiveness

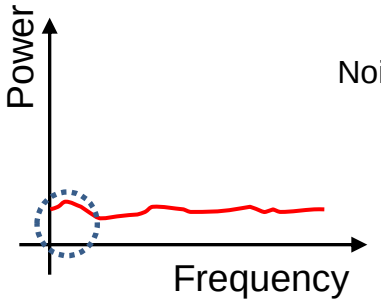


- Delay τ : integration & differentiation
- Delay mismatch $\Delta\tau$: differentiation

Measure **T**

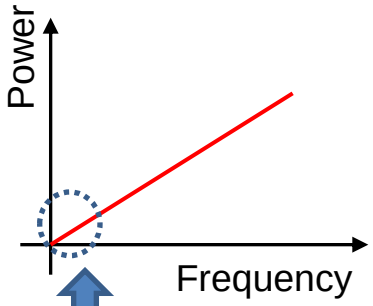
T is DC signal.

delay cell mismatch effects



Noise Shape

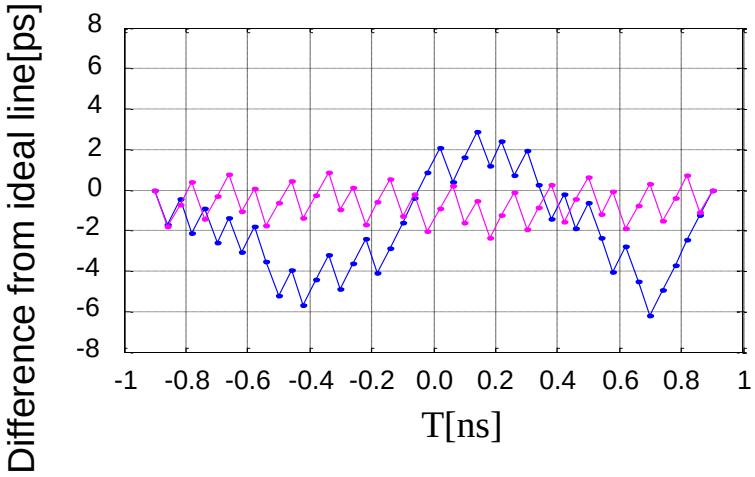
delay cell mismatch effects



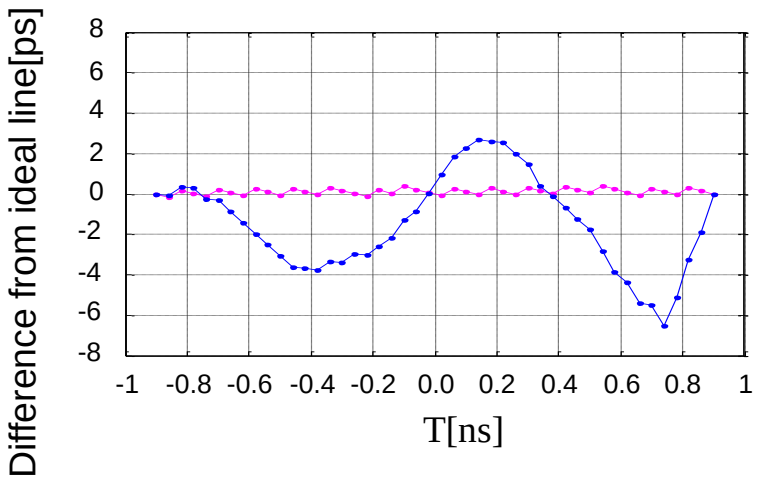
Mismatch effects reduction at DC

Simulation of ΔΣ TDC with DWA

- Output：99 points



- Output：599 points



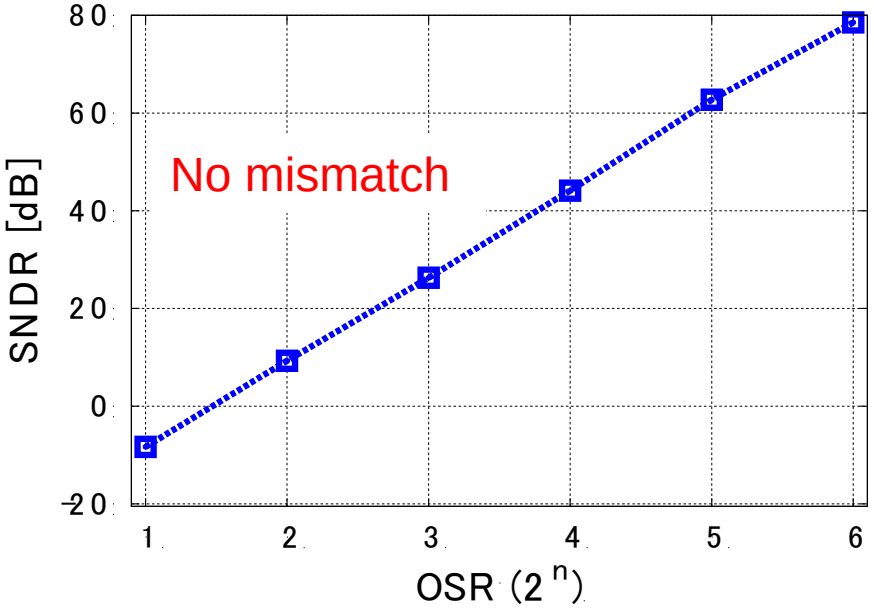
ΔΣ TDC(with DWA)

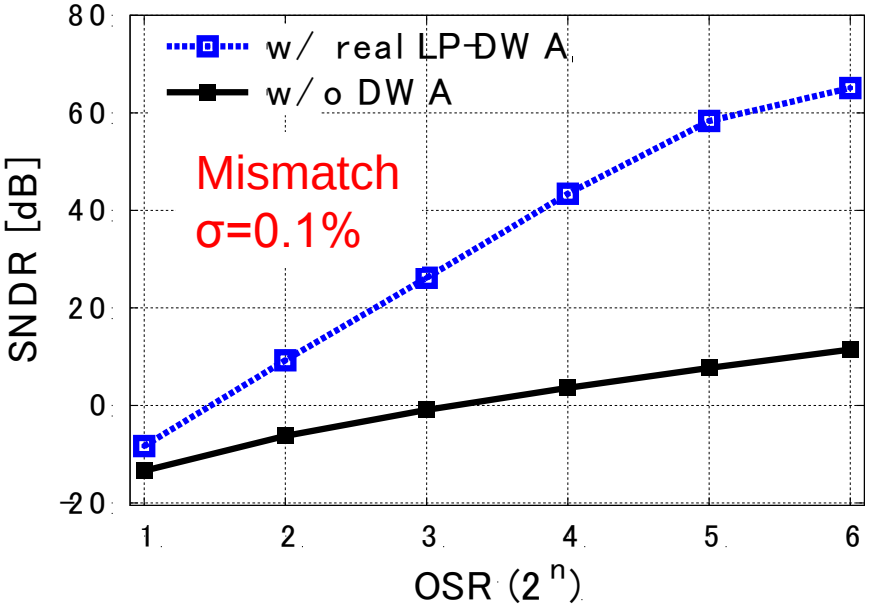
ΔΣ TDC(without DWA)

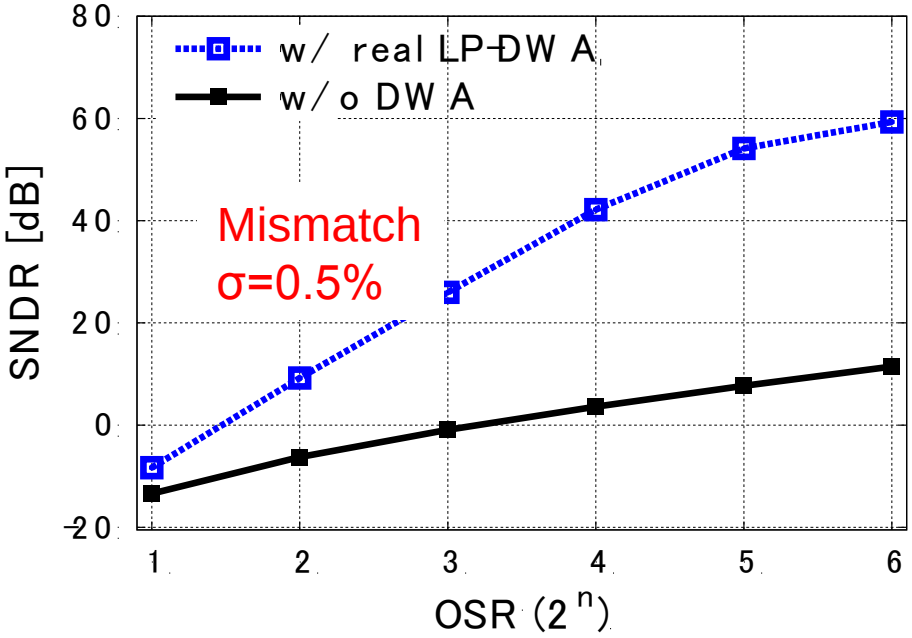
✓Reduce the effect of delay mismatches

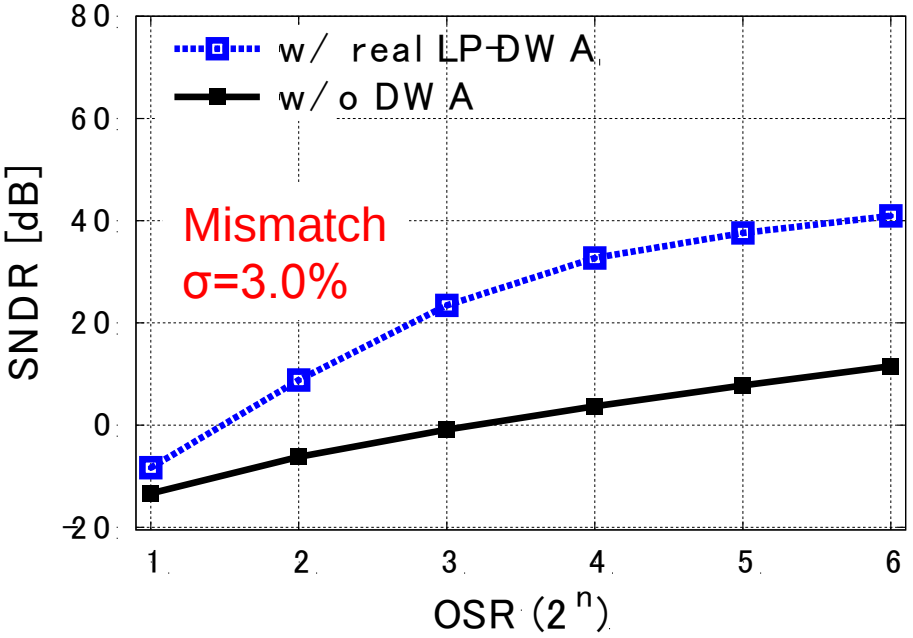
ΣΔ TDC linearity is improved

DWA & Mismatches





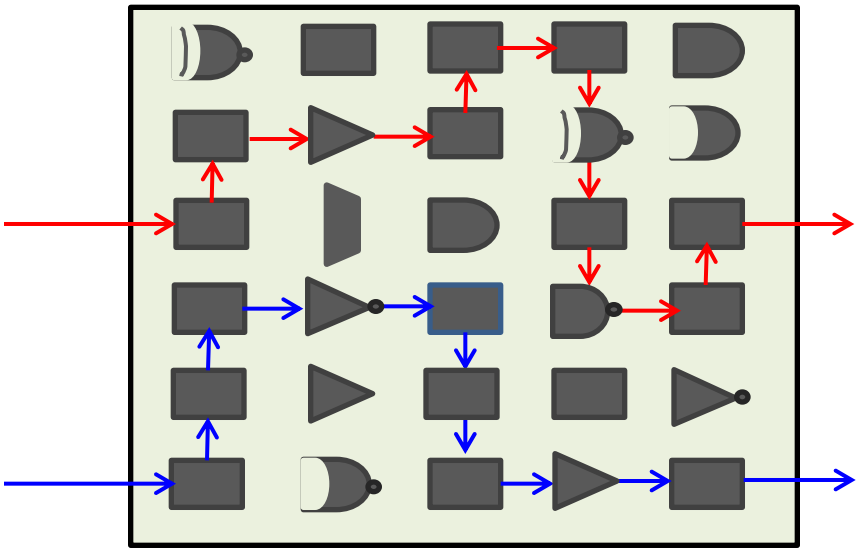




Contents

Analog FPGA Implementation

Programmable System-on-Chip（PSoC） Cypress Semiconductor

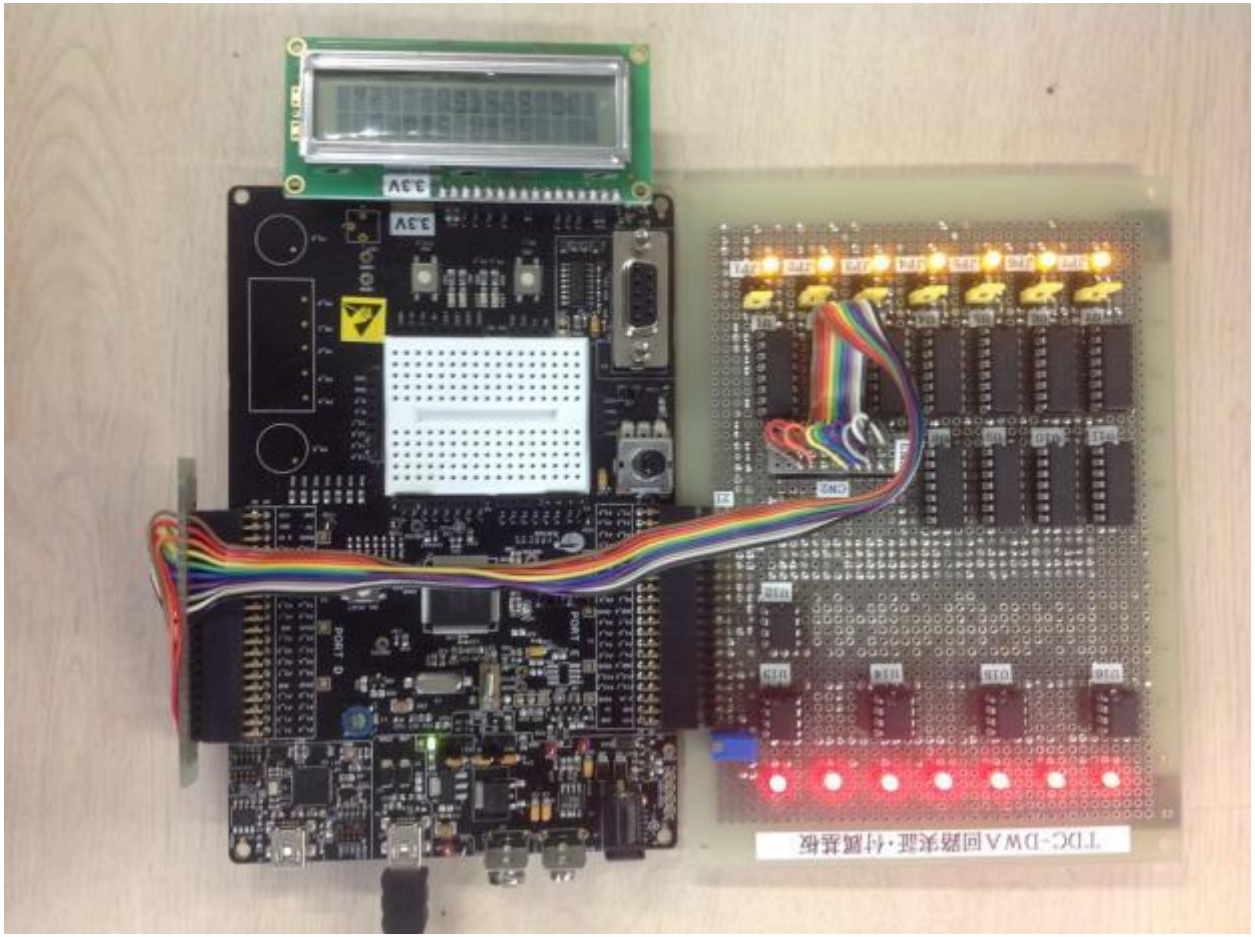


Analog-Digital Mixed-Signal FPGA

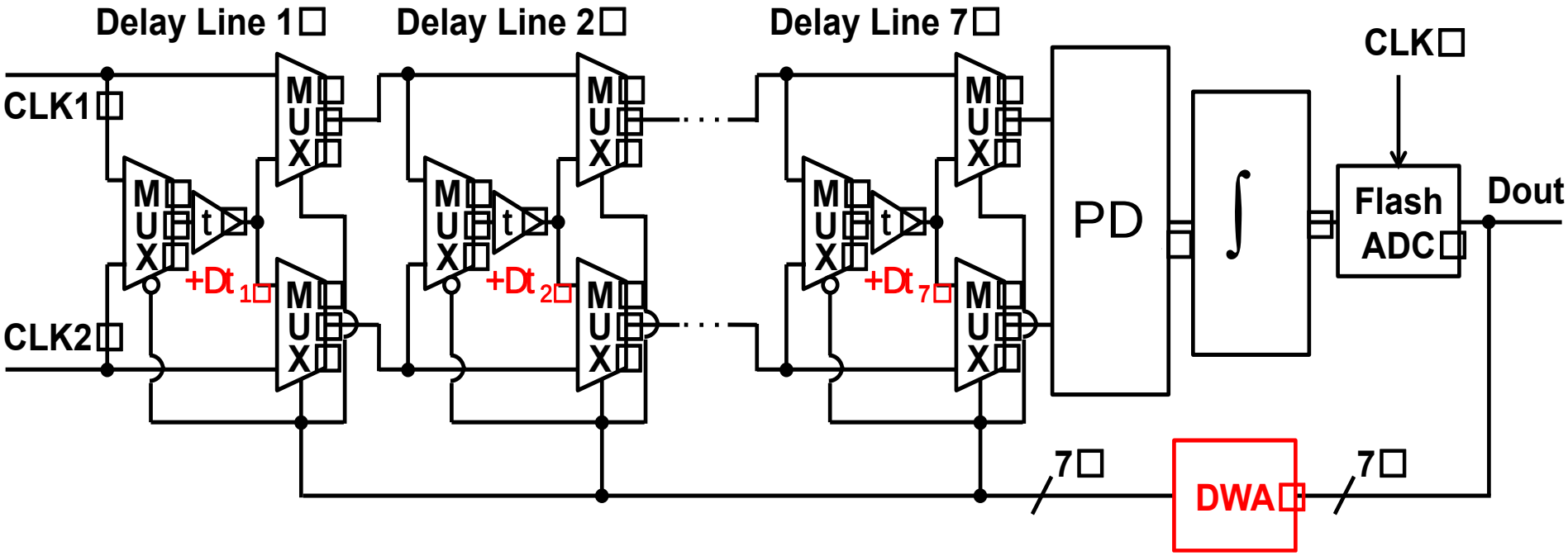
Advantages of PSoC Implementation

- Low cost
- Short design time
- On-chip debug/design correction
- Easy for chip testing

Photo of ΔΣTDC PSoC Implementation

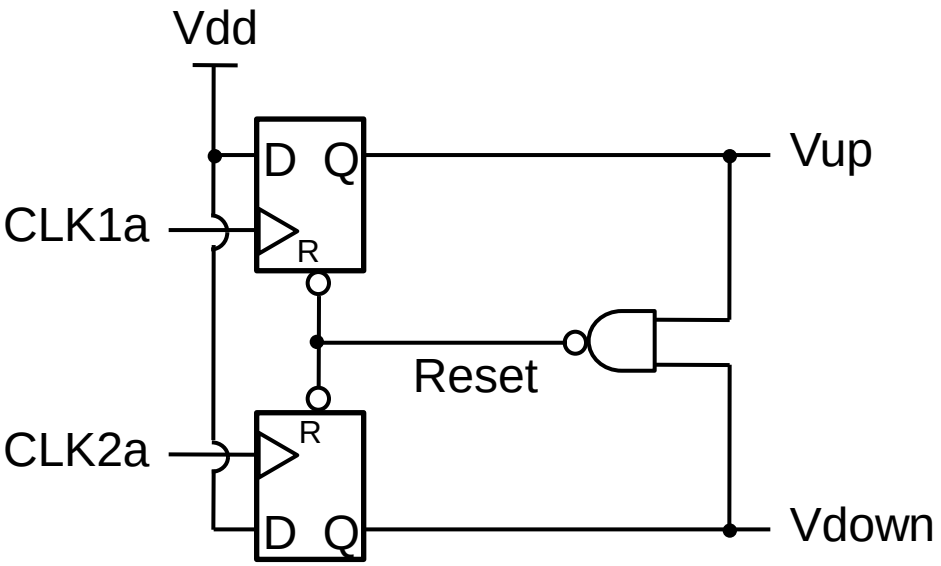


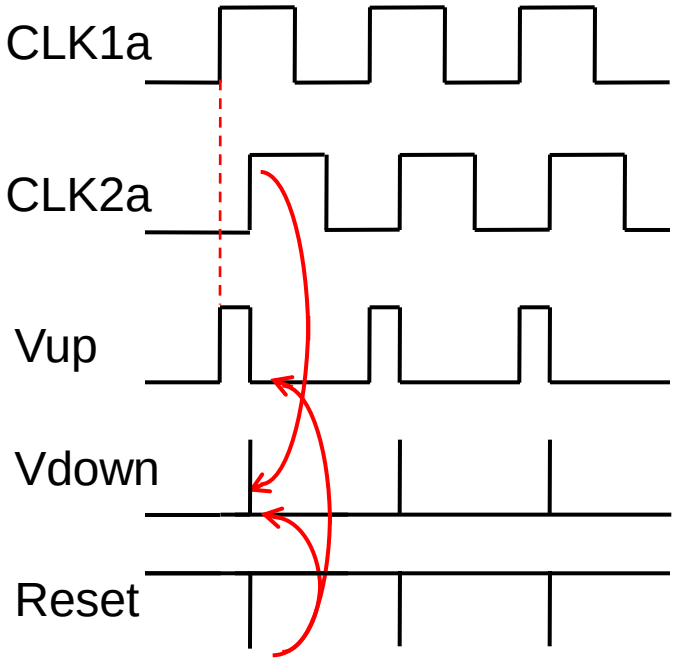
Designed 3-bit ΔΣTDC

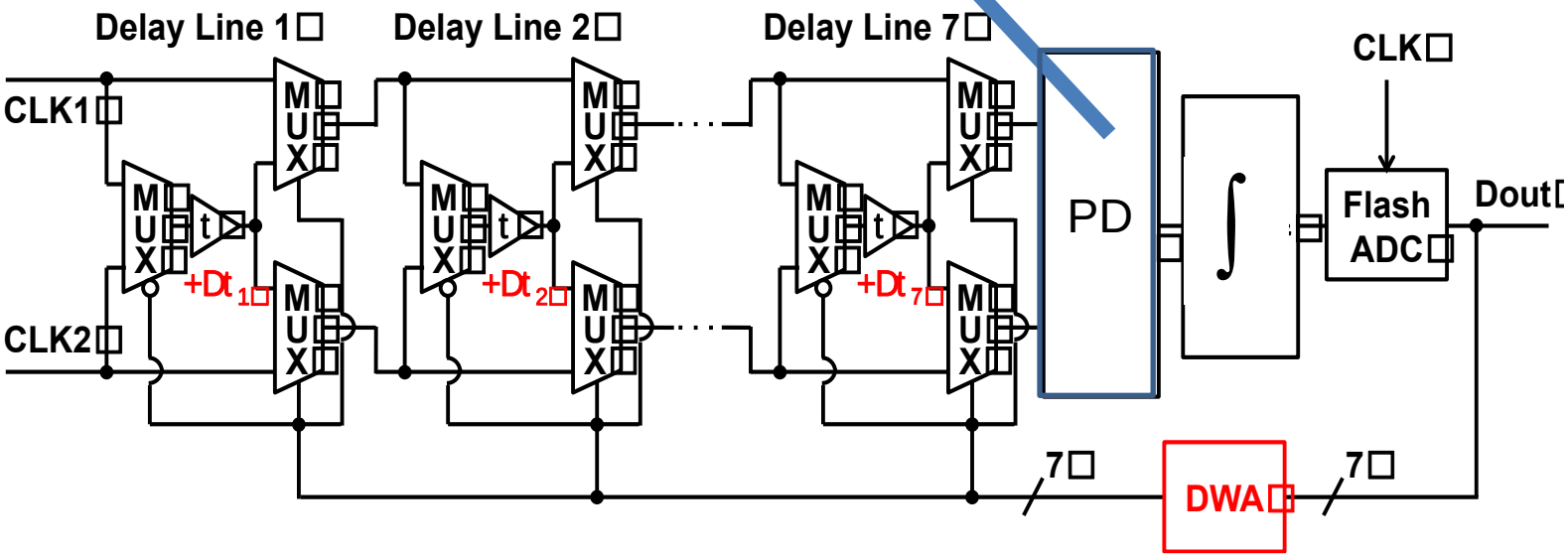


- Delay τ 's are implemented with external R, C.
- R value can be chosen with external switch.

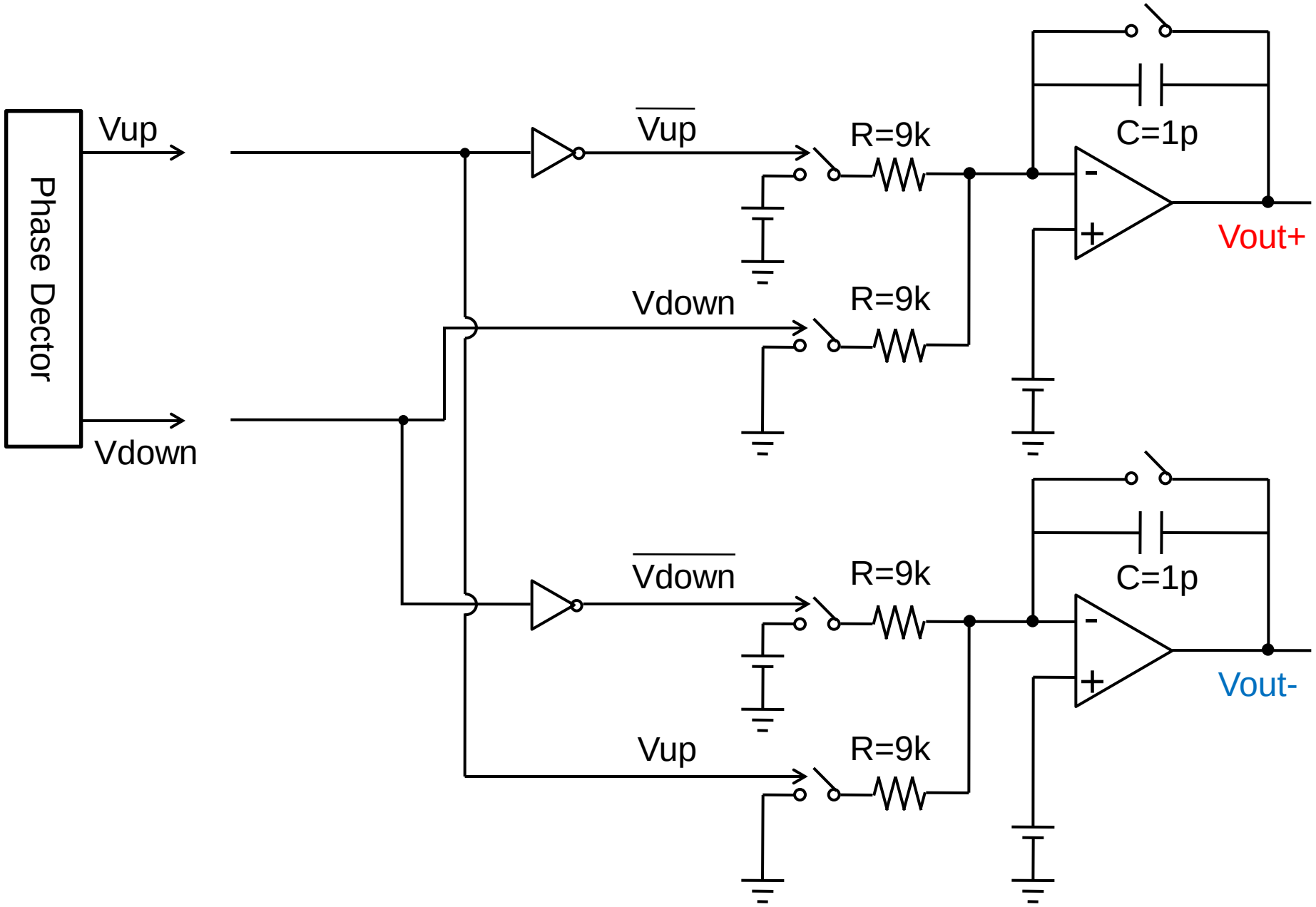
Phase Detector



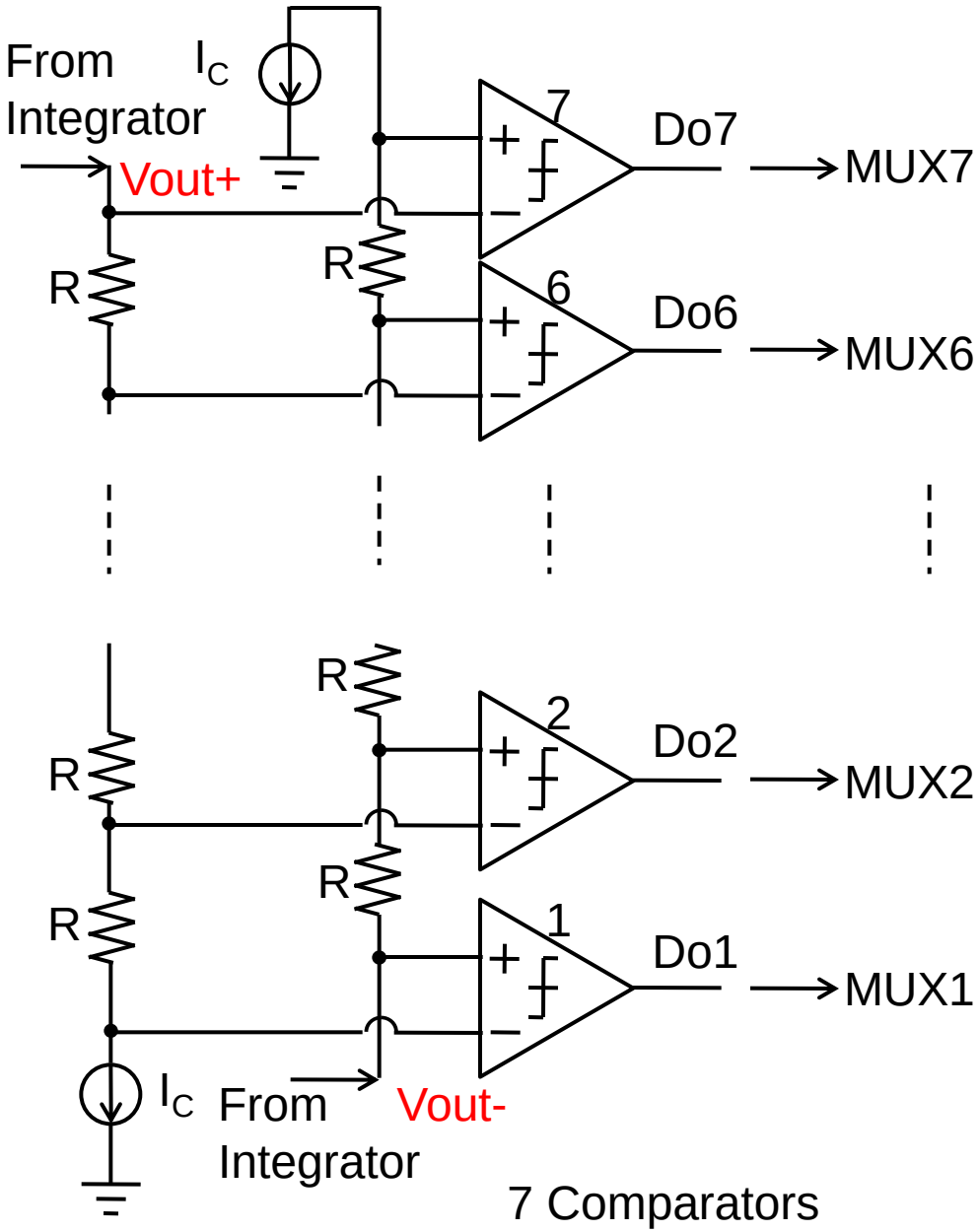




Phase Detector and Integrator



3bit Flash ADC Without Encoder



Differential Input

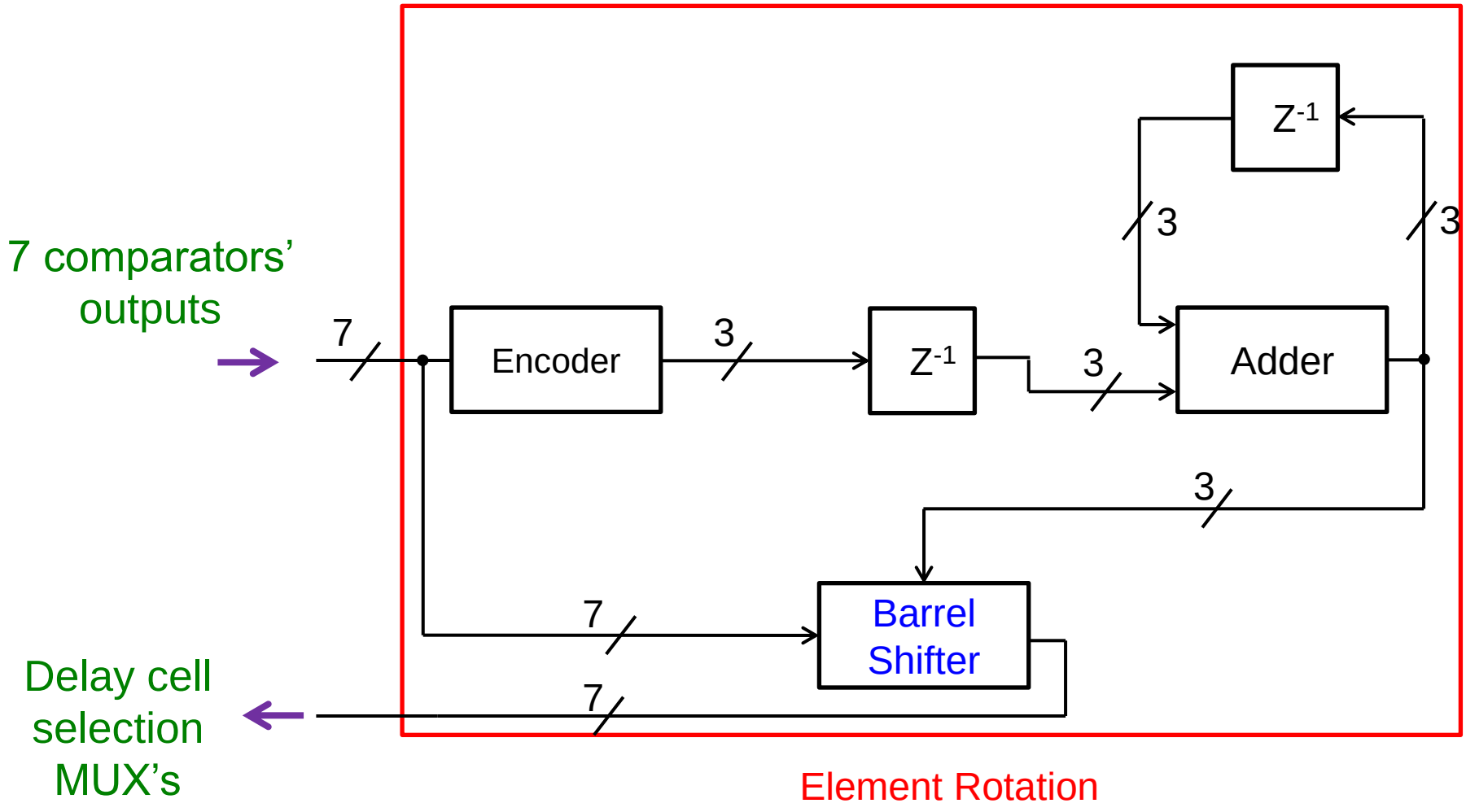
+

Dynamic Resistor Ladder

Input to DWA logic

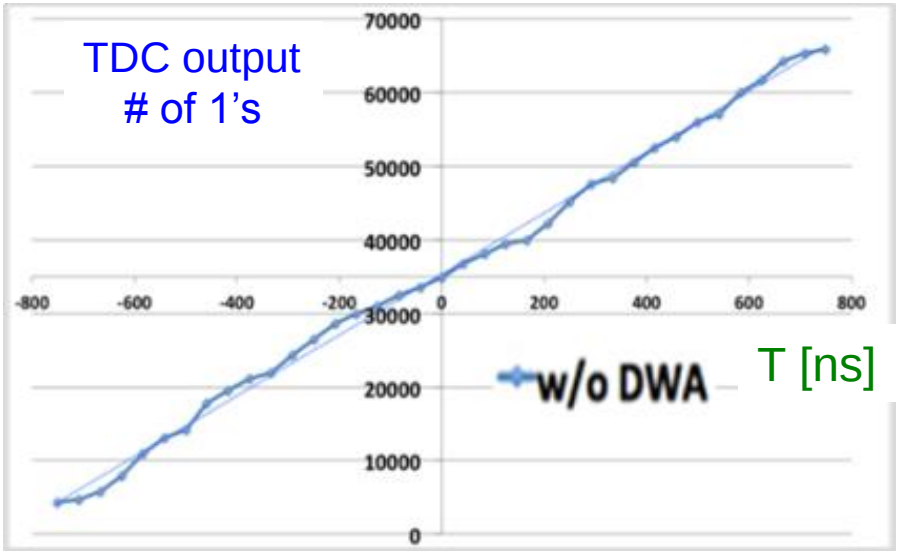
MUX selection signal for delay selection

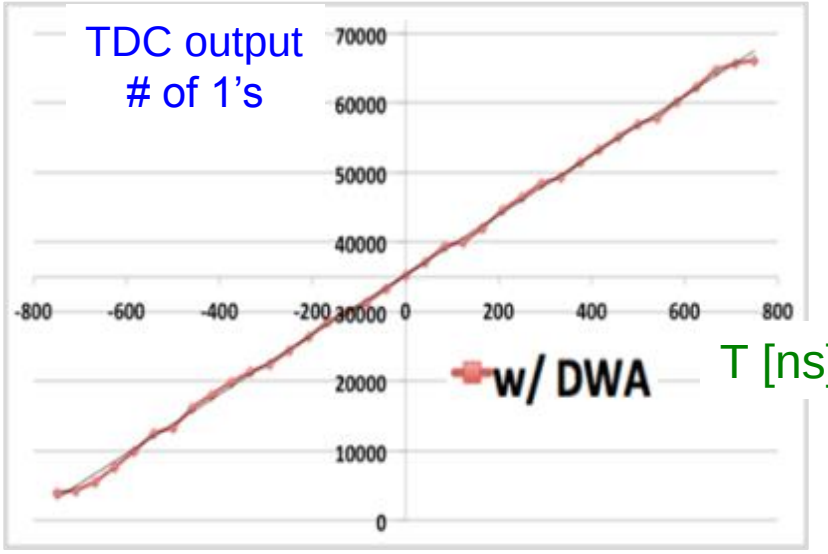
DWA Logic Circuit



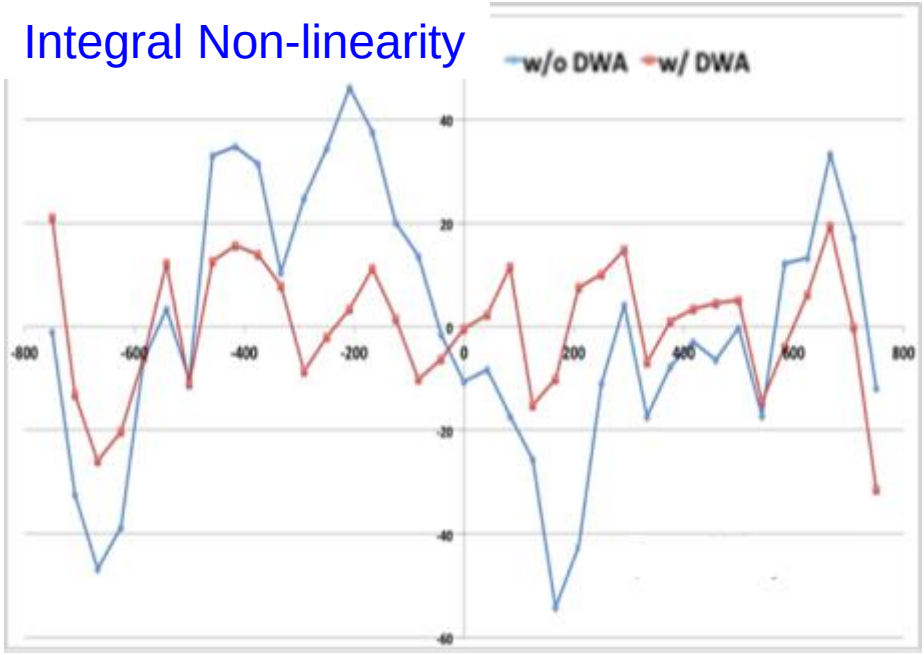
Implemented with small digital circuitry

Measured Result (Case 1)



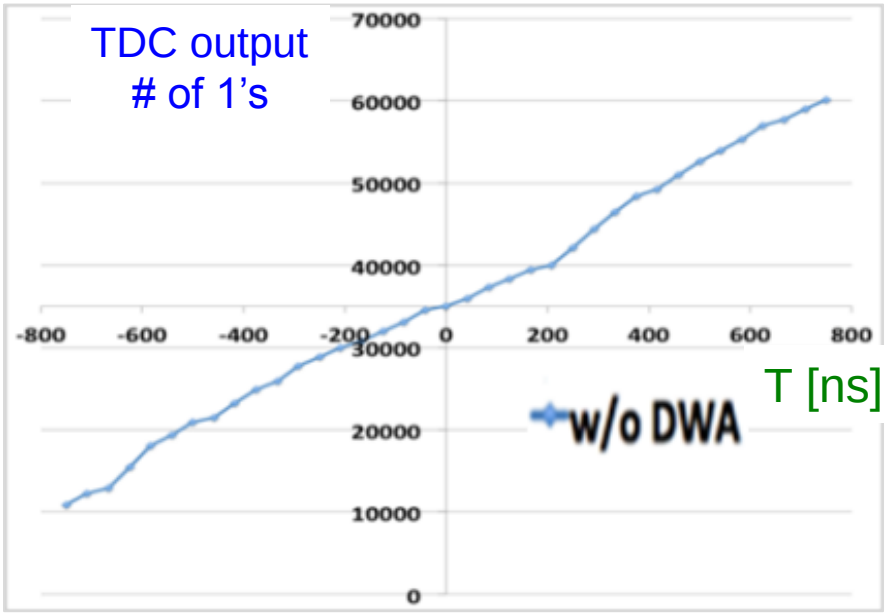


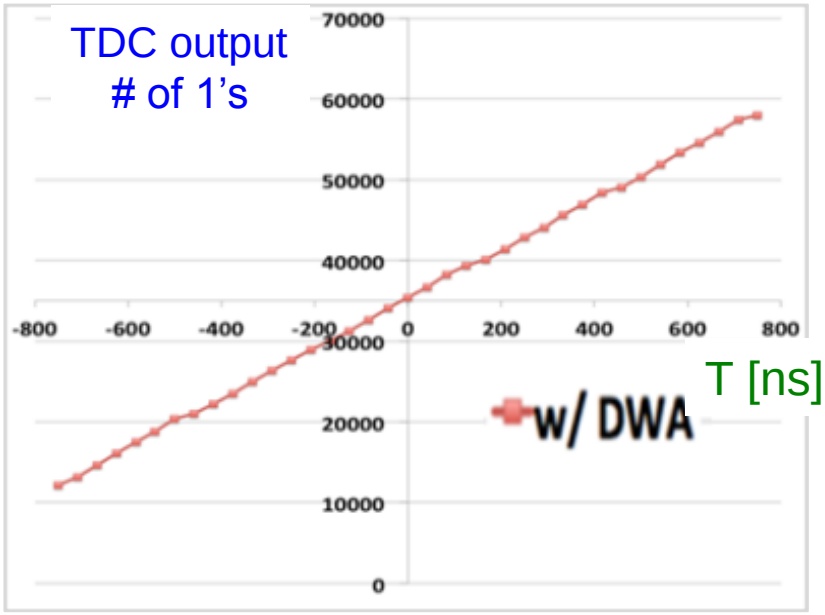
Integral Non-linearity



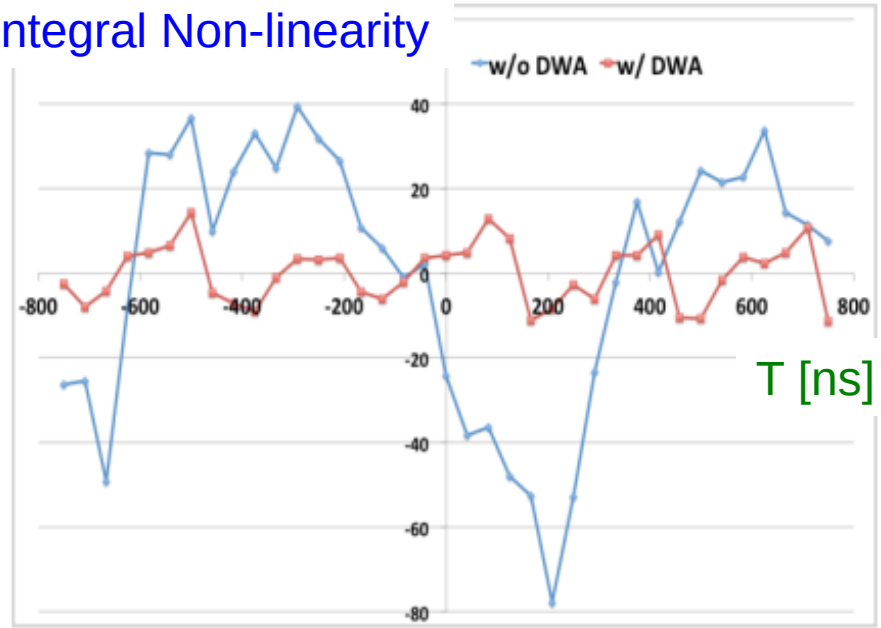
10,000 TDC output data are measured.

Measured Result (Case 2)





Integral Non-linearity



10,000 TDC output data are measured.

Contents

Circuit Performance Comparison

	Flash TDC	1-bit ΔΣ TDC	Multi-Bit ΔΣ TDC (without correction)	Multi-Bit ΔΣ TDC (with correction)
Circuit size	×	◎	○	○
Resolution	×	◎	◎	◎
Linearity	△	◎	×	◎
Testing time	◎	×	○	○

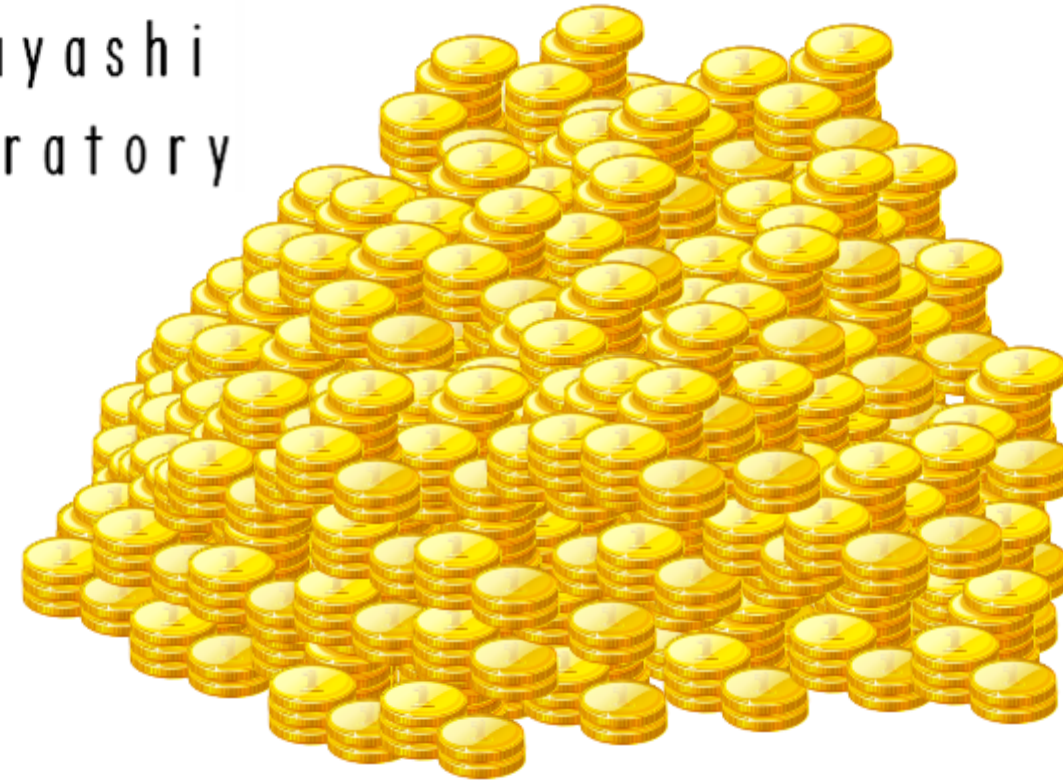
Conclusion

- We propose to use ΔΣ TDC
  for digital signal timing measurement

- Multi-bit ΔΣ TDC
  - ➢ Short measurement time
  - ➢ Fine time resolution
  - ➢ Non-linearity due to mismatches among delay cells
    - ⇨ DWA algorithm for linearity improvement
  - – Analog FPGA verification

Low cost, high quality digital timing test can be realized using BOST.

Kobayashi Laboratory



Time is GOLD !!

ΔΣTDC is a key.

References

Flash-type TDC (first paper)

[1] Y. Arai, T. Baba, “A CMOS Time to Digital Converter VLSI for High-Energy Physics”, IEEE Symposium on VLSI Circuits (1988).

ΔΣTD (first paper)

[2] B. Young, K. Sunwoo A. Elshazly, P. K. Hanumolu, “A 2.4ps Resolution 2.1mW Second-order Noise-shaped Time-to-Digital Converter with 3.2ns Range in 1MHz Bandwidth,” IEEE Custom Integrated Circuits, San Jose (Sept. 2010)

Multi-bit ΔΣTDC Linearity Improvement

[3] S. Uemori, M. Ishii, H. Kobayashi, et. al., “Multi-bit Sigma-Delta TDC Architecture with Improved Linearity,” Journal of Electronic Testing : Theory and Applications, Springer, vol. 29, no. 6, pp.879-892 (Dec. 2013).

Application of ΔΣTDC to Phase Measurement

[4] D. Hirabayashi, Y. Osawa, N. Harigai, H. Kobayashi et. al., ”Phase Noise Measurement with Sigma-Delta TDC”, IEEE International Test Conference, Poster Session, Anaheim, CA (Sept. 2013).