# Timing Measurement BOST With Multi-Bit Delta-Sigma TDC

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*Abstract*— **This paper describes design and implementation of a multi-bit delta-sigma ($\Delta\Sigma$) Time-to-Digital Converter (TDC) with Data-Weighted-Averaging (DWA) algorithm on analog FPGA. I/O interfacing circuits such as double-data-rate (DDR) memory interfaces are very important, and their low-cost, high-quality test is challenging. We propose here simple test circuitry for measuring digital signal timing of I/O interfacing circuits with high resolution and good accuracy. We focus on TDC applications of $\Delta\Sigma$ modulators (for fine-timing-resolution, digital output, and simple circuitry) and with multi-bit architecture (for short testing time). However, the multi-bit $\Delta\Sigma$ TDC suffers from delay mismatches among delay cells. Then we propose to apply the DWA algorithm for the delay cells in order to solve this problem. Our experimental results showed that the DWA algorithm improved the overall multi-bit$\Delta\Sigma$ TDC linearity.**

*Keywords— Time-to-Digital Converter; Time Measurement; Analog FPGA; Delta-Sigma*

## I.    INTRODUCTION

I/O interfacing circuits such as double-data-rate (DDR) memory interfaces are very important, and their low-cost, high-quality test is challenging. [1] This paper describes simple test circuitry for measuring digital signal timing with high resolution and good accuracy. We focus on Time-to-Digital Converter (TDC) applications of delta-sigma ($\Delta\Sigma$) modulators (for fine-timing-resolution, digital output, and simple circuitry) and with multi-bit architecture (for short testing time). [2]-[10]

A multi-bit $\Delta\Sigma$ TDC suffers from delay mismatches among delay cells, but here we propose to apply the data-weighted-averaging (DWA) algorithm [8] for the delay cells in order to solve this problem. In this paper we show implementation of a multi-bit $\Delta\Sigma$ TDC with DWA as a Built-Out Self-Test (BOST) and we present experimental results that the DWA algorithm improves the overall multi-bit $\Delta\Sigma$ TDC linearity.

## II.    FLASH TDC

A TDC can be used to measure digital signal timing. The architecture of a basic flash-type TDC is shown in Fig.1 [11]. It consists of a delay-line using delay cells in the signal path and an array of flip-flops. The input Start signal passes along the delay cells, which are connected in series. And then each signal is connected to a D input terminal in the D flip-flop array. Start signal is delayed only by an integral multiple of the buffer delay $\tau$. The state of each D flip-flop is latched by the rising edge of the Stop signal. This circuit converts the time delay between the signals to a certain number of steps of buffer delay. That is, the output from the D flip-flop is obtained as a thermometer code (unary code) output showing the time delay between Start and Stop signals, and this time delay is obtained as a digital output Dout using a thermometer-code-to-binary encoder.
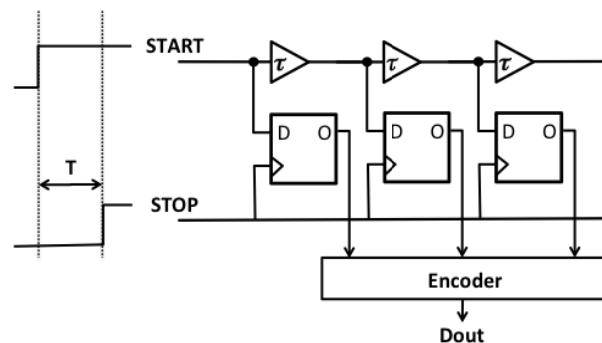


Fig.1 Flash-type TDC.

The flash-type TDC has the advantage of being able to measure a single-event input, however its disadvantages are that the time resolution is determined by the delay value $\tau$, and its circuitry is large.

## III.    DELTA-SIGMA TDC

*A. Single-bit Delta-Sigma TDC:*

We consider here how to measure the time delay between two repetitive digital signals (or clocks), and we use a $\Delta\Sigma$ TDC for the measurement. As shown in Fig.2, the time delay $\Delta T$ is long, the probability (or density) of the TDC output of "1" is high. Although arbitrary digital timing signals cannot be measured with the $\Delta\Sigma$ TDC, it can measure the timing of two clocks where time resolution is inversely proportional to measurement time. The longer the measurement time is, the finer the time resolution is.

Fig.3 shows a single-bit $\Delta\Sigma$ TDC architecture. It consists of a delay element, three multiplexers, an analog integrator, and a comparator. Its inputs are two clock signals CLK1 and CLK2 with the same frequency, and it measures the time difference T of their clock timing edges. In this design, the TDC output as the time difference is positive when the CLK1

rising edge is earlier than CLK2 and it is negative when the CLK1 edge is later. The number of 1's of the comparator output for a given time is proportional to the time difference between CLK1 and CLK2 when CLK1 is earlier. Similarly the number of 0's is proportional to their time difference when CLK2 is earlier.
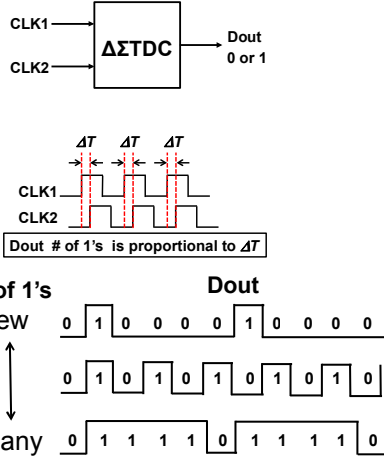


Fig. 2 Single-bit ΔΣ TDC input and output interfaces



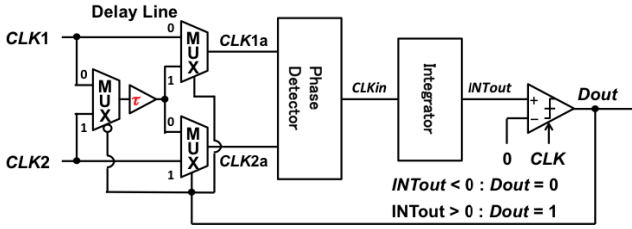Fig.3 Single-bit ΔΣ TDC.

*B. Multi-bit Delta-Sigma TDC:* Next we describe a multi-bit ΔΣ TDC, and Fig.4 shows its architecture. In the case of the multi-bit ΔΣ TDC, a flash-type A/D converter (precisely, an array of comparators) is used instead of a single comparator, and its digital output is in a thermometer code (unary code) format. The same number of delay elements as that of the comparators are used: in case of an N-bit ΔΣ TDC, $2^N - 1$ comparators and delay elements are used. Since the integrator output INTout is digitized with an array of comparators (a flash ADC without an encoder), its output Dout is in a thermometer code format. Then the digital output in a thermometer code is fed into select signals of an array of multiplexers.

Note that the integrator output INTout is digitized with fine voltage resolution with an array of comparators, and hence the multi-bit ΔΣ TDC can obtain fine time resolution compared to the single-bit one for a given measurement time. In other words, the multi-bit ΔΣ TDC takes shorter measurement time for a given time resolution than the single-bit one, which means lower testing cost. However, the multi-bit ΔΣ TDC may suffer from mismatches among delay units,

which degrades the TDC linearity (which is similar to the multi-bit ΔΣ ADC [7]).
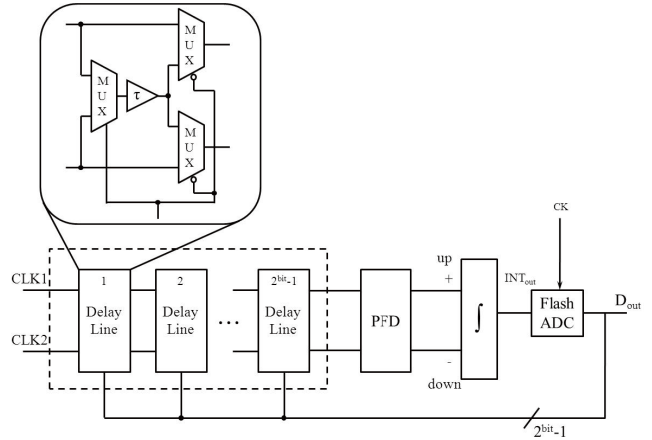


Fig.4 Multi-bit ΔΣ TDC.

*C. Multi-bit Delta-Sigma TDC With DWA:* Next we show our proposal of applying the DWA algorithm [12]-[15] to the multi-bit ΔΣ TDC for its linearity improvement. The boxed area in Fig.5 shows a digital-to-time converter (DTC) in a ΔΣ TDC, and the comparators outputs are feedback and select the corresponding delay cells in the DTC. There is delay value variation among delay cells in actual circuits, and it causes the nonlinearity error of the overall TDC. Then, we propose to apply the DWA algorithm to the multibit ΔΣ TDC. [7]-[10]

The boxed area in Fig.5 shows a delay line composed of delay cells controlled digitally (or a digital-to-time converter: DTC) and the outputs of the comparators are fed-back to select the corresponding delay cells in the DTC. There is delay value variation among delay cells in actual circuits, and it causes the nonlinearity error of the overall TDC. Then, we propose to apply the DWA algorithm to the multi-bit *ΣΔ* TDC to noise-shape the mismatch effects among the delay cells. Fig.5 shows an operation of the DWA logic; it shows the selection of the delay cells whose upper path is delayed by *τ* when the flash ADC (without encoder) outputs are 4, 3, 2, 2, 5, 3, 4, 6, ... sequentially. In other words, it performs the right rotation shift of the *ΣΔ* TDC comparator outputs in a thermometer code as follows:

1. The first input starts at the delay cell 0.
2. Next input starts at the position of the delay cell 4 shifted by 4 (the previous input) from the previous position the delay cell 0.
3. Next input starts at the delay cell 7 that shifted by 3 (the previous input) from the previous position Cell 4, and rotated.

Fig.7 shows an operation example without and with DWA for a multi-bit ΔΣ TDC.

Generalized algorithm description is as follows:
we have N delay elements (delay cell 0, delay cell 1, ..., delay cell N-1) and a pointer $P(n)$ at time $n$ (where $P(0) = 0$).
1.  Suppose that the input data $C1(n) = Cn$ at time $n$ (where $n = 0, 1, 2, 3, 4, ...$).

2. Select *Cn* delay cells of *modN(P(n)+1)*,
   *modN(P(n)+2), ..modN(P(n) + Cn)*.
3. Set the pointer at time *n+1* to
   *P(n+1) = modN(P(n)+Cn)*.

The above procedure is repeated for *n = 0, 1, 2, ...* This is the *ΔΣ* operation (Fig.8), and suppresses errors (caused by the delay cell mismatches) in DC component and pushes it in the high frequency side (Fig.9).
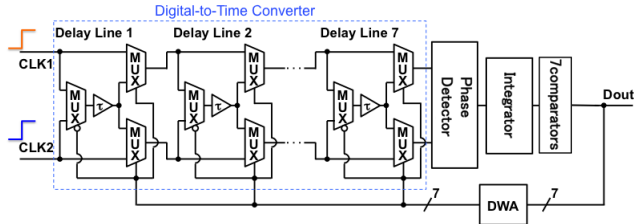

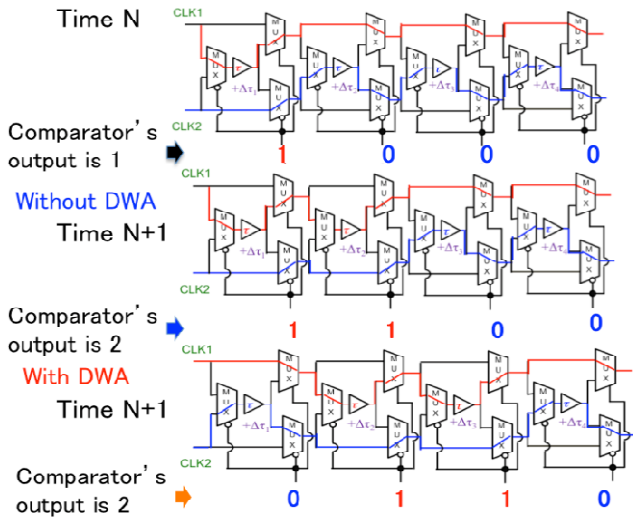
Fig.5. 3-bit ΔΣ TDC with DWA logic



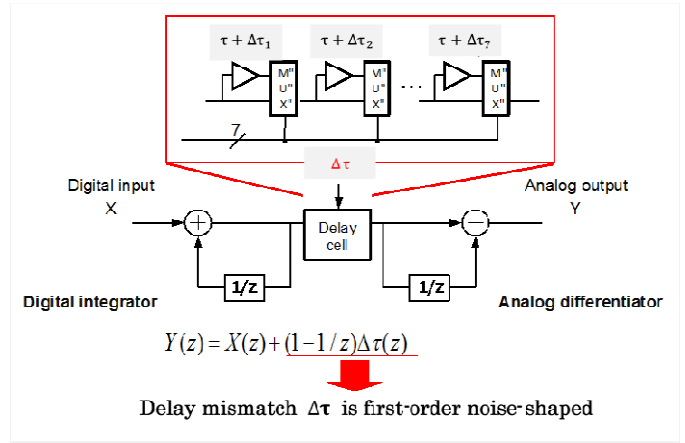Fig.6. DWA algorithm



Fig.7. Delay cell selection without and with DWA.



$$Y(z) = X(z) + (1 - 1/z)\Delta\tau(z)$$

Delay mismatch Δτ is first-order noise-shaped

Fig.8. Equivalent circuit to DWA logic.



Fig.9. First-order noise-shaping of delay cell mismatch effects with DWA.

## IV. ANALOG FPGA IMPLEMENTATION

We have implemented the 3-bit ΔΣ TDC in Fig.3 using an analog FPGA (Programmable System-on-Chip: PSoC, Cypress Semiconductor), and its photo is shown Fig.10. As shown in Fig.11, the core circuit employs pseudo differential structure. Each delay cell consists of a resistor, a capacitor and a buffer; the value of each resistor can be changed externally and individually to give delay variation intentionally so that DWA effectiveness can be evaluated. Also we can select usage or no usage of DWA by a command.
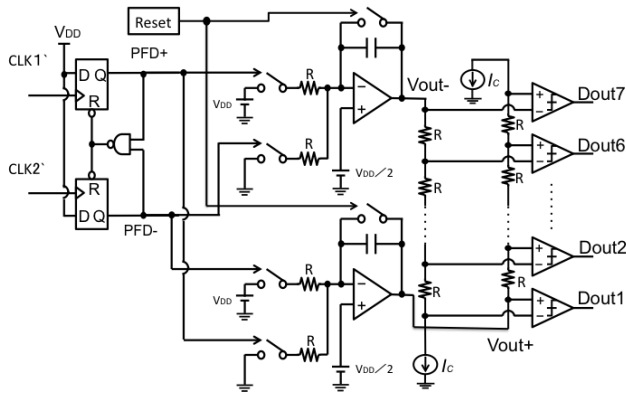


Fig.10. 3-bit ΔΣ TDC implementation with an analog FPGA

Fig.11. Core circuit design of 3-bit ΔΣ TDC with an analog FPGA.

## V. MEASUREMENT RESULTS

Figures 12, 13, 14 and 15 show the measurement results of the 3-bit ΔΣ TDC with and without DWA for several delay variation cases. We see from them that the DWA algorithm improves the overall multi-bit ΔΣ TDC linearity.

In the analog FPGA implementation of the 3-bit ΔΣ TDC, each delay ($\tau 1$, $\tau 2$,…, $\tau 7$) is implemented with external resistor and capacitor. Each resistor of different value can be placed to vary each delay (or cause delay mismatches) intentionally to demonstrate the effectiveness of the DWA algorithm. Resistor values (Ω) for delays ($\tau 1$, $\tau 2$,…, $\tau 7$) in each case are given as follows:

Case 1 (Fig. 12) :    75,   150,   75,   75,   75,   75,   75

Case 2 (Fig. 13) :    75,   75,   150,   75,   75,   75,   75

Case 3 (Fig. 14) :    75,   75,   75,   150,   75,   75,   75

Case 4 (Fig. 15) :  220,   75,   150,   220,   75,   150,   220

The number of the TDC output data is 10,000 for the measured data in Figs. 12 - 15.

Note that the delay value for R=75Ω is around 110ns, and when all delays are 110ns, the input range is from -660ns to 660ns.

We see from Figs. 12-15 that the overall TDC linearity is degraded without DWA at the input of the time difference

  around -550ns in case 1

  around -440ns  in case 2

  around 0ns in case 3, and

  in the whole  input range  in case4.

However  it is recovered by adopting DWA algorithm.

## VI. CONCLUSION

We have described multi-bit ΔΣ TDC design and implementation on an analog FPGA as well as measurement results for fast and high accuracy testing of the timing between two clocks. We have proposed applying a DWA technique to reduce the effects of delay mismatches among delay cells, an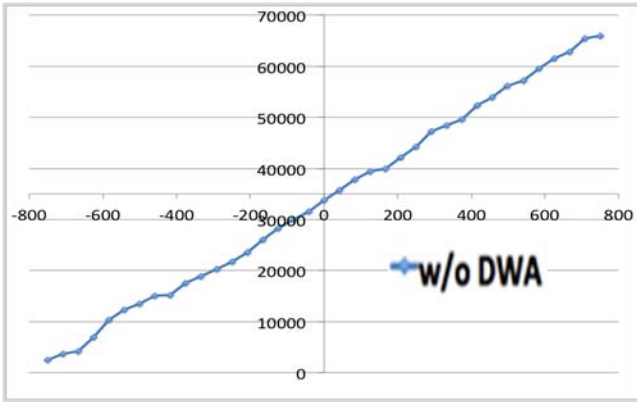d our measurement results validate the effectiveness of our proposed approach. Our proposed circuits are simple but enable fast and accurate testing, and hence we expect to use them as DFT, BIST or BOST for clock timing measurement and testing.
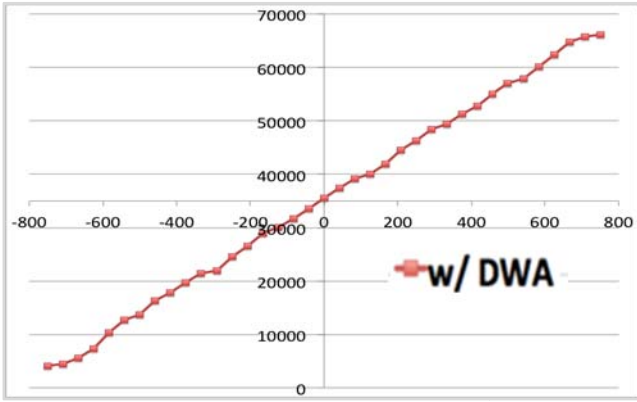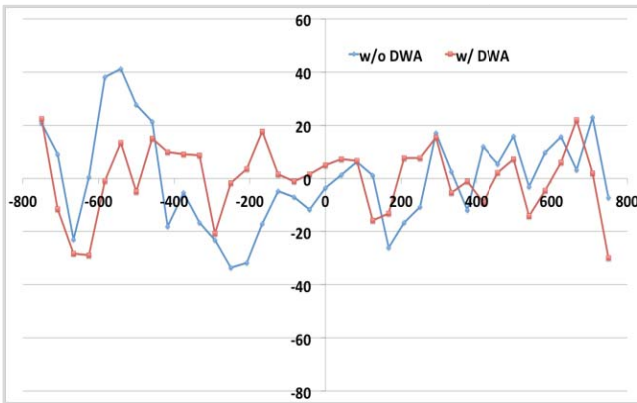
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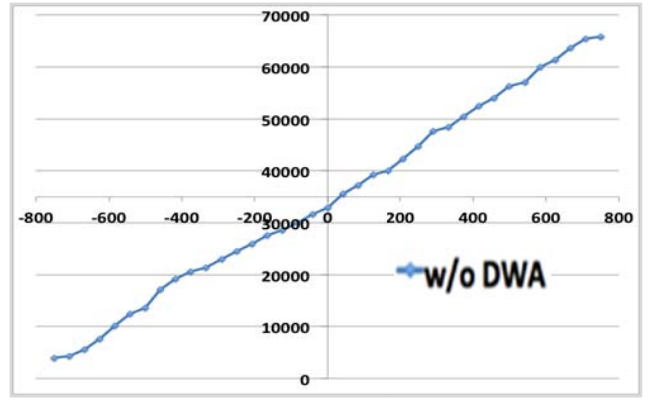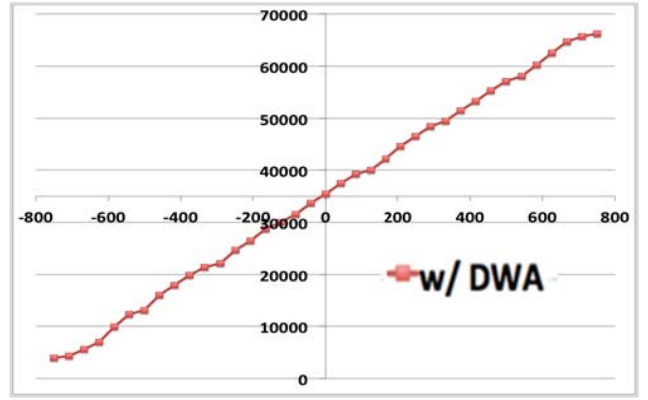
(a)　Without DWA
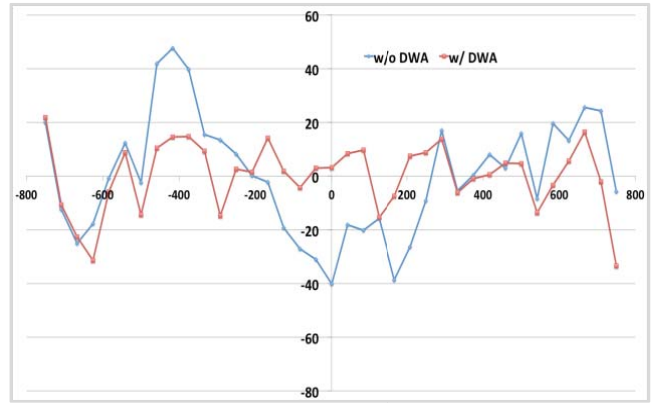


(b)　With DWA



**(c)**　INL with and without DWA

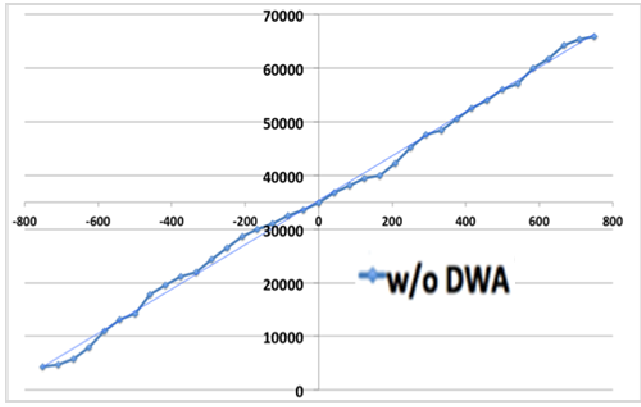Fig.12. Measurement result for the 3-bit ΔΣ TDC (case 1)



(a)　Without DWA



(b)　With DWA



(c)　INL with and without DWA

Fig.13. Measurement result for the 3-bit ΔΣ TDC (case 2)
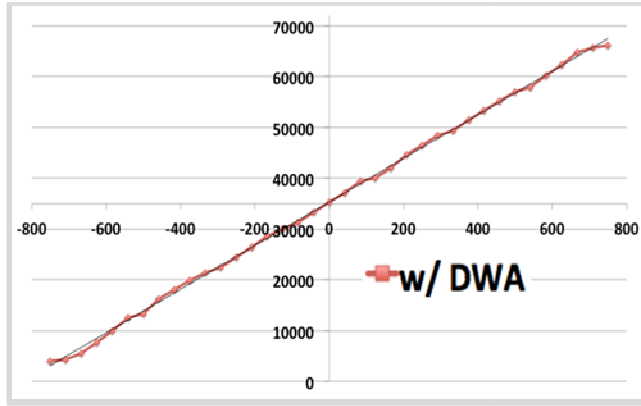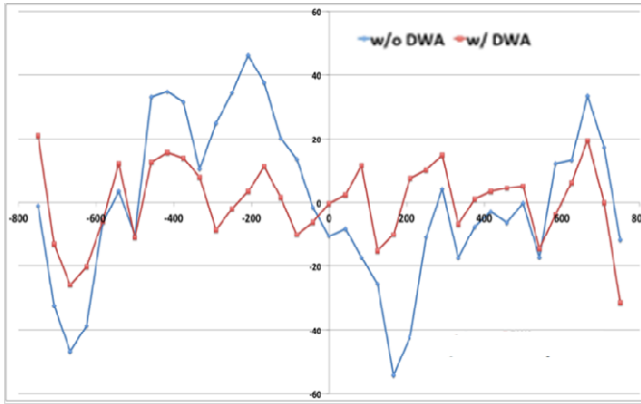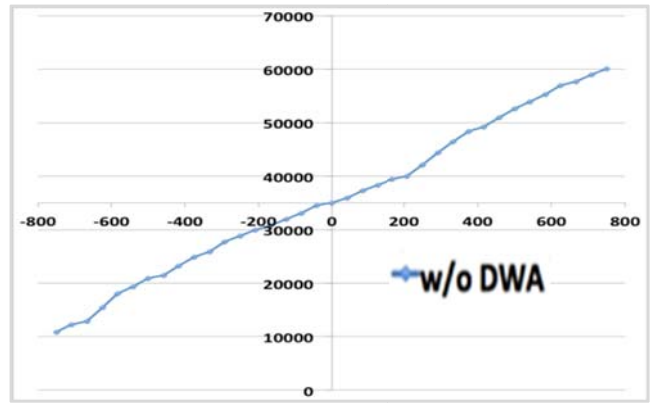
(a)   Without DWA



(b)   With DWA



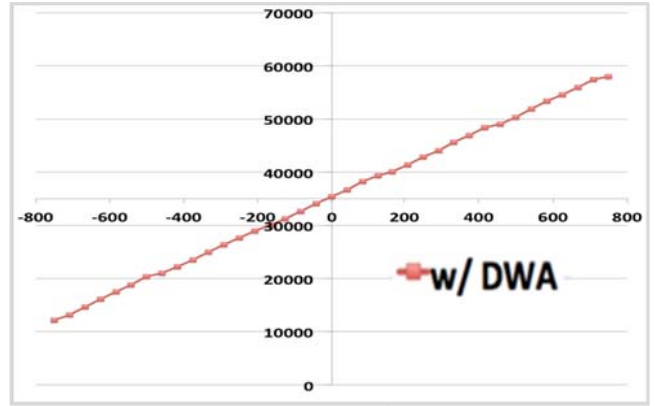(c)   INL with and without DWA
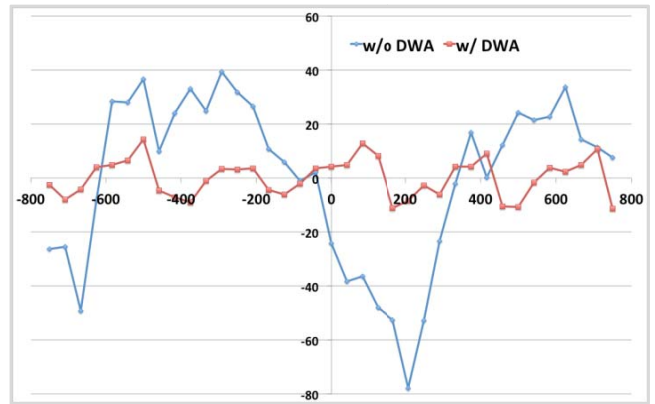
Fig.14. Measurement result for the 3-bit ΔΣ TDC (case 3)



(a)   Without DWA



(b)   With DWA



(c)   INL with and without DWA

Fig.15. Measurement result for the 3-bit ΔΣ TDC (case 4)