Linearity Improvement Technique of Multi-bit Sigma-Delta TDC for Timing Measurement

Yuta Arakawa, Yusuke Oosawa, Haruo Kobayashi, Osamu Kobayashi†
Division of Electronics and Informatics, Gunma University, Kiryu 376-8515 Japan email: k_haruo@el.gunma-u.ac.jp
† Semiconductor Technology Academic Research Center (STARC), Yokohama 222-0033 Japan

***Abstract*— This paper describes the architecture and operation of a sigma-delta ($\Sigma\Delta$) time-to-digital converters (TDC) for high-speed I/O interface circuit test applications; they offer good accuracy with short testing time. In particular, we describe multi-bit $\Sigma\Delta$ TDC architecture for fast testing. However, mismatches among delay cells in delay lines degrade the linearity there. Then we investigate additional calibration methods to improve the overall TDC linearity: delay-cell sorting algorithms and their combination with data-weighted averaging (DWA) algorithm. Our Matlab simulation results demonstrate the effectiveness of our proposed approach.**

I. Introduction

High-speed I/O interfacing circuits such as for double-data-rate (DDR) memory interfaces are very important, and low-cost, high-quality testing of such circuits is challenging [1]. This paper describes simple test circuitry for measuring digital signal timing (such as DDR memory interface signal timing) with high resolution and good accuracy. We focus on Time-to-Digital Converter (TDC) applications of $\Sigma\Delta$ modulators (for fine-timing-resolution, digital output, and simple circuitry) and with multi-bit architecture (for short testing time).

A multi-bit $\Sigma\Delta$ TDC can suffer from delay mismatches among delay cells, but we propose a technique to solve this problem and maintain good accuracy: combination delay-cell sorting and its combination with data-weighted averaging (DWA) algorithm. We have already proposed two techniques in [2], [4] to improve the linearity of the multi-bit $\Sigma\Delta$ TDC; (i) DWA and (ii) self-calibration.

1) The DWA technique is simple and effective for small variation among delay cells. However, the delay cell variation among delay cells may be relatively large (though it depends on circuit implementation), and in such a case only DWA may not be enough.
2) On the other hand, the self-calibration [4] with the delay cell measurement using a ring oscillator can be accurate but it requires large DSP overhead.

In this paper, we propose the delay-cell sorting algorithms (such as [5]) and their combination with data-weighted averaging (DWA) algorithm, and show with simulation how effective they for large variation with relatively small circuit.

II. Sigma-Delta TDC

A. TDC Architecture Comparison

TDC can be used to measure digital signal timing, and there are several TDC architectures.

Flash-type TDC : The architecture of a basic flash-type TDC is shown in Fig.1 [6]. It consists of a delay-line using delay cells in the signal path and an array of flip-flops. The input **Start** signal passes along the delay cells, which are connected in series. And then each signal is connected to a D input terminal in the D flip-flop array. **Start** signal is delayed only by an integer multiple of the buffer delay τ. The state of each D flip-flop is latched by the rising edge of the **Stop** signal. This circuit converts the time delay between the signals to a certain number of steps of buffer delay. That is, the output from the D flip-flop is obtained as a thermometer code (unary code) output showing the time delay between **Start** signal and **Stop** signal, and this time delay is obtained as a digital output D_{out} using a thermometer-code-to-binary encoder.

The flash-type TDC has the advantage of being able to measure a single-event input, however its disadvantages are that the time resolution is determined by the delay value τ, and its circuitry is large.

Vernier-type TDC : Fig.2 shows a vernier-type TDC which uses two delay lines: one, with a buffer delay of τ_1, for the reference edge, and the other, with a buffer delay of τ_2, for the edge under measurement. Time resolution is given by $\tau_1 - \tau_2$ (gate delay difference) which can be smaller than that of the basic TDC, but note that it uses 2N buffers (N buffers of τ_1 and N buffers of τ_2) for an input range from 0 to N ($\tau_1 - \tau_2$).

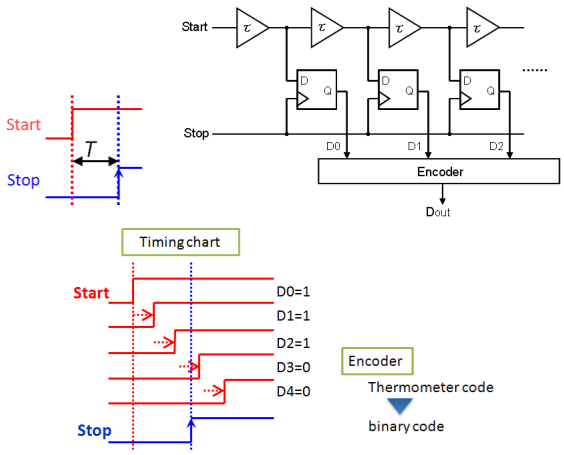


Fig. 1. Flash-type TDC architecture and operation.

We consider here how to measure the time delay between two repetitive digital signals (or clocks), and we use a $\Sigma\Delta$

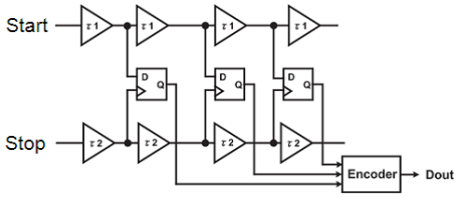


Fig. 2. Vernier-type TDC.

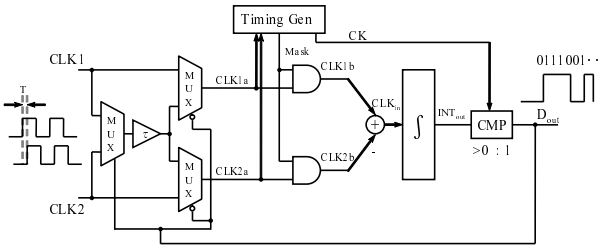


Fig. 3. A single-bit ΣΔ TDC (Matlab simulation model).

TDC for the measurement. Although arbitrary digital timing signals cannot be measured with the ΣΔ TDC, it can measure the timing of two clocks where time resolution is inversely proportional to measurement time. The longer the measurement time, the finer the time resolution. We consider here the use of a multi-bit architecture for short testing time, and the use of DWA or self-calibration of the delay cell elements for good accuracy.

Remark (i) Flash-type and vernier-type TDCs can measure timing difference between two digital signals of *single event*. However a ΣΔ TDC can measure it only for *repetitive* two clocks.
(ii) ΣΔ TDCs have been studied recently [7], [8], [9], [10] mainly for all-digital PLL circuits. In this research, we consider to use them for digital signal timing measurement and testing.

B. Single-bit Sigma-Delta TDC

Fig.3 shows a single-bit ΣΔ TDC architecture for our Matlab simulation. It consists of a delay element, three multiplexers, an analog integrator, and a comparator. Its inputs are two clock signals $CLK1$ and $CLK2$ with the same frequency, and it measures the time difference T of their clock timing edges.

In this design, the TDC output as the time difference is positive when the $CLK1$ rising edge is earlier than $CLK2$ and it is negative when the $CLK1$ edge is later. The number of 1's of the comparator output for a given time is proportional to the time difference between $CLK1$ and $CLK2$ when $CLK1$ is earlier. Similarly the number of 0's is proportional to their time difference when $CLK2$ is earlier. Its operation is as follows:

1) When the comparator output is "1", $CLK1$ is delayed by τ while $CLK2$ is not delayed. When the comparator

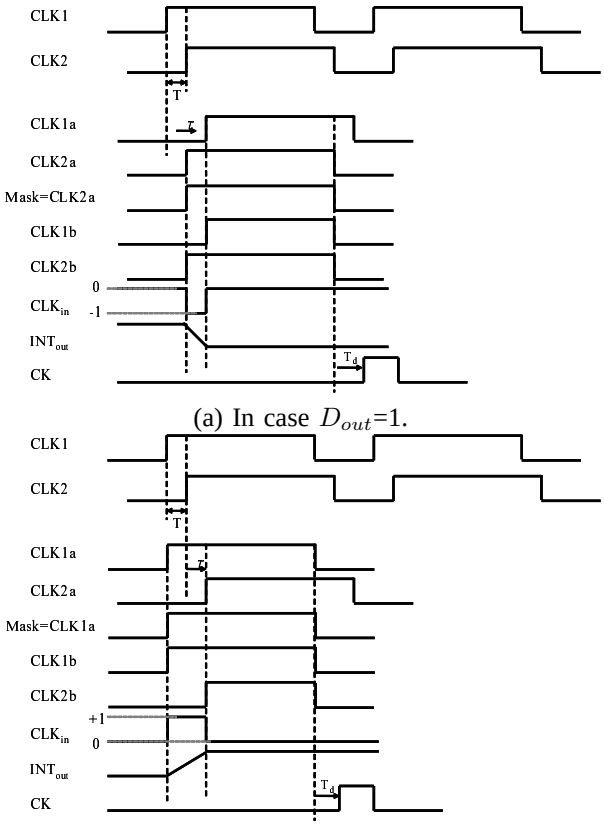


Fig. 4. Timing diagram of a single-bit ΣΔ TDC.

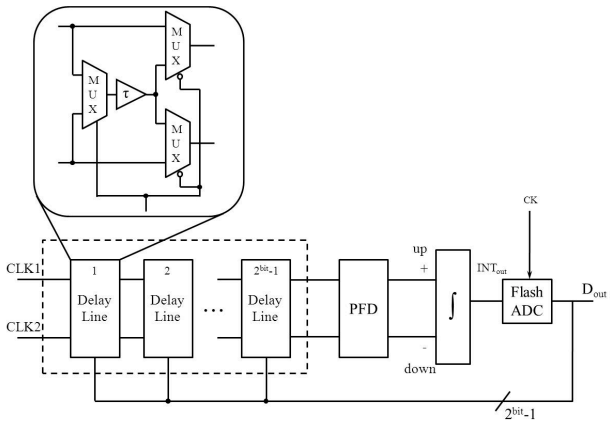


Fig. 5. Architecture of a multi-bit ΣΔ TDC. PFD stands for phase frequency detector.

output is "0", $CLK1$ is not delayed, while $CLK2$ is delayed by τ.

2) The clock signals acquired as the result are defined as $CLK1a$ and $CLK2a$, respectively.
3) Mask signal (generated in "Timing Generator") is the same as $CLK1a$ when $CLK1a$ comes earlier than $CLK2a$; otherwise it is the same as $CLK2a$.
4) $CLK1b$ is logical AND of Mask signal and $CLK1a$, while $CLK2b$ is logical AND of Mask signal and $CLK2a$.
5) We produce the time delay signal CLK_{in} between $CLK1b$ and $CLK2b$ and convert it to the voltage signal with subtraction CLK1b from CLK2b in analog domain, and feed it to the integrator whose output is INT_{out}.
6) The comparator examines (at the rising edge of CK which is delayed by T_d from the falling edge of Mask signal) whether the integrator output INT_{out} is larger than "0" or not. Its output D_{out} is that of the $\Sigma\Delta$ TDC and fedback to the multiplexers.

Fig.4 shows timing diagram of the signals.

C. Multi-bit Sigma-Delta TDC

Next we describe the multi-bit $\Sigma\Delta$ TDC, and Fig.5 shows its architecture. In the case of the multi-bit $\Sigma\Delta$ TDC, a flash-type A/D converter (precisely, an array of comparators) is used instead of a single comparator, and its digital output is in a thermometer code (unary code) format. The same number of delay elements as that of the comparators are used: in case of an N-bit $\Sigma\Delta$ TDC, $2^N - 1$ comparators and delay elements are used.

Since the integrator output INT_{out} is digitized with an array of comparators (a flash ADC without an encoder), its output D_{out} is in a thermometer code format. Then the digital output in a thermometer code is fed into select signals of an array of multiplexers.

Note that the integrator output INT_{out} is digitized with fine voltage resolution with an array of comparators, and hence the multi-bit $\Sigma\Delta$ TDC can obtain fine time resolution compared to the single-bit one for a given measurement time. (This statement is supported by our previous work [2].) In other words, the multi-bit $\Sigma\Delta$ TDC takes shorter measurement time for a given time resolution than the single-bit one, which means lower testing cost.

However, the multi-bit $\Sigma\Delta$ TDC may suffer from mismatches among delay units, which degrades the TDC linearity (which is similar to the multi-bit $\Sigma\Delta$ ADC [11], [13], [14]).

In case of a 3-bit $\Sigma\Delta$ TDC, 7 delay cells are uses and we denote the delay value as τ_k for the k-th delay cell (k=1,2,..,7). Then we define the average delay τ as follows:

$$\tau = \frac{1}{7}\sum_{k=1}^{7}\tau_k. \quad (1)$$

Also we define the delay variation τ_k for the k-th delay cell:

$$\Delta\tau_k = \tau_k - \tau. \quad (k = 1, 2, 3, ..., 7). \quad (2)$$

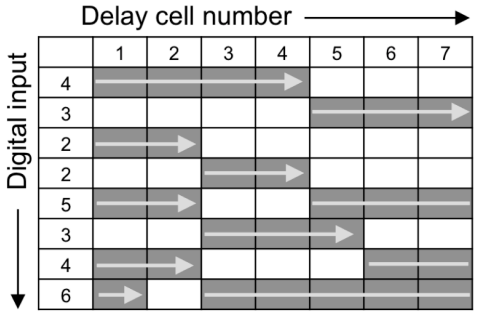


Fig. 6. Operation of DWA logic.

These $\Delta\tau_k$'s cause nonlinearities of the overall TDC if we do not take care of them. Notice that we have the following from eqs. (1), (2):

$$\sum_{k=1}^{7}\Delta\tau_k = 0. \quad (3)$$

Remark

(i) A DAC inside a $\Sigma\Delta$ ADC is replaced with a delay-line (or digital-to-time converter: DTC) in a $\Sigma\Delta$ TDC and the DAC is not used there, so that we need only consider the nonlinearity of the multi-bit DTC in the multi-bit $\Sigma\Delta$ TDC.
(ii) The delay τ determines the input range of the $\Sigma\Delta$ TDC; the time resolution of the $\Sigma\Delta$ TDC is determined not only by τ but also by the measurement time length (the number of the comparisons of the ADC inside the modulator).
(iii) The input range of a single-bit $\Sigma\Delta$ TDC time range is from - τ to τ. But for example, a 3-bit $\Sigma\Delta$ TDC time range is from - 8τ to 8τ; hence the delay value of the 3-bit $\Sigma\Delta$ TDC should be designed to one-eighth of that of the single-bit $\Sigma\Delta$ TDC. (if necessarily, a vernier-type delay line can be used to realize effectively fine τ.)
(iv) The nonlinearity of the flash ADC does not affect the overall TDC linearity, because the flash ADC lies in the forward path and its quantization noise is noise-shaped [11].

III. Multi-bit Sigma-Delta TDC with DWA

This section shows our proposal of applying the DWA algorithm to the multi-bit $\Sigma\Delta$ TDC for its linearity improvement. The DWA algorithm is a well-known technique in $\Sigma\Delta$ ADC/DAC [11], [13], [14], but our application to multi-bit $\Sigma\Delta$ TDCs in [2], [4] would be the first attempt, to our knowledge.

The boxed area in Fig.5 shows a delay line composed of delay cells controlled digitally (or a digital-to-time converter: DTC) and the outputs of the comparators are fed-back to select the corresponding delay cells in the DTC.

There is delay value variation among delay cells in actual circuits, and it causes the nonlinearity error of the overall TDC. Then, we propose to apply the DWA algorithm to the multi-bit $\Sigma\Delta$ TDC to noise-shape the mismatch effects among the delay cells. Fig.6 shows an operation of the DWA logic; it shows the selection of the delay cells whose upper path is delayed

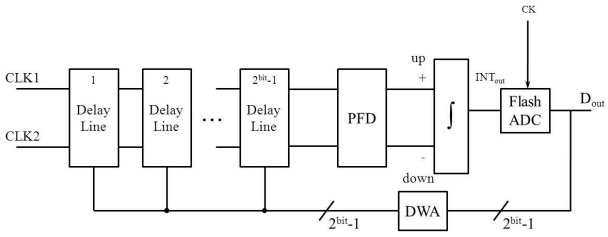
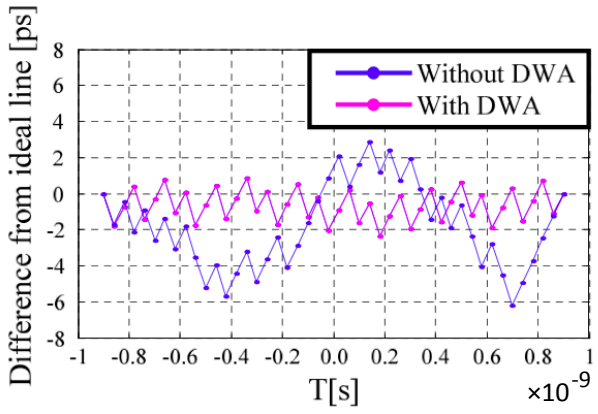


Fig. 7. Architecture of a multi-bit ΣΔ TDC with DWA logic.

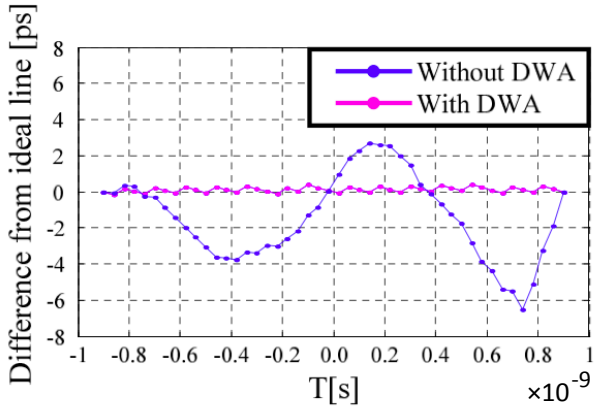
TABLE I

PARAMETERS OF DELAY VALUES FOR SIMULATION (UNIT IS [NS]).

	$\tau 1$	$\tau 2$	$\tau 3$	$\tau 4$
Delay values(Ideal)	0.145	0.145	0.145	0.145
Delay values(Actual)	0.140	0.149	0.148	0.143
	$\tau 5$	$\tau 6$	$\tau 7$	Total of τ
Delay values(Ideal)	0.145	0.145	0.145	1.015
Delay values(Actual)	0.145	0.148	0.146	1.019



(a) In case 99 times.



(b) In case 599 times.

Fig. 8. INL with and without DWA (Matlab simulation results).

by τ when the flash ADC (without encoder) outputs are 4, 3, 2, 2, 5, 3, 4, 6, ... sequentially. In other words, it performs the right rotation shift of the ΣΔ TDC comparators outputs in a thermometer code as follows:

1) The first input starts at the delay cell 1.
2) Next input starts at the position of the delay cell 5 shifted by 4 (the previous input) from the previous position the delay cell 1.
3) Next input starts at the delay cell 1 that shifted by 3 (the previous input) from the previous position Cell 5, and rotated.

Generalized algorithm description is as follows: we have N delay elements (delay cell 0, delay cell 1, ..., delay cell N-1) and a pointer $P(n)$ at time n (where $P(0) = 0$).

1) Suppose that the input data $C_1(n) = c_n$ at time n (where $n = 0, 1, 2, 3, 4, ...$).
2) Select c_n delay cells of $mod_N(P(n)+1), mod_N(P(n)+2), ..mod_N(P(n)+c_n)$.
3) Set the pointer at time $n+1$ to $P(n+1) = mod_N(P(n)+c_n)$.

The above procedure is repeated for $n = 0, 1, 2, ...$ This is the ΣΔ operation [14], and suppresses errors (caused by the delay cell mismatches) in DC component and pushes it in the high frequency side.[11], [12], [13], [14]

Fig.7 shows a block diagram of the multi-bit ΣΔ TDC with DWA logic. The outputs of the comparator array are fed into DWA logic and their outputs are given to the multiplexers as select signals in the DTC.

We have performed Matlab simulation for a 3-bit ΣΔ TDC with DWA logic. Simulation conditions are given in Table I. The time difference between input clocks used for the simulation is from -0.9ns to 0.9ns.

Figs.8 (a) and (b) show the difference between an ideal line and the simulated result (i.e., the integral non-linearity: INL). Fig.8 (a) is the result in case that the number of comparison times (number of samplings) is 99, and Fig.8 (b) is when it is 599. We see that the INL is large without DWA, however when DWA is employed, it is small and the TDC linearity is improved.

IV. DELAY CELL SORTING

We discuss here delay cell sorting techniques. First note that the value of k-th delay cell τ_k can be measured with the ring oscillator configuration (Figs. 9, 10). We can measure the order from the smallest to the largest delay cell values with a digital method as described in our paper [4].

A. Sorting Algorithm 1

Now we discuss the switching sequence post adjustment (SSPA) algorithm [5] for delay cell sorting. The SSPA is a calibration method that can changes the switching sequence of delay cells especially after fabrication process, and a very good integral linearity of the delay cell line (or digital-to-time converter) can be obtained. Its algorithm is as follows (Fig.11):

1) The delay cells are measured using the method in Fig.10 and sorted from the lowest to the highest order.

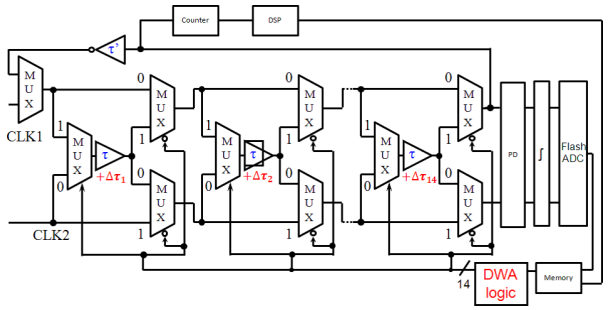


Fig. 9. Circuit configuration of our proposed method.

2) Then, the sorted delay cells are rearranged by arranging small delay cells between two large cells.
3) After that, each two neighboring delay cells are summed.
4) Then summed delays are again measured and sorted as 1).
5) They are rearranged as 2).
6) Finally, the final sequence is obtained.

B. Sorting Algorithm 2

We propose here a 2-step SSPA algorithm, which uses, e.g., 14 delay cells and combine two to make 7 delay cells and also use the SSPA algorithm: their combinations are done so that each two-combined cell delay value is close to each other as much as possible (Fig.12).

By setting the memory values (Fig.13), we can arrange the switching for the multiplexers according to the flash ADC output inside the modulator.

Remark : We can have redundant delay cells. For example, we have 16 delay cells and discard two cells with the largest and the smallest delays, and we perform the same method to the remaining 14 delay cells as described above.

V. Simulation Results

We have performed Matlab simulation for the 3-bit $\Sigma\Delta$ TDC in several variation cases (the standard deviation is up to 10%) and compared its linearity without and with the sorting.

Fig.14 shows one of the simulation results with conditions in Table II with only DWA and with both DWA and sorting.

We found that in most cases the linearity is improved when our sorting algorithms are used; Fig.15 shows the simulation results with sorting algorithm 2 (but no DWA) and without sorting nor DWA in 18 cases of delay values variations (horizontal axis). We see that sorting algorithm 2 improves the averaged INL (indicated in vertical axis).

Fig.16 shows simulated linearity for possible combinations of sorting algorithms 1, 2 and DWA in 5 cases of delay cell variations when the number of TDC output data is 1,000. We see that the sorting algorithms are effective though the circuit becomes a little bit complicated.

Fig.17 shows the simulated linearity for possible combinations of sorting algorithms 1, 2 and DWA with respect to the number of TDC output data. We see that as the number increases, the linearity is improved.

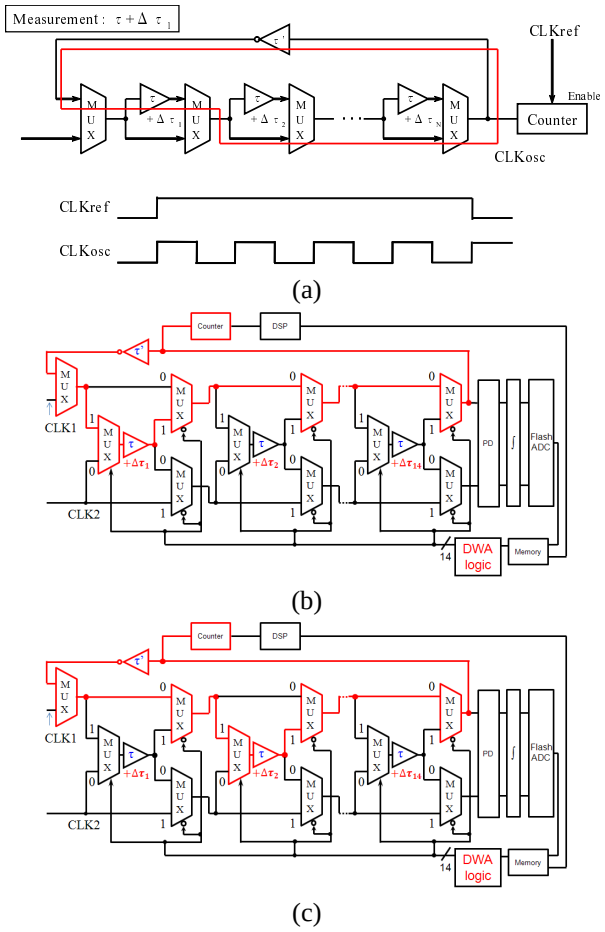


Fig. 10. (a) Self-measurement of delay values with a ring oscillator configuration. (b) $\tau + \Delta\tau_1$ measurement. (c) $\tau + \Delta\tau_2$ measurement.

In summary we have the following observation from our simulation results:

1) The sorting algorithm 2 is the most effective.
2) The sorting algorithm 1 is the second.
3) The DWA algorithm is the third.
4) Effectiveness of applying DWA after sorting algorithm 1 (or 2) is almost the same as only applying the sorting algorithm 1(or 2, respectively).
5) As the number of the TDC output data increases, the linearity improves in all cases.

Remark : The standard deviation of capacitor mismatches in a multi-bit DAC in a multi-bit $\Sigma\Delta$ ADC would be approximately 0.1% [11]. However, that of the delays can be much larger (though it depends on circuit implementation) and in this case the DWA algorithm may not be enough; Applying the sorting algorithms may need to be considered with the penalty of small hardware overhead.

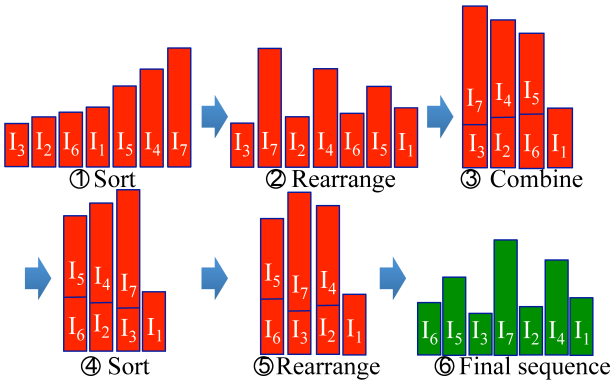


Fig. 11. Explanation of the switching sequence post adjustment algorithm.

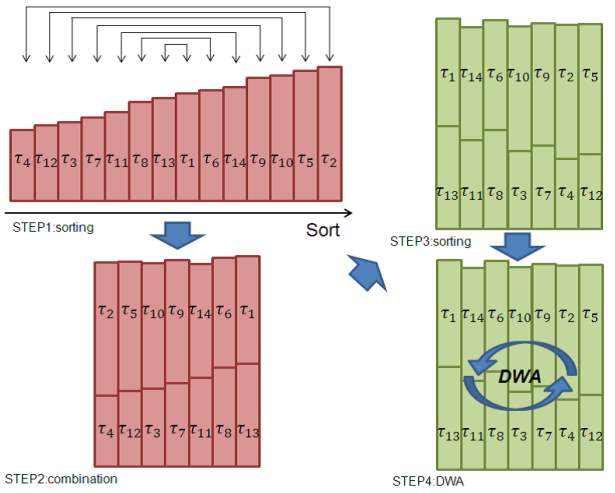


Fig. 12. Step 1: Delay cell sorting. Step 2: Two-delay-cell combination. Step 3: Combined two-delay-cell sorting. Step 4: Applying DWA algorithm after sorting.

STEP2:combination

ADRESS	D2	D1	D0	τ1	τ2	τ3	τ4	τ5	τ6	τ7	τ8	τ9	τ10	τ11	τ12	τ13	τ14
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
3	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
4	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
6	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
7	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0

STEP3:sorting

ADRESS	D2	D1	D0	τ1	τ2	τ3	τ4	τ5	τ6	τ7	τ8	τ9	τ10	τ11	τ12	τ13	τ14
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0
2	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	1
3	0	0	0	1	0	0	0	0	1	0	1	0	0	1	0	1	1
4	0	0	0	1	0	1	0	0	1	0	1	0	1	1	0	1	1
5	0	0	0	1	0	1	0	0	1	1	1	1	1	1	0	1	1
6	0	0	0	1	1	1	1	0	1	1	1	1	1	1	0	1	1
7	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Fig. 13. Delay cell combination and sorting data stored in memory for switching the multiplexers.

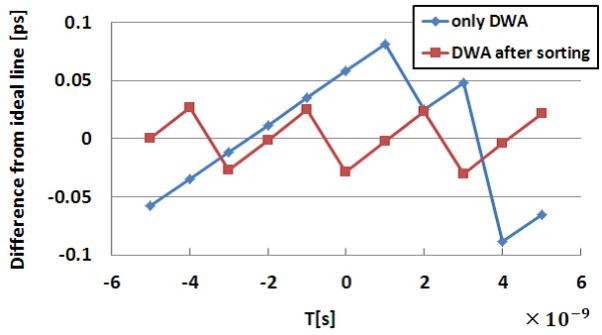


Fig. 14. INL (rms) simulation result comparison with only DWA and with DWA after the sorting algorithm 2.

TABLE II

DELAY CELL VALUES USED IN SIMULATION.

	τ1	τ2	τ3	τ4
Delay values	0.94	1.00	0.99	0.99
	τ5	τ6	τ7	τ8
Delay values	1.09	1.09	1.01	0.99
	τ9	τ10	τ11	τ12
Delay values	0.93	1.03	0.94	0.99
	τ13	τ14		Total of τ
Delay values	0.97	1.02		13.98

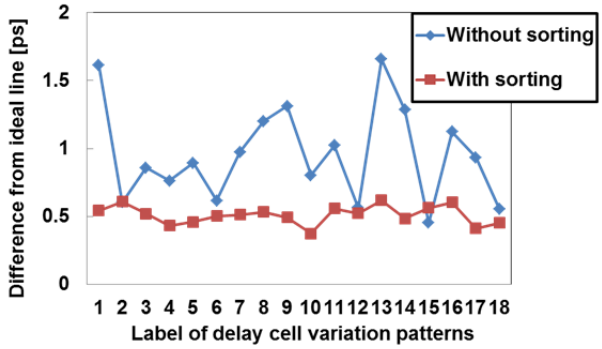


Fig. 15. Averaged (rms) integral nonlinearity with and without sorting algorithm 2 in 18 cases of delay cell variations.

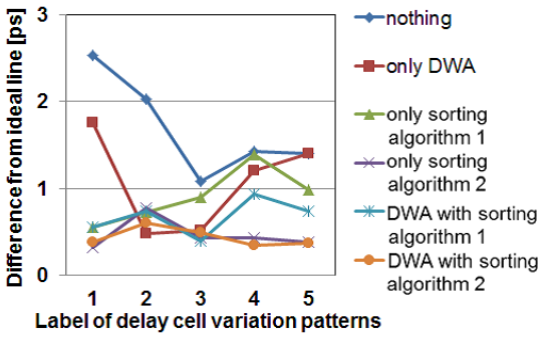


Fig. 16. Simulated TDC INL (rms) for all possible combinations of sorting algorithms 1, 2 and DWA in 5 cases of delay cell variations.

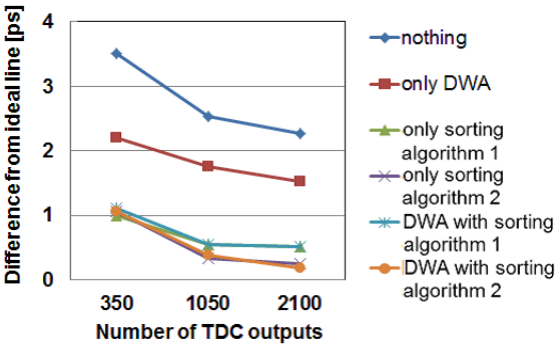


Fig. 17. Simulated TDC INL (rms) for all possible combinations of sorting algorithms 1, 2 and DWA with respect to the number of TDC output data.

VI. Conclusions

We have described multi-bit ΣΔ TDC architecture for fast and high accuracy testing of the timing between two clocks. We have proposed techniques to reduce the effects of delay mismatches among delay cells: delay cell sorting algorithms and their combination with the DWA algorithm. Delay measurement for our delay cell sorting can be done easily since the signal is "time" rather than "voltage. Our simulation results show that the correction techniques can improve linearity of the multi-bit ΣΔ TDC.

Our proposed techniques are simple but enable fast and accurate testing, and hence we expect to use it as Design-for-Testability (DFT), Built-In Self-Test (BIST) or Built-Out Self-Test (BOST) [1], [15], [16], [17] for clock timing measurement and testing.

We close this paper by remarking that the ΣΔ TDC can be also used for phase noise testing of the clock; its phase noise frequency characteristics can be easily obtained by FFT of the ΣΔ TDC outputs, and our proposed method is also applicable there [18].

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