

# Fibonacci Sequence Weighted SAR ADC Algorithm and its DAC Topology

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## Abstract

This paper describes redundant successive approximation register (SAR) ADC design methods to improve reliability and conversion speed by digital error correction. Especially we show that redundant SAR ADC using Fibonacci sequence and its property called Golden ratio can be well-balanced design. We also present some simple golden-ratio-weighted DAC topologies for easy realization of the redundant SAR ADC by utilizing many interesting properties of Fibonacci sequence.

## 1. Introduction

Recently, automotive electronics are gathering attention for industry competitiveness of vehicles. SAR ADCs embedded in micro-controller for automotive electronics applications need better performance such as high reliability and high speed, and then we study here redundancy design of SAR ADCs to realize them by digital error correction [1-6].

We have shown Fibonacci-weighted redundancy SAR ADC is better than conventional redundancy SAR ADC regarding to correction-capability and conversion-speed [6]. So this paper proposes some DAC topologies with simple R-R ladder network, C-C ladder network or their combinations for the Fibonacci weighted SAR ADC. In other words, we show that the Fibonacci-weighted SAR ADC is realized easily by using simple DAC circuits using properties of Fibonacci sequence. Conventional non-binary algorithm SAR ADC is realized by using entirely unary type [1-3] or estimation of its radix [4-5], which requires complex circuit. Therefore, our proposal of using Fibonacci weighted algorithm has another advantage also in its internal DAC realization.

## 2. SAR ADC and Redundancy Design

### 2.1 SAR ADC

SAR ADCs are used for medium sampling speed and high-resolution applications. Since they have features of low power and small chip area, they are widely applied to such as automotive, factory automation. Furthermore, it does not require operational amplifiers, which is suitable for nano-CMOS implementation.

The SAR ADC consists of a sample-and-hold circuit, a comparator, a DAC, SAR logic and a timing generator (Fig. 1). For precise AD conversion, enough accuracy of the sample-and-hold circuit and the DAC is required.

Conversion of the SAR ADC is based on principle of

balance and generally it uses the binary search algorithm. Firstly, the sample-and-hold circuit acquires analog input voltage. Secondly, the comparator compares the input analog voltage and the reference voltage that is generated by the DAC and decides 1-bit digital output. Thirdly, SAR logic provides DAC input based on the comparator output. The input voltage and the updated DAC output voltage are compared by the comparator. This operation is repeated and finally SAR ADC can obtain the whole digital output. Figure 2 shows the binary search algorithm of a 4-bit SAR ADC. The bold line in Fig. 2 indicates the reference voltage value to compare with the analog input at each step. Their values are calculated by either sum or difference between the last step reference voltage and the weighted voltage  $p(k)$  of each step as shown in Fig. 2.

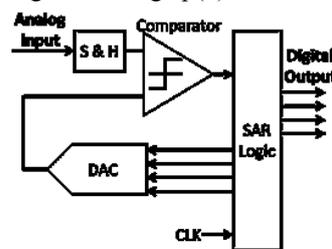


Fig.1 Block diagram of an SAR ADC.

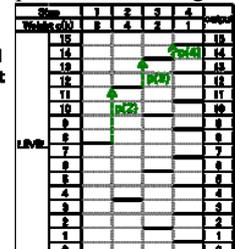


Fig. 2 Binary search algorithm of a 4-bit 4-step SAR ADC.

### 2.2 SAR ADC Redundancy Design

Redundancy design is a popular technique to improve circuit and system performance. To apply the redundancy design to the SAR ADC means adding extra comparison [1-6]. This method changes binary weights to non-binary weights for the DAC and realizes digital error correction with redundancy property.

Figure 3 shows an example of two redundant search operations of a 4-bit 5-step SAR ADC. There, the input voltage is 8.3LSB and the reference voltage weights  $p(k)$  are 1, 2, 3, 6 and 8. The one operation (solid arrows) assumes that the comparison is correct, whereas the other (dotted arrows) assumes that it is incorrect. However, both obtain the correct digital output of 8 by digital error correction. In the 4-bit 5-step SAR ADC as shown in Fig. 3, there are  $2^5$  comparison patterns and  $2^4$  output patterns. In other words, a given output level can be expressed by multiple comparison patterns. Thus, even if comparator decision is wrong at some steps, the correct ADC output may be obtained. Then we can make reliable SAR ADC.

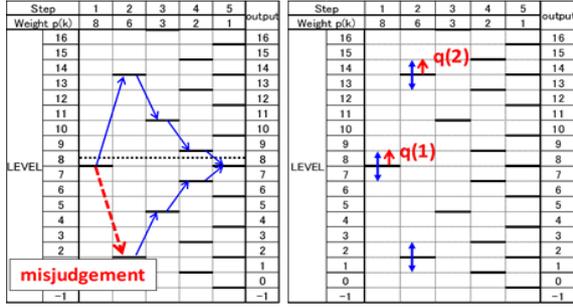


Fig. 3 Operation of a 4-bit 5-step SAR ADC in case of correct and incorrect judgments.

In addition, even if the number of the comparison steps is increased, the digital error correction enables high-speed AD conversion as a whole, because the digital error correction can take care of the DAC incomplete settling [1-6]; thus redundancy design has potential for reliable and/or high-speed SAR AD conversion.

### 2.3 Conventional Redundancy Design Issues

Reference voltage weight  $p(k)$  greatly affects redundant SAR ADC performance, and designers have selected  $p(k)$  by using Eq.(1). Here,  $M$  is the number of the whole steps and  $k$  is comparison step number.

$$p(k) = R^{M-k} \quad (1)$$

But conventional decision methods of reference voltage weights  $p(k)$  [1-5] have several issues as the following:

First, the reference voltage weight  $p(k)$  in Eq.(1) is not an integer which is not suitable for the circuit design. We must round  $p(k)$  values to use integer for easy design and accurate conversion. However rounding operation causes variability of the correction capability at each step and they may disturb performance improvement.

Second, there is difficulty of appropriate radix choice. ADC designers must choose a proper radix  $R$  ( $1 \leq R < 2$ ) in Eq.(1). Figure 3 shows an example in case of radix 1.80 and using rounding. However in Fig.4, two-way arrows indicate that correctable input range cannot cover all input range, which means that there are some ranges that cannot be corrected. There is a trade-off between correction capability and conversion speed, and the SAR ADC designer is forced to search a radix that is the most suitable for SAR ADC.

Third, there is an issue of internal DAC configuration. In the binary search SAR ADC, its internal DAC is realized easily by using binary network topology. But it is difficult to design the internal DAC of redundant SAR ADC. Conventional methods have realized internal DAC by complicated and large circuits.

We have shown the first and second issues are solved by Fibonacci sequence redundancy algorithm [6]. Further, this paper shows the Fibonacci sequence method also solve third issue.

## 3. Redundancy design using Fibonacci Sequence

### 3.1 Fibonacci Sequence

Fibonacci sequence is defined by a recurrence relation as shown in Eq.(2), where  $n$  in Eq.(2) is an integer greater than or equal to 0. Fibonacci sequence is presented in 1202 by Leonardo Fibonacci, who was a mathematician in Italy and it is known as one of the most famous number theories [7].

$$F_{n+2} = F_n + F_{n+1} \quad (2)$$

$$\text{where } F_0 = 0, F_1 = 1$$

Fibonacci numbers are expressed as the following by calculating Eq.(2).

$$0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, 233, 377, \dots$$

In short, the sum of neighboring two terms is next term. In addition, the closest terms ratio of Fibonacci sequence converges at about 1.62 as shown Eq.(3).

$$\lim_{n \rightarrow \infty} \frac{F_n}{F_{n-1}} = 1.6180339887 = \varphi \quad (3)$$

This ratio is called ‘‘Golden ratio’’ and it is widely recognized as the most beautiful ratio.

Fibonacci sequence and Golden ratio are based on very simple rules like the above. However we can find them in various places of our surroundings such as nature and humanity, and they have many interesting and unique properties. Thus they have been studied by many researchers for more than 800 years.

### 3.2 Fibonacci Sequence Redundancy design

We have studied redundancy algorithm using Fibonacci sequence to solve issues shown in Section 2.3. This algorithm selects Fibonacci sequence for reference voltage weights and realizes approximate radix 1.62 with only integer terms.

Then, we have shown several advantages as the following. Since Fibonacci sequence consists of integer terms, we don’t require rounding operation. And Figure 5 using Fibonacci sequence weighted SAR ADC shows that all input range is covered by correctable range showed two-way arrows. It means that high reliability is achieved unlike conventional methods in Fig. 3.

Furthermore, we also showed Fibonacci method’s advantage at speed as well as reliability. Figure 4 shows total settling time of internal DAC each algorithms at some resolutions. We can see that the Fibonacci method is the fastest method at all resolutions in Fig. 6.

Then we can indicate that the Fibonacci sequence method is better than conventional methods at reliability and speed. However, redundant SAR ADCs must use a complicated DAC instead of a binary DAC (such as a R-2R ladder DAC). We show in Section 4 that the Fibonacci sequence redundant SAR ADC can be realized by simple structure internal DAC.

Fig. 4 4-bit 5-step SAR ADC algorithm and definition of correctable difference  $q(k)$ .

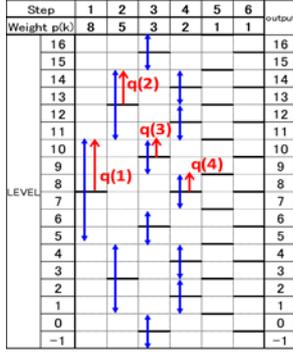


Fig.5. Redundant search algorithm of a 4-bit 6-step SAR ADC using Fibonacci sequence.

Settling time (fixed clock)

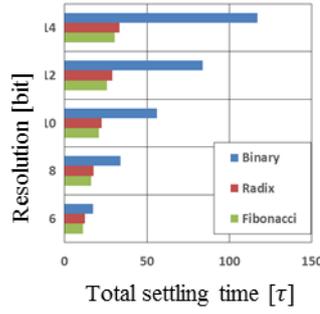


Fig.6. the comparison of the settling time of ADC at each resolution

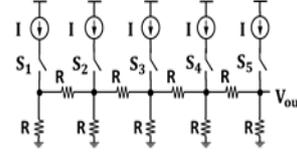


Fig.7. R-R ladder DAC with R termination.

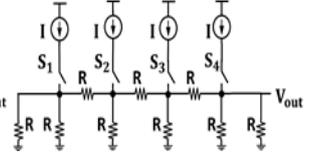


Fig.8. R-R ladder DAC with R||R termination.

#### 4. Fibonacci sequence weighted DAC

Posts Fibonacci numbers calculated in Eq. (2).

0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, 233, 377, 610, 987, ...

Odd term is as follows.

1, 2, 5, 13, 34, 89, 233, 610, ...

Even term is as follows.

1, 3, 8, 21, 55, 144, 377, 987, ...

##### 4.1 R-R ladder DAC circuit

###### A. R-R ladder DAC circuit with R termination

Figure 7 shows composition of the proposed Fibonacci weighted DAC circuit, and Figure 9 shows its operation example. Unlike R-2R ladder circuit of the binary weights, the proposed circuit changes resistance value of  $2R$  to  $R$ . In the top of the circuit of Fig.9, the current which is weighted to Fibonacci sequence flows through each resistor  $R$ . The current which is weighted to odd term of Fibonacci sequence flows from each node to GND. Therefore, voltage of each node is generated as a voltage which is weighted odd term of Fibonacci numbers. Here, think about the R-R ladder circuit with  $N$  ( $N=1,2,3,\dots$ ) point node. Then the current is divided on basis of the Fibonacci numbers  $F_n$  at each node. From this division, the node voltage of the  $m$ -th ( $V(m)$ ) from left side is given as Eq.7.

$$V(m) = \left( \frac{F_{2(N-m)+1}}{F_{2N}} \right) IR \quad (7)$$

In Fig.9, we show that it can obtain these voltages from most right node (output node) by shifting current source to each node of output side. If we adjust current values and resistance values, the denominator of Eq. (7) is possible to remove. As an example, the input current source value is set as the 55I in Fig.9. Using principle of superposition, the circuit in Fig.6 can realize a DAC weighted to odd term of Fibonacci sequence.

###### B. R-R ladder DAC circuit with R||R termination

Figure 8 shows our proposed circuit, and Figure 10 shows its operation example. Unlike the circuit in Fig.7,

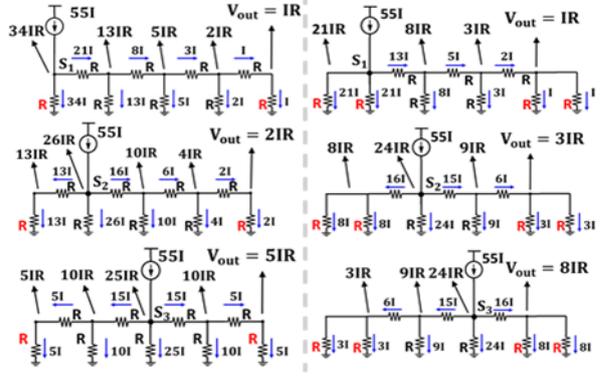


Fig.9. Operation examples of R-R ladder DAC with R termination.

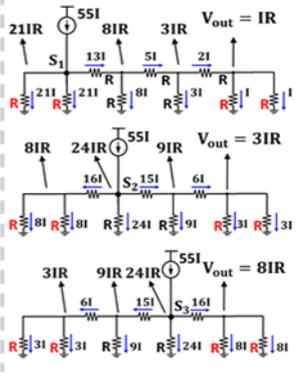


Fig.10. Operation examples of R-R ladder DAC with R||R termination.

termination of circuit is not  $R$  but  $R||R$ . In the same definition as above, we calculate  $m$ -th ( $V(m)$ ), and obtain Eq.(8).

$$V(m) = \left( \frac{F_{2(N-m+1)}}{F_{2(N+1)}} \right) IR \quad (8)$$

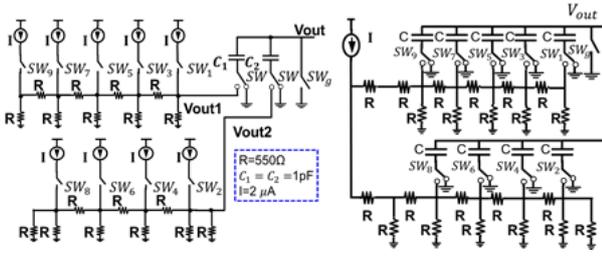
Eq. (8) shows that this circuit can generate voltage on based of even term of Fibonacci sequence.

Thus, it can express all terms of Fibonacci sequence by combination of circuits of Fig.7 and Fig.8.

###### C. R-R resistor DAC weighted to Fibonacci numbers

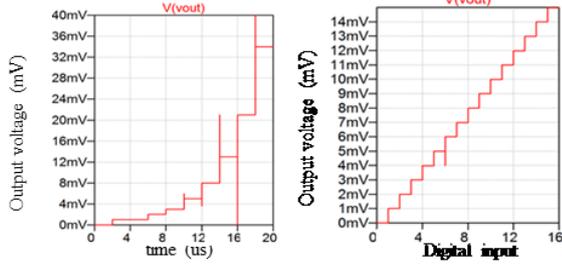
Figure 11 shows two examples (type (a) and type (b)) of combined circuits in Fig.7 and Fig.8. There odd terms generate in R termination circuit (upper stage), even terms generate in  $R||R$  termination circuit (lower stage). Then their outputs are added by using capacity array. They can obtain voltages weighted to all Fibonacci numbers.

Fig.12 shows SPICE simulation results which check the operation of the proposed DACs in Fig.11-(a). Element values of each circuit set resistor, capacitor and current source to  $550\Omega$ ,  $1pF$  and  $2\mu A$ . When put any one of switches (SW1~9), Fig.12-(a) shows output voltage ratios become Fibonacci numbers (0,1,1,2,3,5,8,13,...). Its result means that each current source can generate the voltage weighted to Fibonacci number. Thus, circuit of Fig.11-(a) can generate voltages weighted Fibonacci numbers. In addition, according to digital inputs, Fig.12-(b) show that it generate analog values. These results prove that it can use as DAC weighted Fibonacci numbers.



(a) R-R ladder of current addition type. (b) R-R ladder of single current division type.

Fig. 11. Proposed Fibonacci weighted DACs.



(a) Confirmation of output voltage with Fibonacci weights. (b) Confirmation of linear output voltage.

Fig. 12. Simulated output waveform of DACs in circuit of Fig. 11-(a).

Circuit of Fig. 11-(b) also generates the same waveform, and further can be realized by single current source. However, compared to it, that of Fig. 11-(b) can generate voltage full-scale of approximately 1/10. These circuits can use as DAC weighted Fibonacci numbers.

#### 4.2 C-C Capacitor Network

These circuit constitutions in Fig. 13 and Fig. 14 are similar to R-R ladder circuits; there are C and C||C terminations. Different points are as follows: change of resistor R to capacitor C, and change of current source to voltage source. Outputs of these circuits also obtain voltages weighted to Fibonacci numbers. We confirmed that DAC can be realized by addition of capacity array by simulation. In addition, since they don't flow DC current, low power consumption may be realized. However due to the influence of parasitic capacitances, it may be difficult to realize a high-precision DAC.

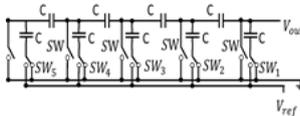


Fig. 13 C-C capacitor ladder DAC circuit with C termination.

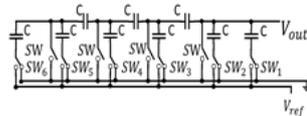


Fig. 14 C-C capacitor ladder DAC circuit with C||C termination.

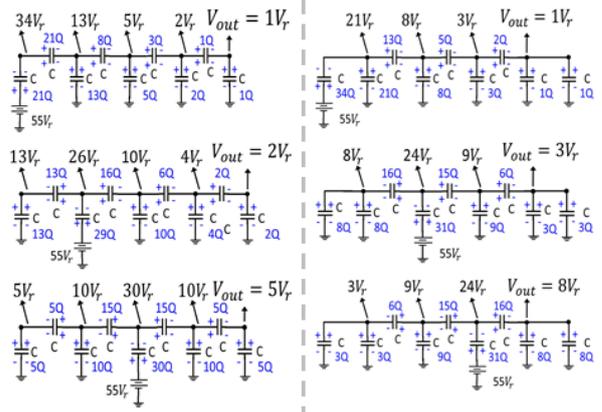


Fig. 15. Operation principle of C-C ladder with C termination. Fig. 16. Operation principle of C-C ladder with C||C termination.

#### 5. Summary

In this paper, we have described redundancy SAR ADC algorithm design methods with applying properties of Fibonacci sequence such as the closest terms ratio called golden ratio and realization of all terms with integer. Especially we have shown that several DAC topologies for its internal use can be realized simple structure.

#### Acknowledgments

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