ICSICT-2016
2016 IEEE 13th International Conference on Solid-State and Integrated Circuit Technology
Oct. 25- Oct.28, 2016
White Horse Lake Jianguo Hotel, Hangzhou, China

S23-1　Analog Circuits III
10:15-10:45 AM
Oct. 28, 2016 (Fri)

Analog / Mixed-Signal Circuit Design Based on Mathematics

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Our Statement

Beautiful mathematics

⇨ good analog/mixed-signal circuit

Besides transistor level design

- Control theory
- Number theory
- Statistics
- Coding theory
- Modulation
- Signal processing algorithm

⇩

Enhance analog/mixed-signal circuit performance

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Control Theory and Operational Amplifier Design

Our proposal

For

Analysis and design of operational amplifier stability

Use

Routh-Hurwitz stability criterion

- Popular in control theory
- Not in circuit design

We can obtain

Explicit stability condition for circuit parameters

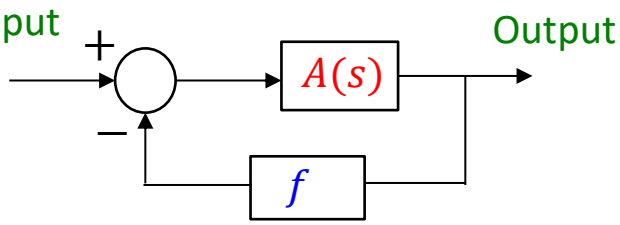
(which can NOT be obtained only with Bode plot).

[1] J. Wang, H. Kobayashi, et. al., "Analysis and Design of Operational Amplifier Stability Based on Routh-Hurwitz Method", IEEE ICSICT (Oct. 2016).

Routh-Hurwitz Stability Criteria

- Transfer function of closed-loop system

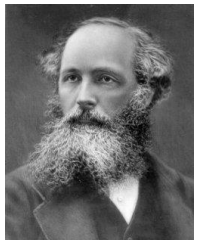
$$G(s) = \frac{A(s)}{1 + fA(s)} = \frac{N(s)}{D(s)}$$



- Suppose

$$N(s) = b_m s^m + b_{m-1} s^{m-1} + \cdots + b_1 s + b_0$$

$$D(s) = a_n s^n + a_{n-1} s^{n-1} + \cdots + a_1 s + a_0$$



J. Maxwell

A. Stodola

- System is stable if and only if

real parts of all the roots s_p of the following are negative:

Maxwell and Stodola found out !!

Characteristic equation $D(s) = a_n s^n + a_{n-1} s^{n-1} + \cdots + a_1 s + a_0 = 0$

- To satisfy this, what are the conditions for $a_n, a_{n-1}, \cdots a_1, a_0$?

Routh and Hurwitz solved this problem independently !!

Amplifier Circuit and Small Signal Model

Open-loop transfer function from small signal model

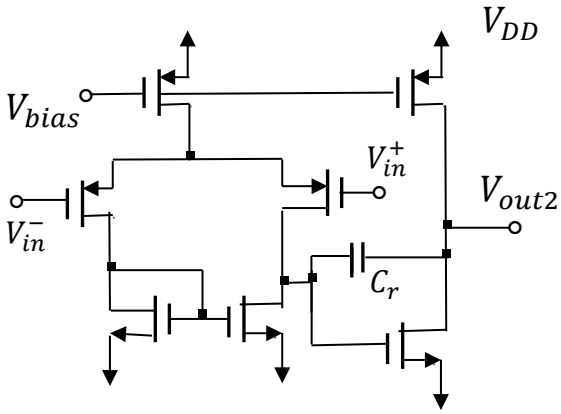
$$A(s) = \frac{v_{out}(s)}{v_{in}(s)} = A_0 \frac{1 + b_1 s}{1 + a_1 s + a_2 s^2}$$

$$b_1 = -\frac{C_r}{G_{m2}}$$

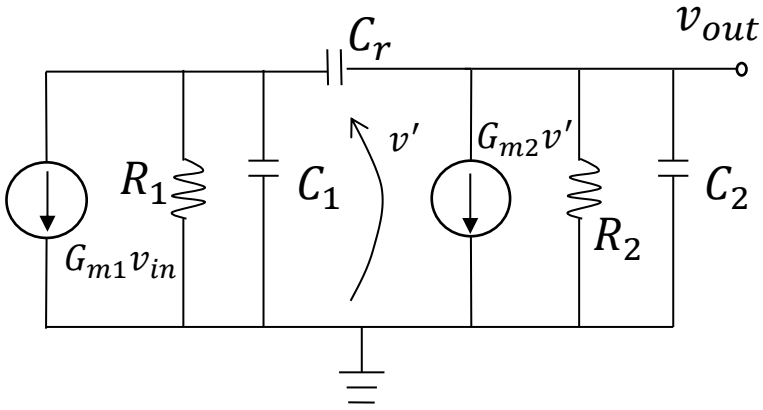
$$A_0 = G_{m1} G_{m2} R_1 R_2$$

$$a_2 = R_1 R_2 C_2 \left[C_1 + \left(1 + \frac{C_1}{C_2} \right) C_r \right]$$

$$a_1 = R_1 C_1 + R_2 C_2 + (R_1 + R_2 + R_1 G_{m2} R_2) C_r$$



Amplifier circuit

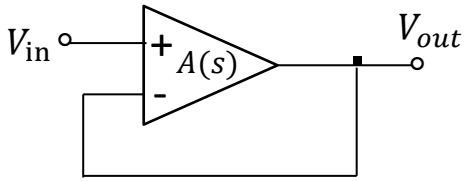


Small signal model

Explicit Condition for Feedback Stability

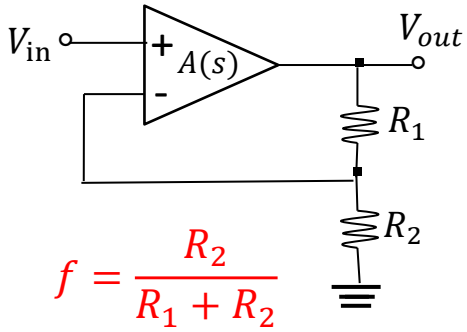
Closed-loop transfer function:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{A(s)}{1+fA(s)} = \frac{A_0(1+b_1 s)}{1+fA_0+(a_1+fA_0b_1)s+a_2s^2}$$



$$f = 1$$

Necessary and sufficient stability condition based on R-H criterion



$$f = \frac{R_2}{R_1+R_2}$$

$$a_1 + fA_0b_1 > 0$$

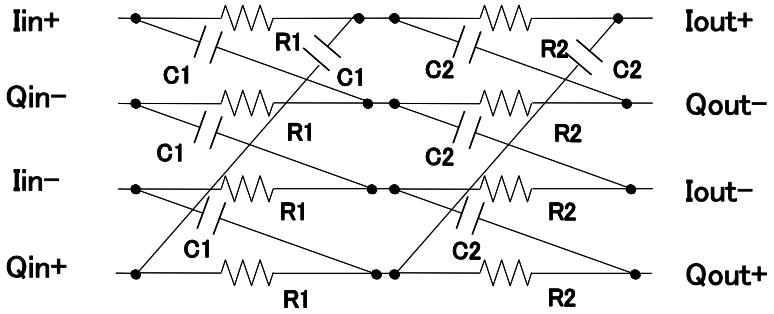
$$R_1C_1 + R_2C_2 + (R_1+R_2)C_r + (G_{m2} - fG_{m1})R_1R_2C_r > 0$$

Explicit stability condition for parameters

Contents

RC Polyphase Filter

- Its input and output are complex signals.
- Passive RC analog filter
- One of key components in wireless transceiver analog front-end
  - I, Q signal generation
  - Image rejection



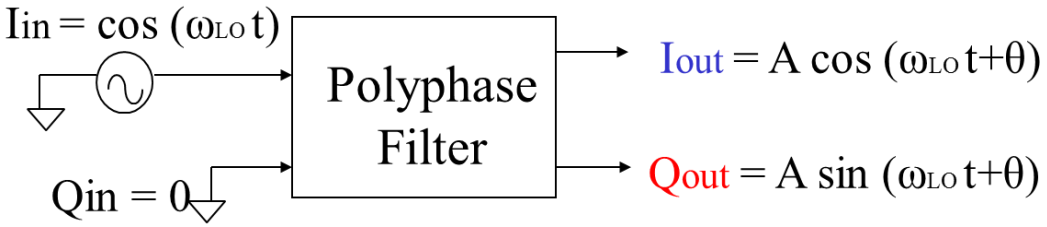
Differential Complex Input: $Vin = Iin + j\,Qin$

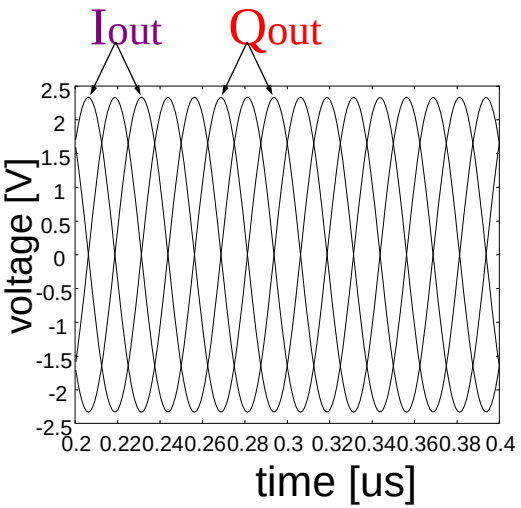
Differential Complex Output: $Vout = Iout + j\,Qout$

[1] Y. Niki, S. Sasaki, H. Kobayashi, "Flat Passband Gain Design Algorithm for 2nd-order RC Polyphase Filter," IEEE ASICON (Nov. 2015).

Roles of RC Polyphase Filter

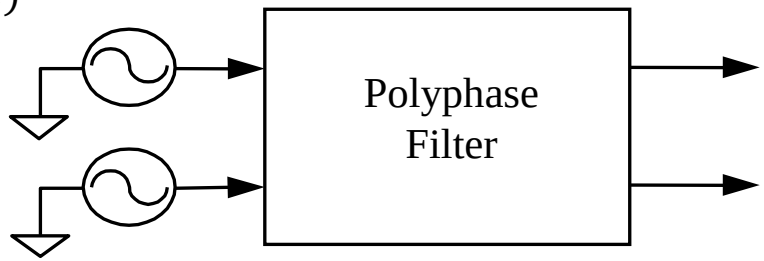
- Sine, cosine signal generation





- Image rejection

$I_{in} = (A + B)\cos(\omega t)$



$I_{out} = A\cos(\omega t)$

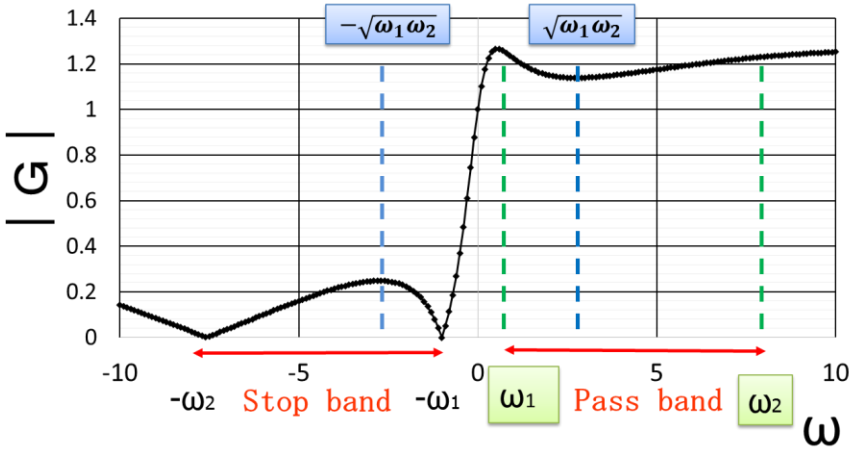
$Q_{out} = A\sin(\omega t)$

$Q_{in} = (A - B)\sin(\omega t)$

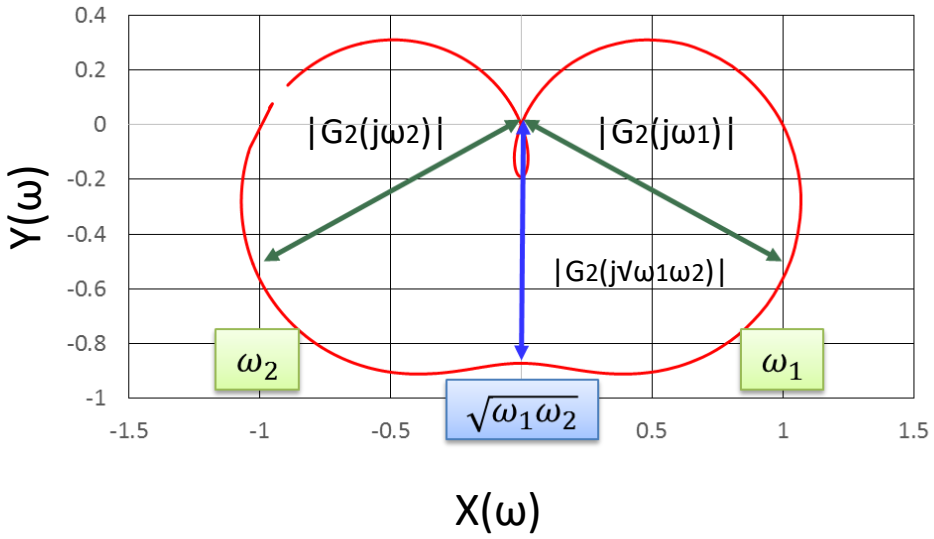
$Ae^{j\omega t} + Be^{-j\omega t}$ → $Ae^{j\omega t}$

Nyquist Chart of Complex Transfer Function *G2*

Gain characteristics $|G_2(j\omega)|$



Nyquist chart of $G_2(j\omega)=X(\omega)+j\,Y(\omega)$

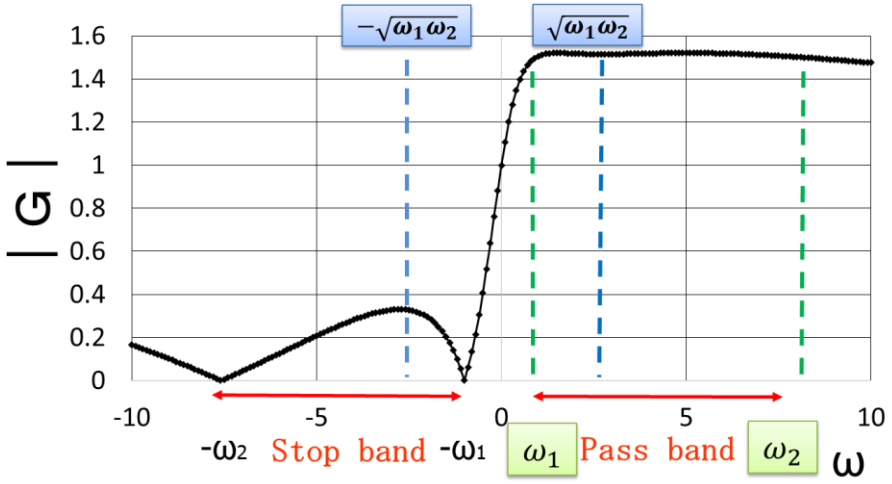


$$|G_2(j\omega_1)|=|G_2(j\omega_2)|$$

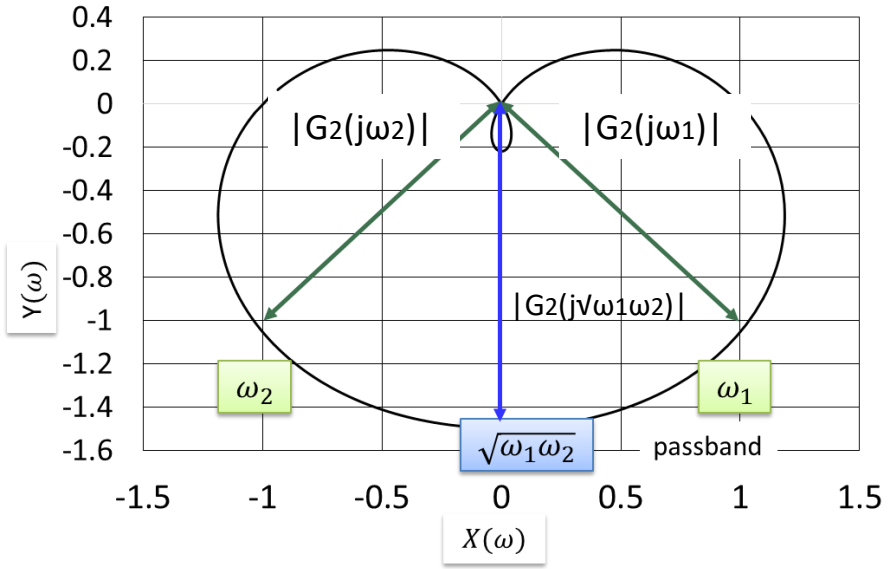
But in general $|G_2(j\omega_1)|=|G_2(j\omega_2)| \neq |G_2(j\sqrt{\omega_1\omega_2})|$

Our Idea for Flat Passband Gain Algorithm

Gain characteristics $|G_2(j\omega)|$



Nyquist chart of $G_2(j\omega)=X(\omega)+j\,Y(\omega)$



If we make $|G_2(j\omega_1)| = |G_2(j\omega_2)| = |G_2(j\sqrt{\omega_1\omega_2})|$,
gain would be flat from ω1 to ω2.

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ADC: Analog-to-Digital Converter

DAC: Digital-to-Analog Converter

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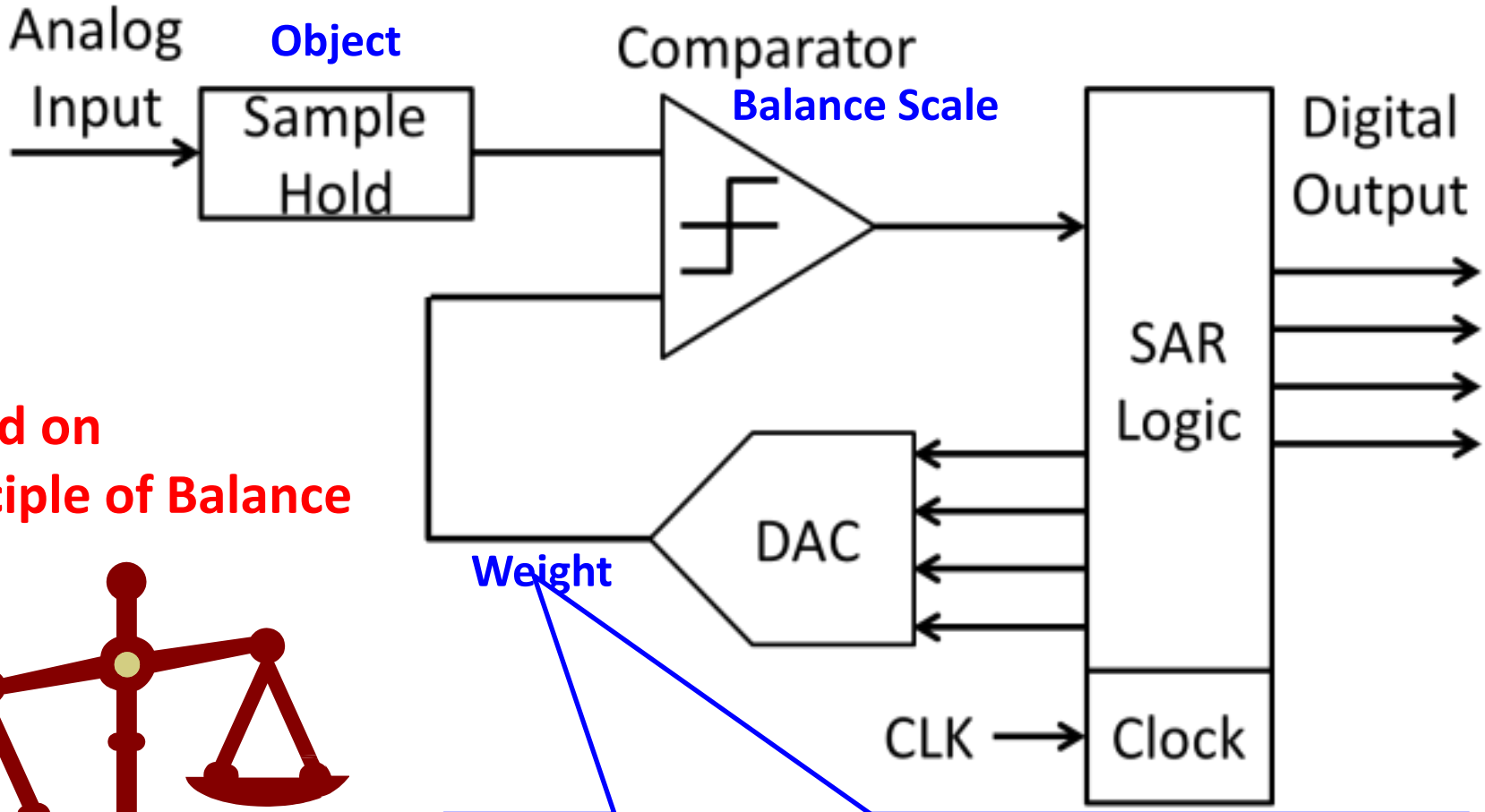
DAC: Digital-to-Analog Converter

SAR ADC Configuration



Based on Principle of Balance

Generally use binary weights
(1 , 2 , 4 , 8 , 16 , 32, 64 …)

Binary Search SAR ADC Operation

5bit-5step SAR ADC

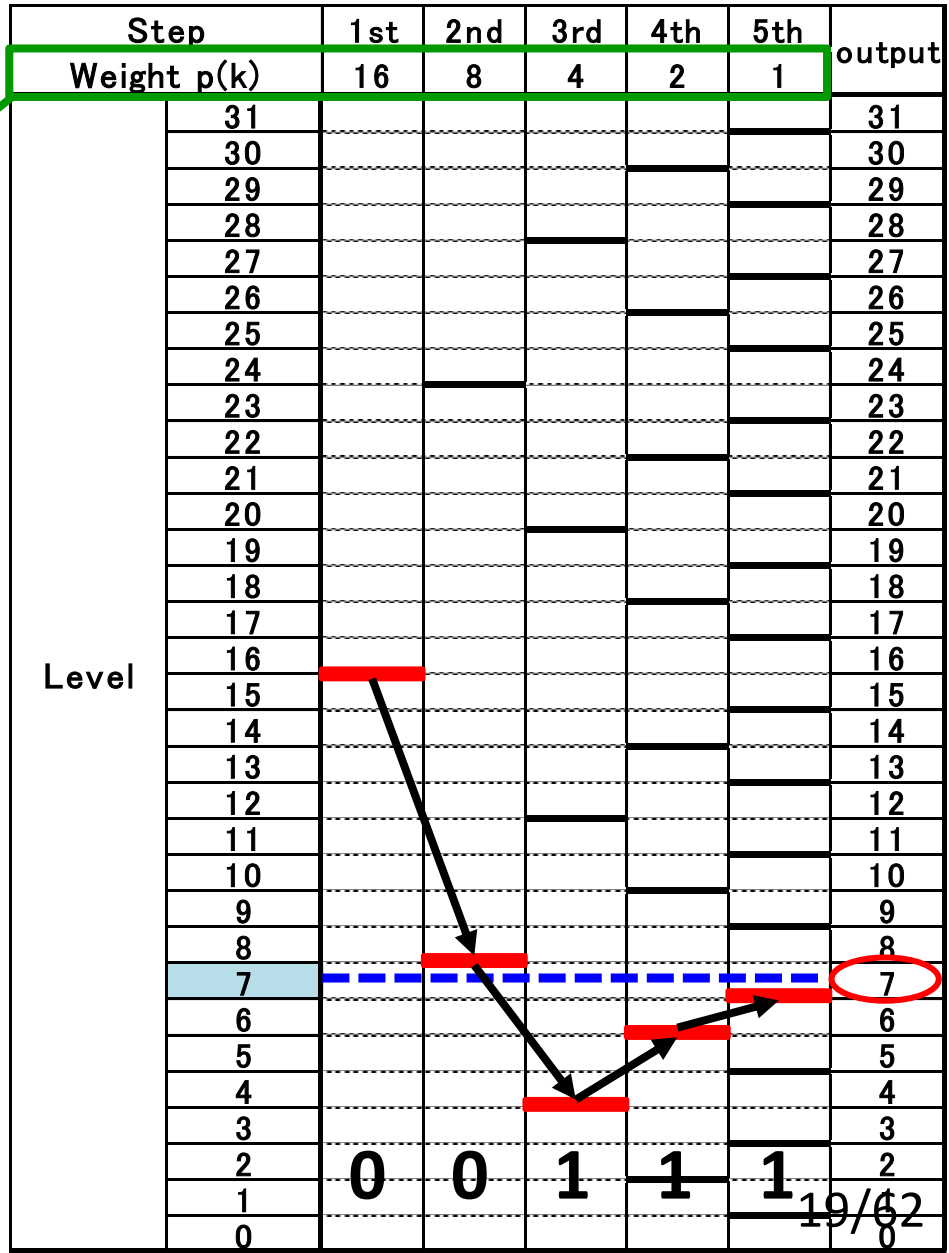
- Binary weight

  p(k) = 16, 8, 4, 2, 1
- Analog input 7.3

One-to-one mapping
between decimal and binary codes

$$D_{out} = (00111)_2$$

$$7 = 16 - 8 - 4 + 2 + 1 + 0.5 - 0.5$$



Redundant Search SAR ADC Operation

5bit-6step SAR ADC

- **Redundant weight**

  p(k) = 16, 10, 6, 3, 2, 1

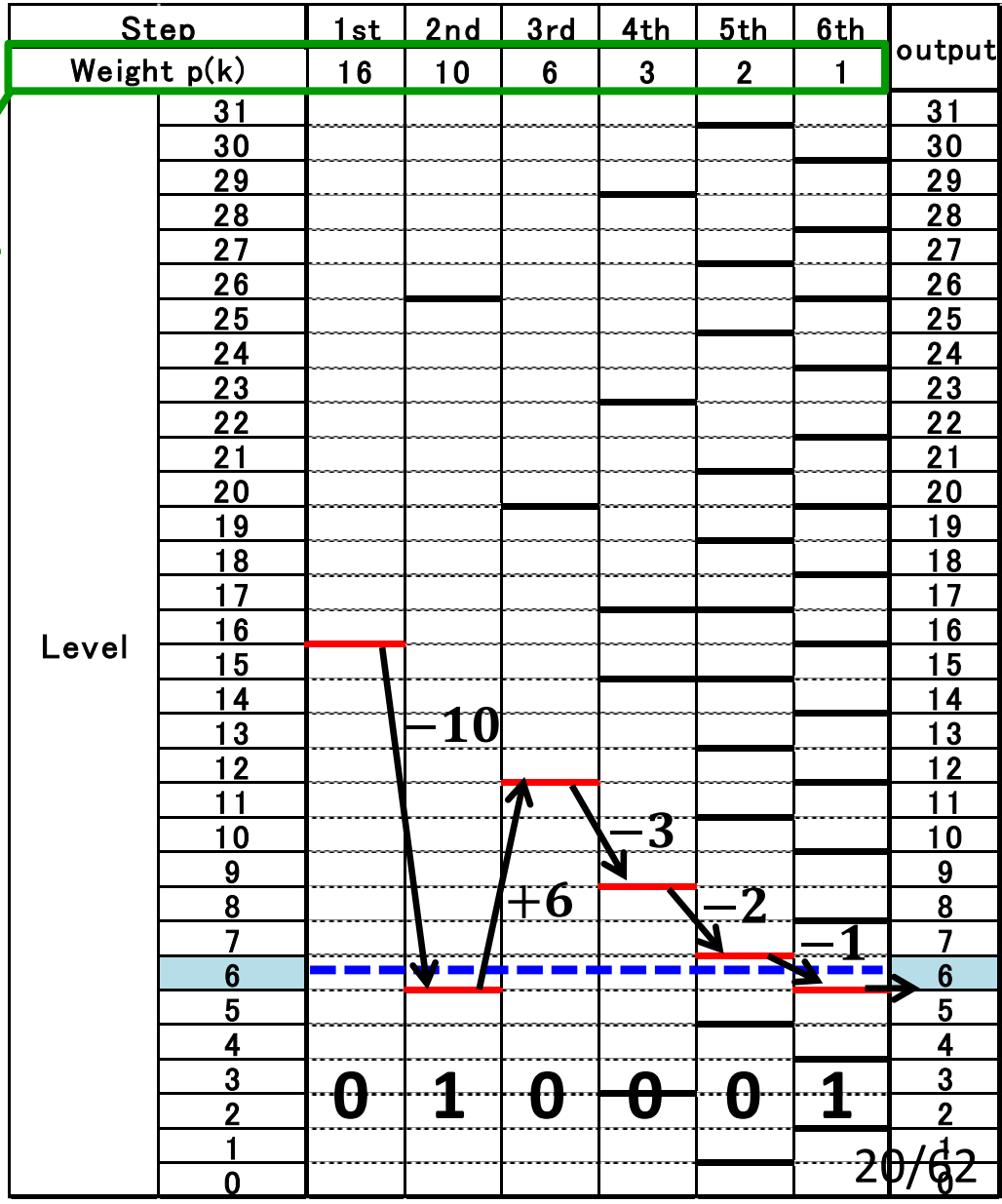
- **Analog input 6.3**

Increase number of

comparison steps

6⇒010001⇒6

16−10+6−3−2−1+0.5-0.5 = 6



Fibonacci Sequence

Definition (n=0,1,2,3…)

$$F_0 = 0$$
$$F_1 = 1$$
$$F_{n+2} = F_n + F_{n+1}$$

Example of numbers(Fibonacci number)

0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89…

Leonardo Fibonacci (around 1170-1250)

Property

The closest terms ratio converges to *"Golden Ratio"* !

$$\lim_{n\to\infty} \frac{F_n}{F_{n-1}} = 1.618033988749895 = \varphi$$

Fibonacci Weights

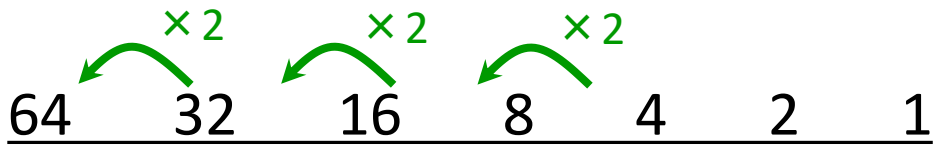
We select N bit and M step SAR ADC k-th step reference voltage p(k).

here $p(1) = 2^{N-1}$

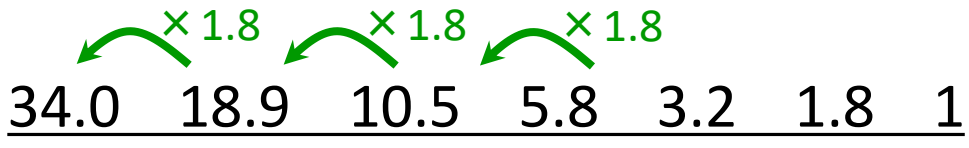
Proposed solution

Using Fibonacci sequence for p(k):$p(k) = F_{M-k+1}$

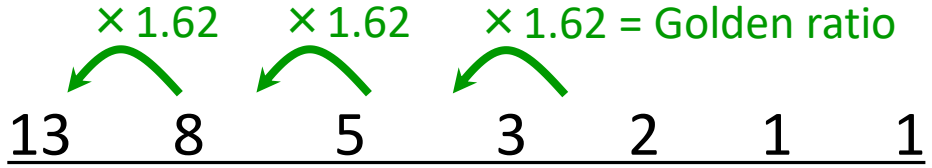
Binary Weight



Radix 1.8 Weight



Fibonacci Weight
(Radix 1.62 Weight)

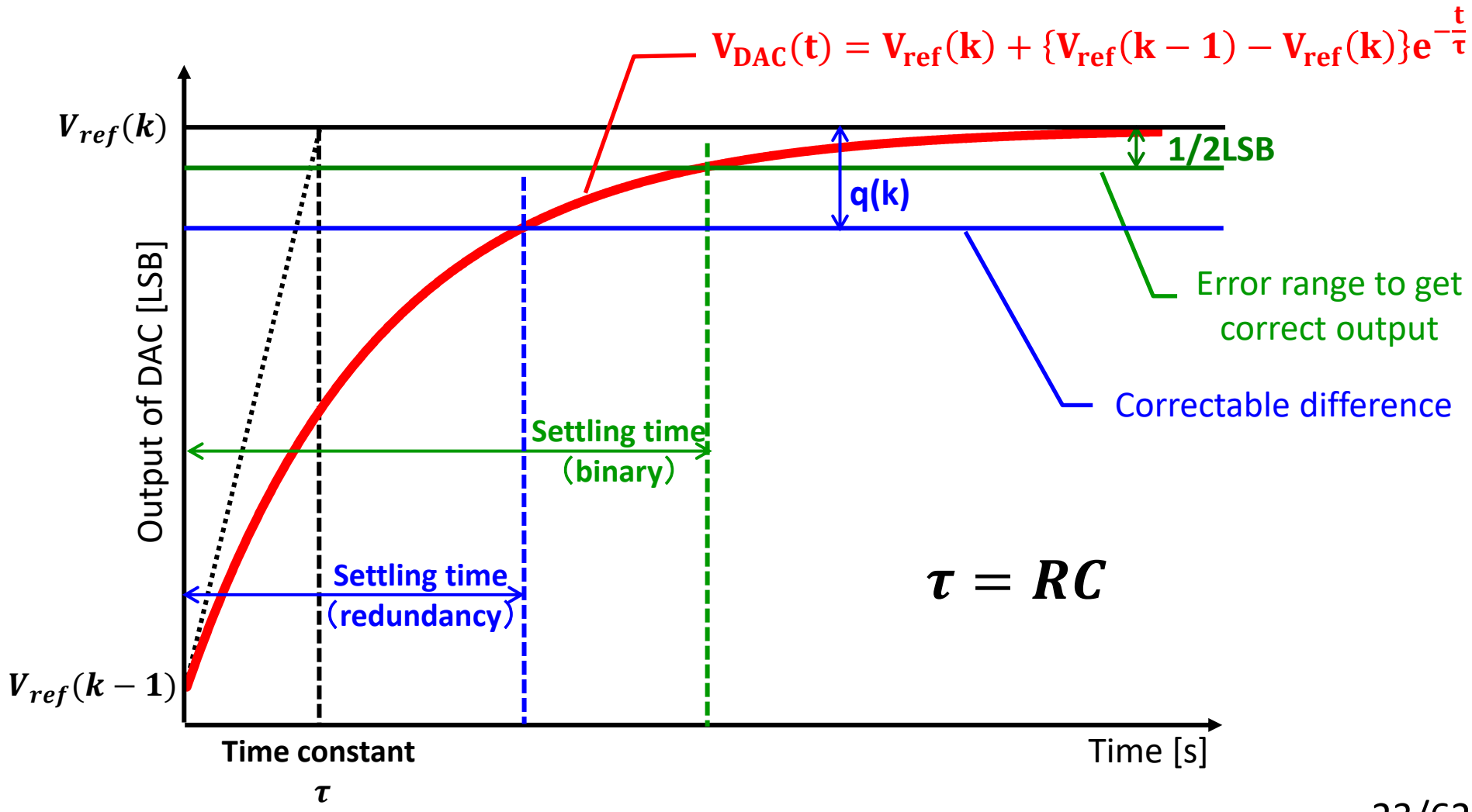


Property converging to Golden Ratio

Realize **Radix 1.62 Weight** by using **only integer** !

Internal DAC Settling Time

DAC Settling model by a simple first-order RC circuit

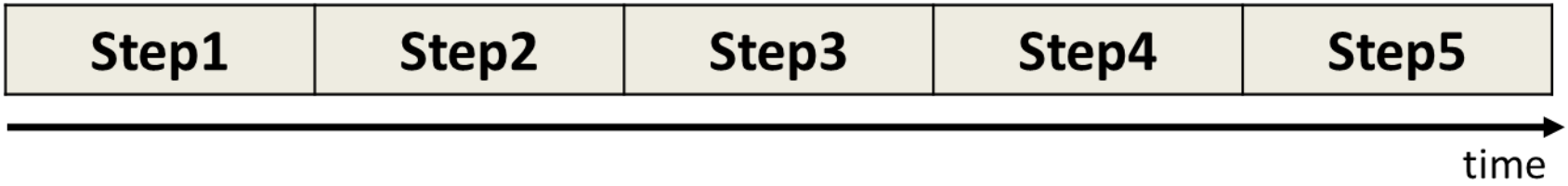


SAR ADC Speed and DAC Settling

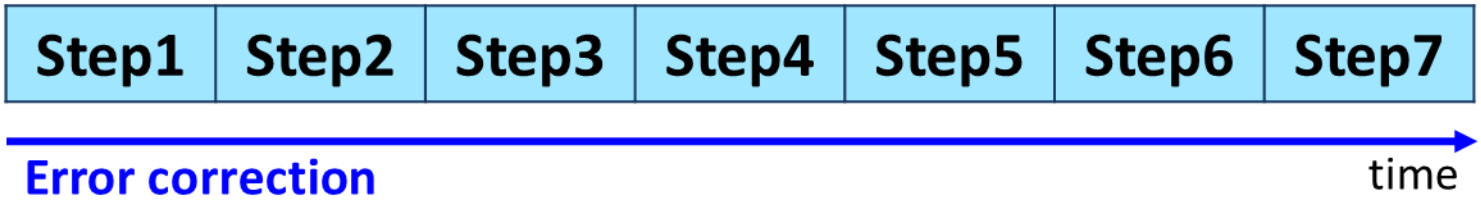
Redundancy → **Incomplete settling**

5bit SAR ADC

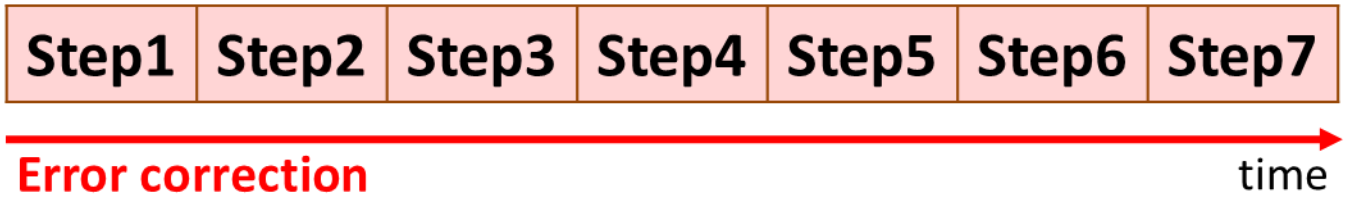
Binary search (complete settling)



Redundant search (incomplete settling)



Fibonacci search (incomplete settling)



The shortest AD conversion time !!

Fibonacci Weights SAR ADC

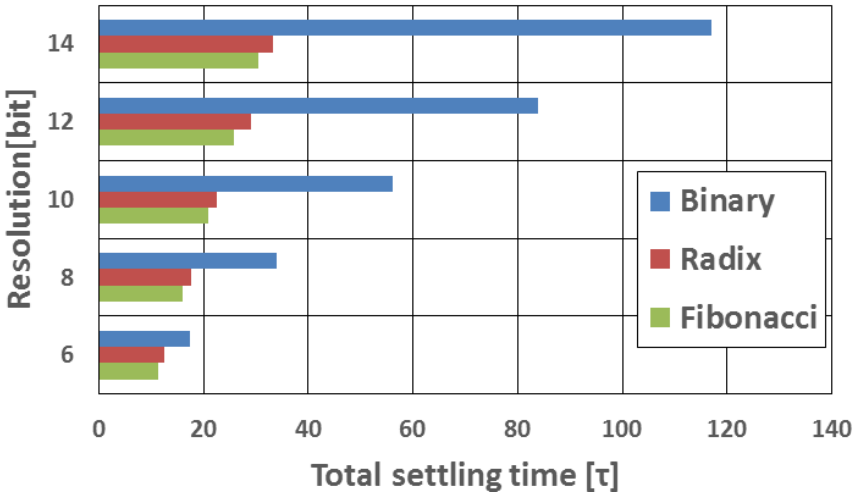
We have found the following:

- Reliable

  Comparator decision errors can be recovered with redundancy.

- Fastest SAR AD Conversion

  In case the internal DAC incomplete settling is considered.



[1] Y. Kobayashi, H. Kobayashi, et. al.,
"SAR ADC Design Using Golden Ratio Weight Algorithm", ISCIT (Oct. 2015).
[2] T. Arafune, Y. Kobayashi, H. Kobayashi , et. al., "Fibonacci Sequence Weighted SAR ADC Algorithm and its DAC Topology," IEEE ASICON (Nov. 2015).

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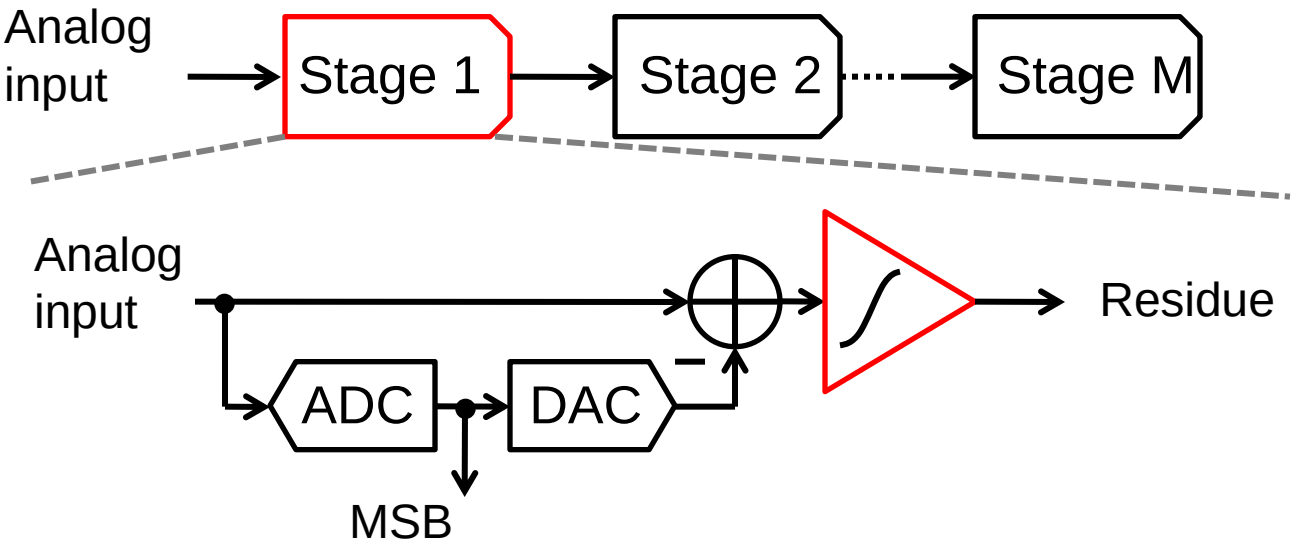
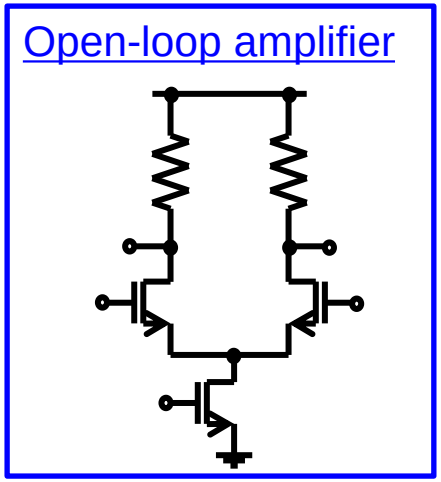
ADC: Analog-to-Digital Converter

DAC: Digital-to-Analog Converter

Power Consumption of Pipelined ADC

•First stage amplifier：Consumes considerable power

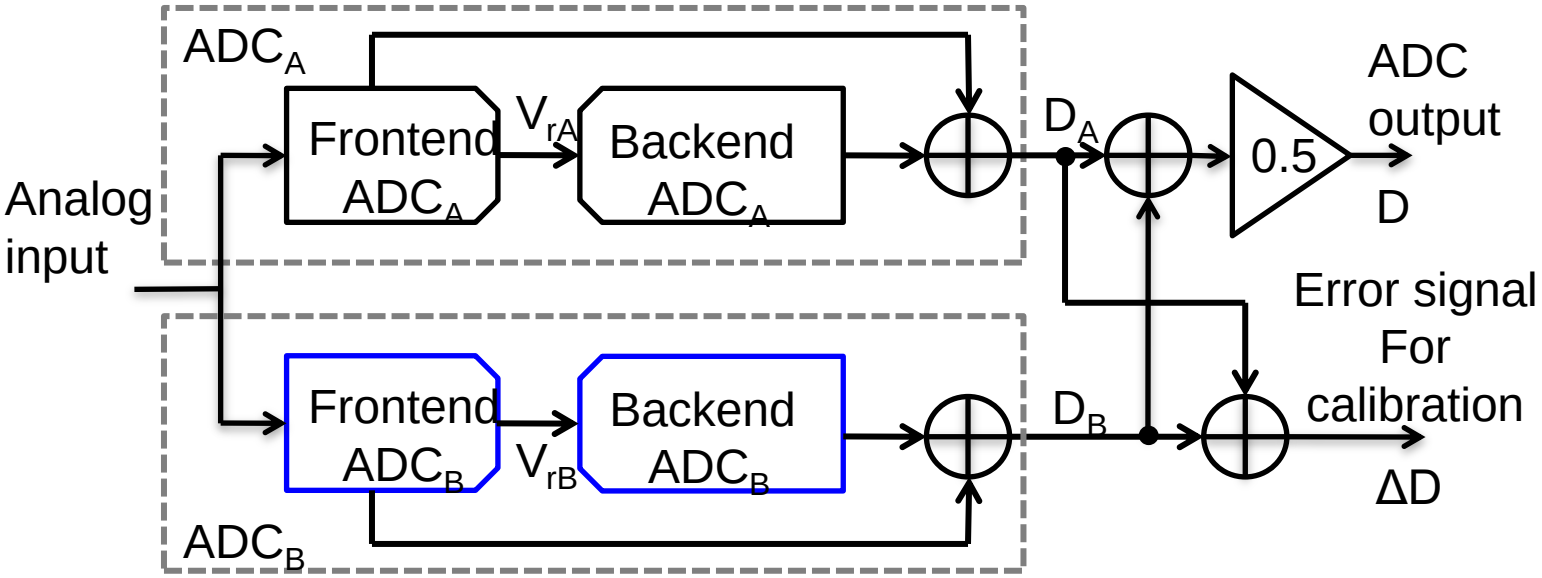




- First stage amplifier：Open-loop
- Low power consumption

•Nonlinearity of open-loop amplifier : background self-calibration

Split ADC Structure

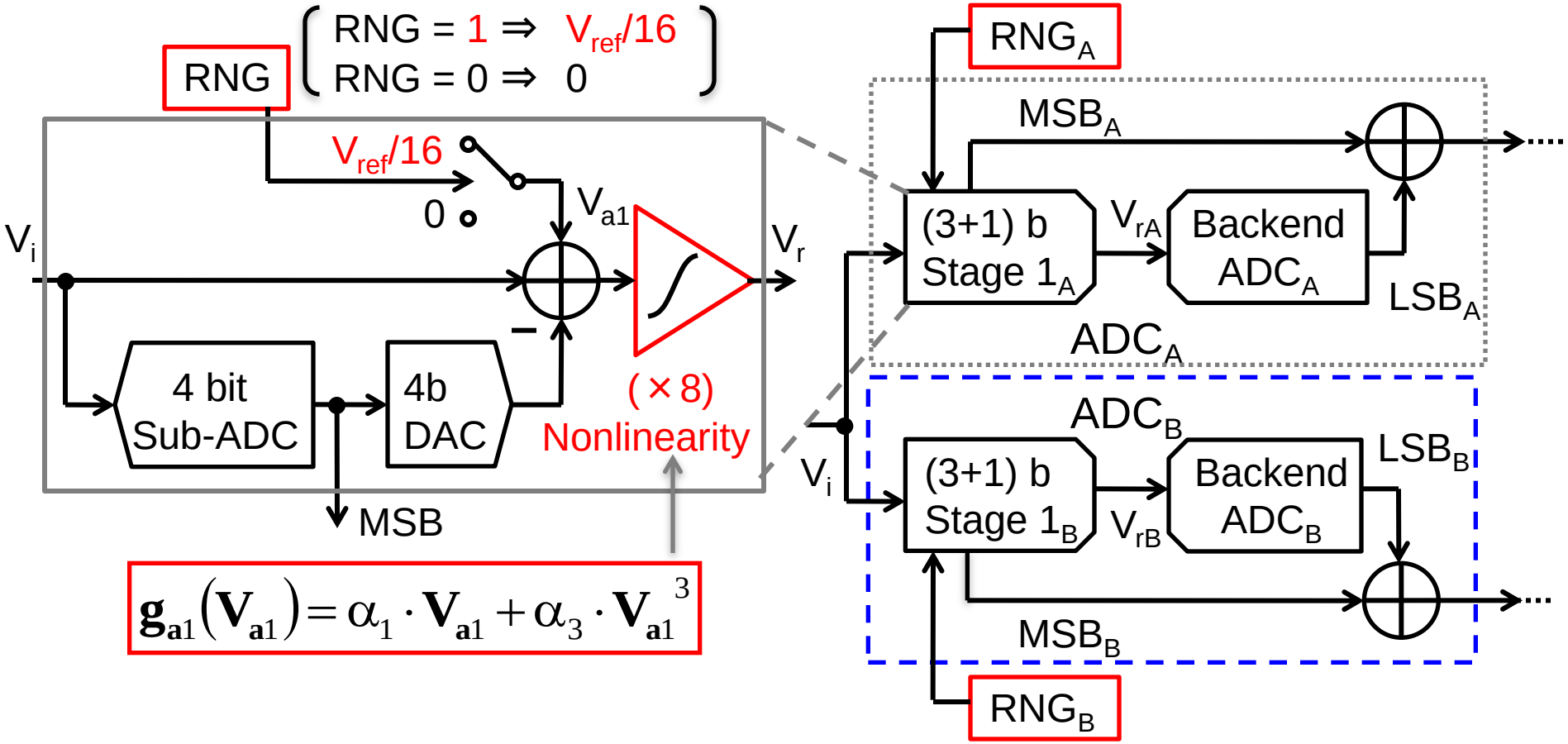


- Each channel ADC: half gm, half capacitor
  different residue logic ➡ converge quickly
- Power consumption : small overhead
- Chip area : small overhead

[1] T. Yagi, H. Kobayashi, "Background Calibration Algorithm for Pipelined ADC with Open-Loop Residue Amplifier Using Split ADC Structure," IEEE APCCAS, (Dec. 2010).

[2] Haijun Lin, "Split-Based 200Msps and 12 bit ADC Design", IEEE ASICON (Nov. 2015).

Complicated Adaptive Signal Processing for Calibration



- Adding pseudo randomly
  → Generate two residue waveforms
- RNG(A & B) : Set default value to different

RNG:Random Numbar Generator

Validate the Effectiveness with MATLAB

ADC_A ($Stage1_A$)

- C mismatch： 2% (σ)
- Nonlinearity of amplifier：

$$\mathbf{g_{a1}}(\mathbf{V_{a1}}) = 7.5 \cdot \mathbf{V_{a1}} + (-15) \cdot \mathbf{V_{a1}}^3$$

- Nonlinearity correction
  - ✓ LMS loop：
    μ_A= 1/8192
  - ✓ IIR filter gain：
    μ_{3a} = 1/512
- Gain error, C mismatch correction
  - ✓ IIR filter gain：
    μ_{1a} = 1/1024

ADC_B ($Stage1_B$)

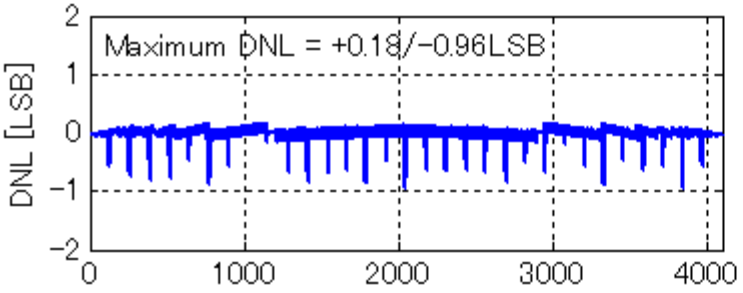
- C mismatch： 2% (σ)
- Nonlinearity of amplifier：

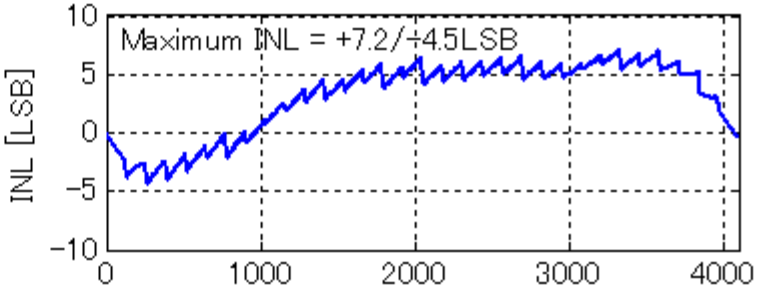
$$\mathbf{g_{b1}}(\mathbf{V_{b1}}) = 7.6 \cdot \mathbf{V_{b1}} + (-15.2) \cdot \mathbf{V_{b1}}^3$$

- Nonlinearity correction
  - ✓ LMS loop：
    μ_B= 1/8192
  - ✓ IIR filter gain：
    μ_{3b} = 1/512
- Gain error, C mismatch correction
  - ✓ IIR filter gain：
    μ_{1b} = 1/1024

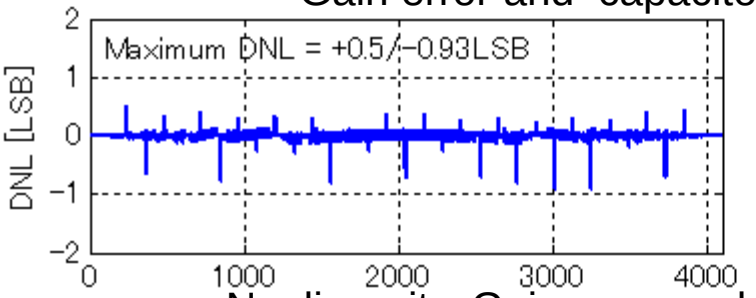
DNL and INL of the ADC output

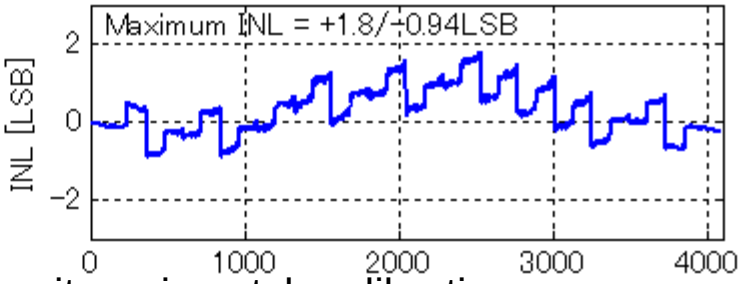
No calibration



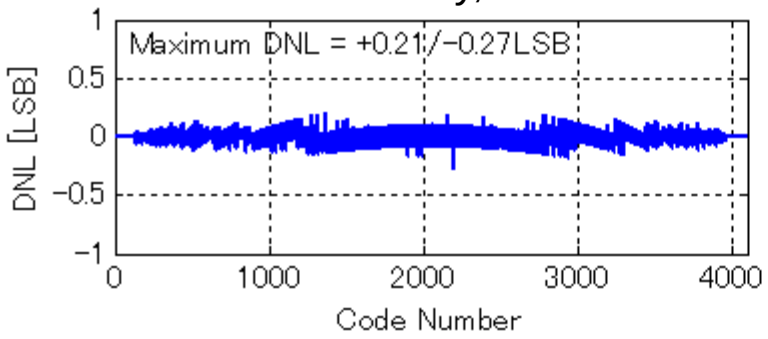


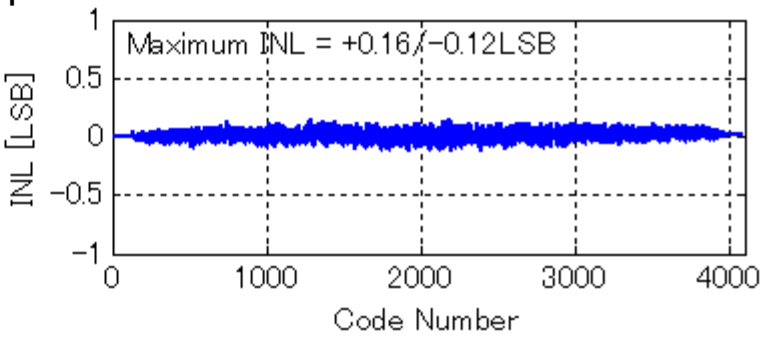
Gain error and capacitor mismatch calibration





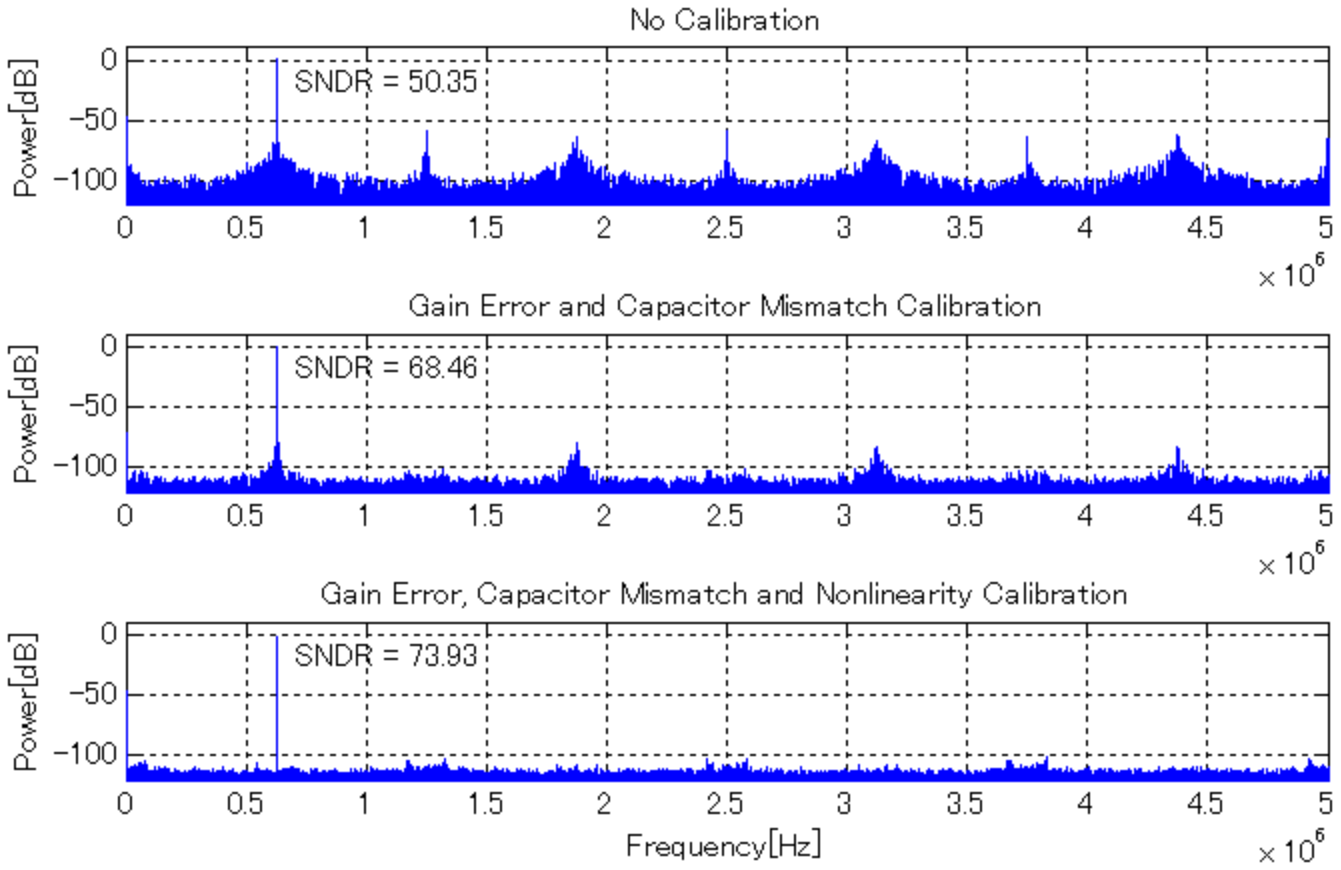
Nonlinearity, Gain error and capacitor mismatch calibration





•Calibrate all error : DNL, INL are within ±0.5LSB

Output Power Spectrum



- Calibrate all error : SNDR=73.9dB

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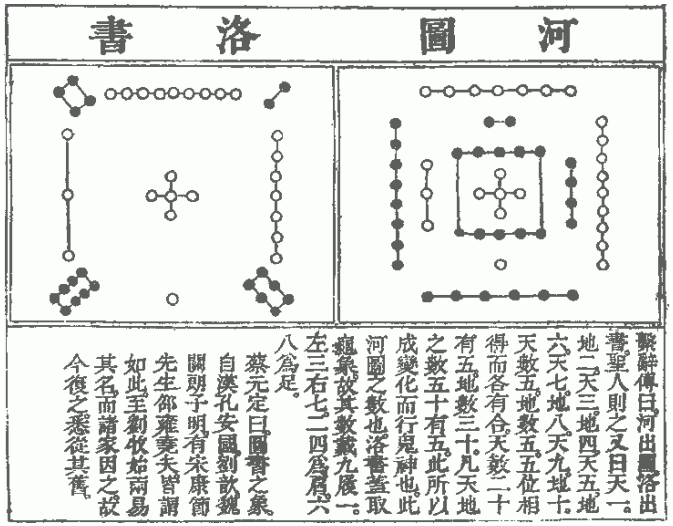
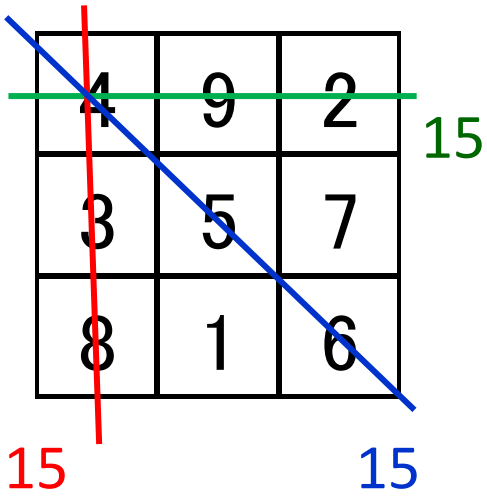
What is Magic Square (魔方陣)？

- Classical mathematics
- Origin from Chinese academia
- “Constant sum” characteristics
- Varieties of magic squares

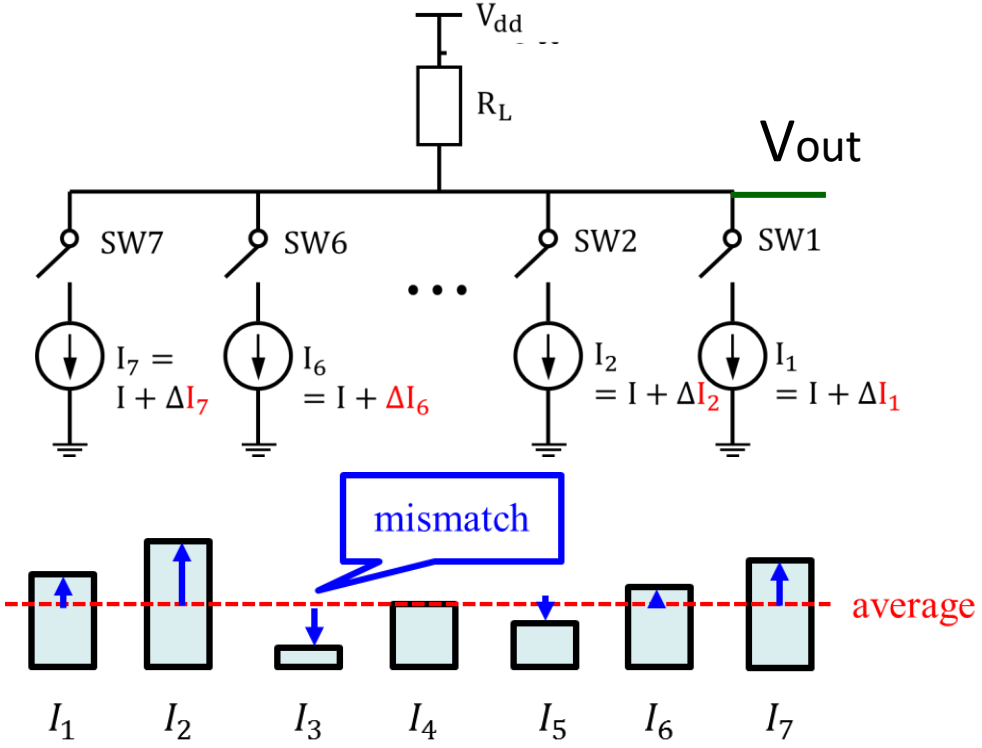


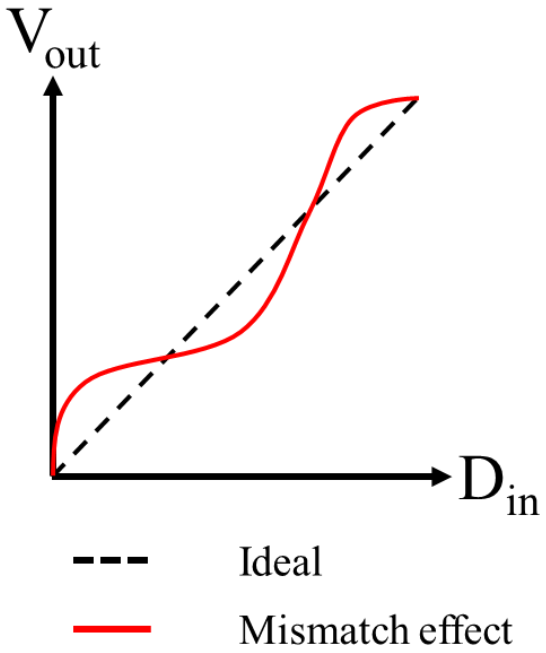
3x3 魔方陣



59	5	4	62	63	1	8	58
9	18	17	49	50	42	19	56
55	20	28	33	29	40	45	10
54	44	38	31	35	26	21	11
12	43	39	30	34	27	22	53
13	24	25	36	32	37	41	52
51	46	48	16	15	23	47	14
7	60	61	3	2	64	57	6

Unary DAC and Mismatch Problem



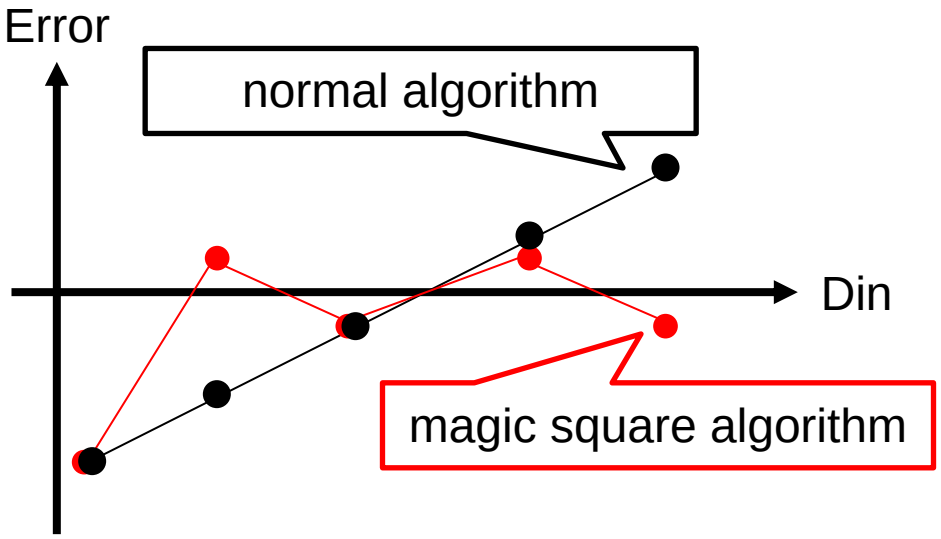


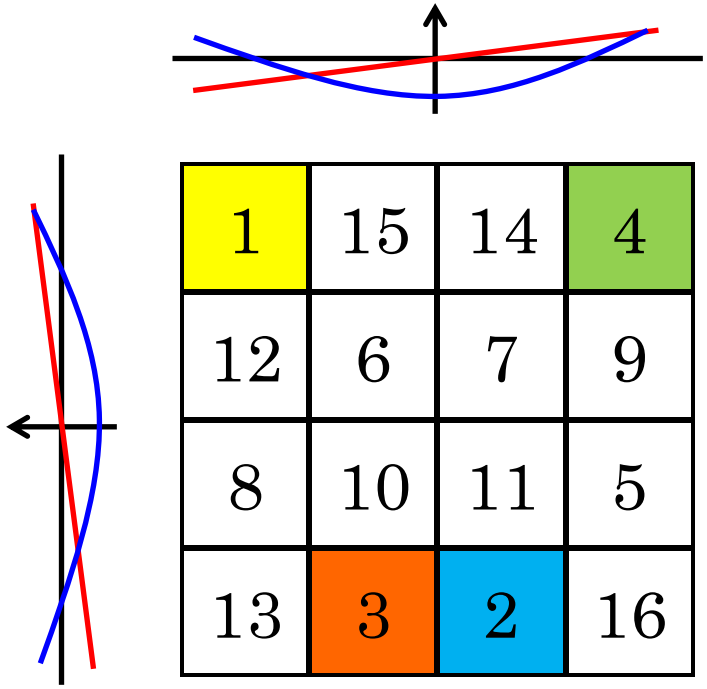
In practice, current sources have mismatches.

➡ DAC becomes non-linear.

Possibility of Using Magic Square (魔方陣)

- Semiconductor devices have random and systematic mismatches
- Changing the switching order with magic square
  - ➡ Cancellation of mismatch effects





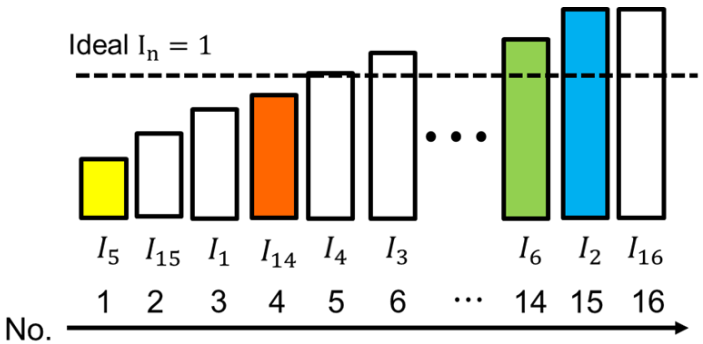
1	15	14	4
12	6	7	9
8	10	11	5
13	3	2	16

[1] M. Higashino, H. Kobayashi, “DAC Linearity Improvement Algorithm With Unit Cell Sorting Based on Magic Square”, IEEE VLSI-DAT (April 2016).

Inspired New Algorithm

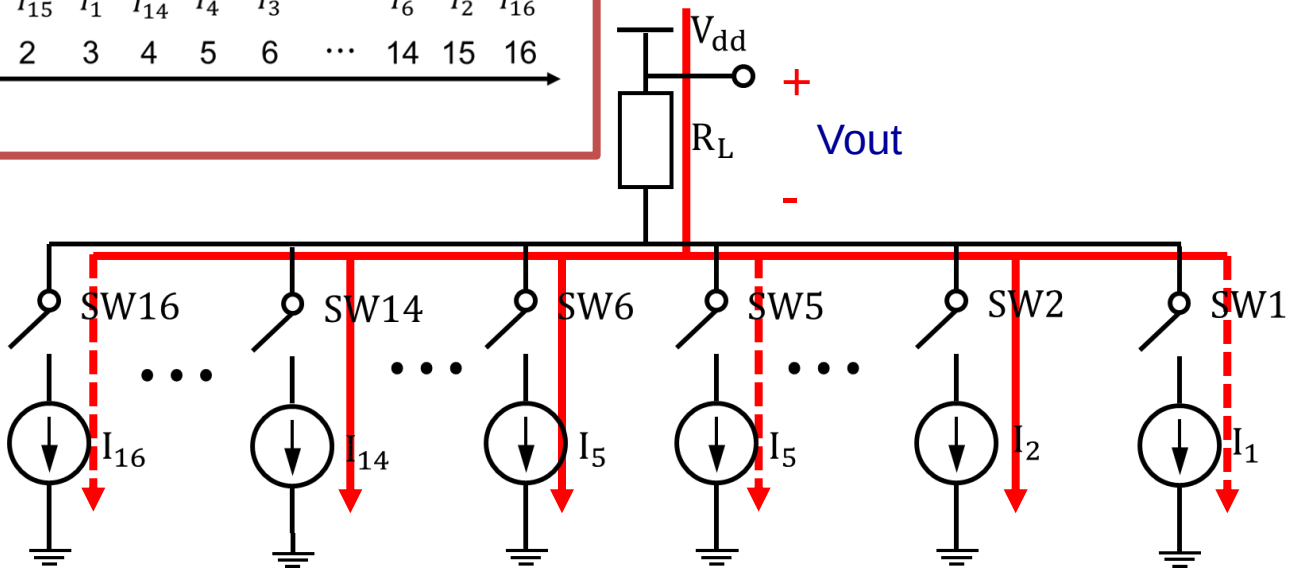
- Unit current source selection-order change algorithm

1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16



1. Measure the order of unit current cells
2. Align them virtually in magic square
3. Select current cells

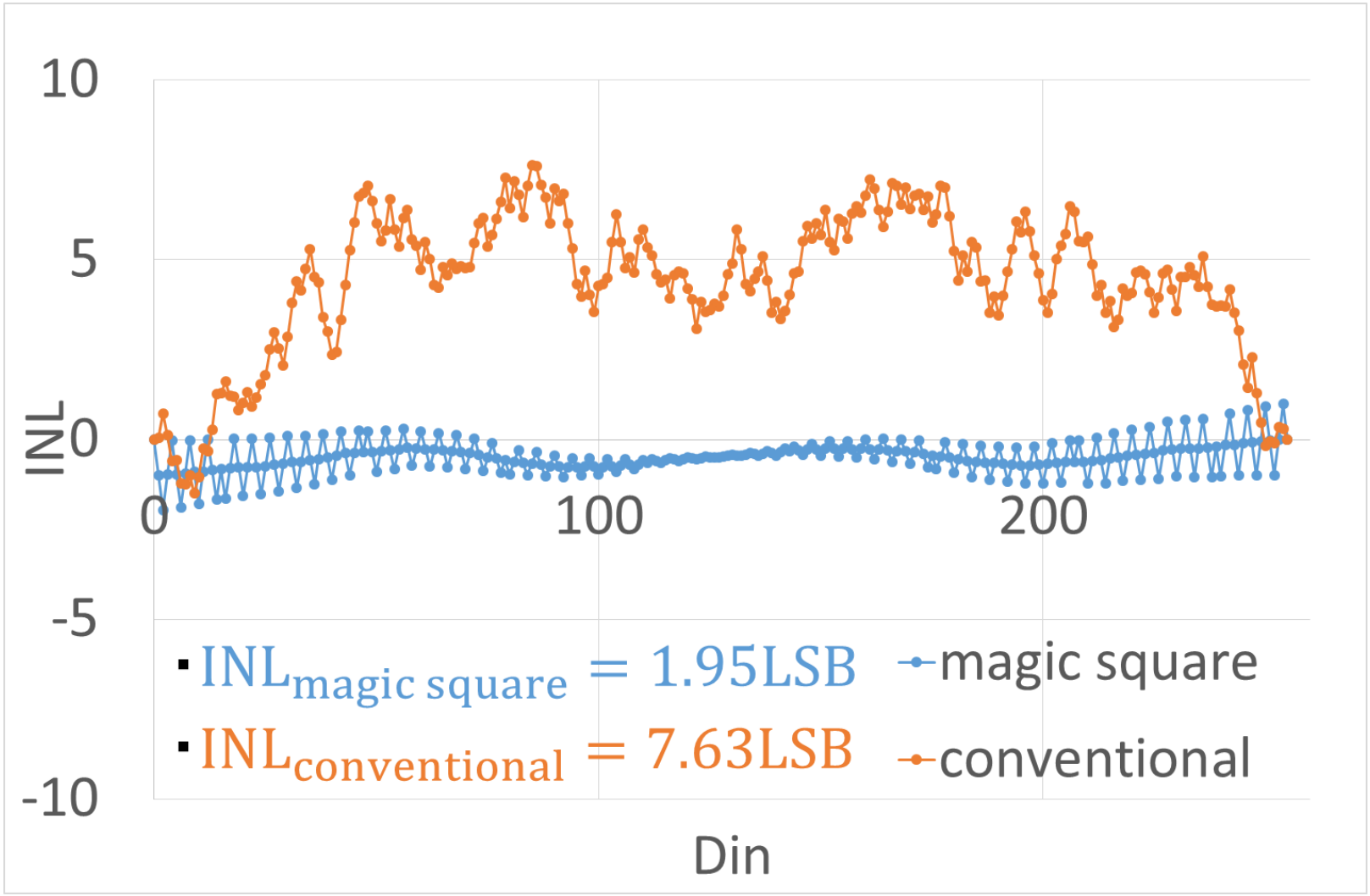
1	15	14	4
12	6	7	9
8	10	11	5
13	3	2	16



MATLAB Simulation Result

Integral Non-Linearity (INL)

- 5.7 LSB improvement by the magic square algorithm



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  - Gray Code and TDC Design
  - ΔΣ Modulation and TDC
- Conclusion

TDC: Time-to-Digital Converter

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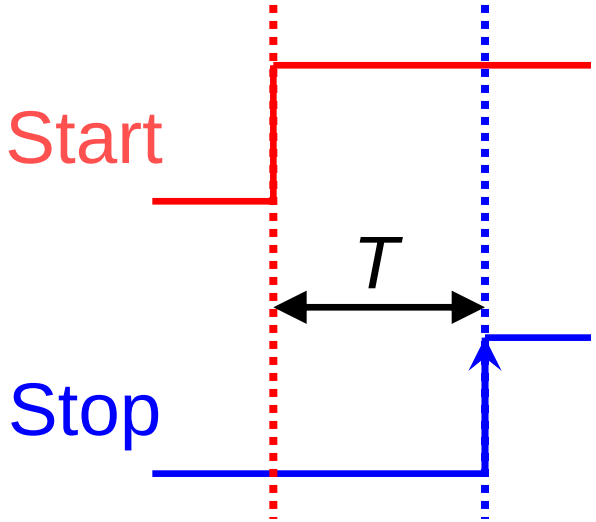
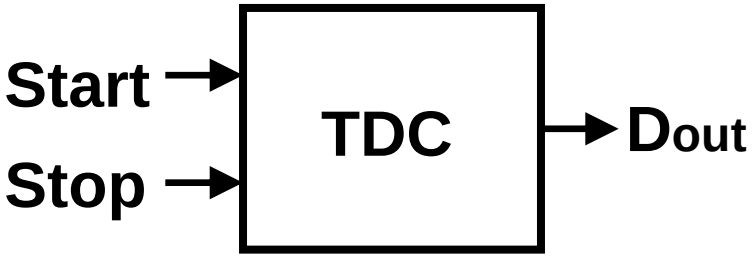
TDC: Time-to-Digital Converter

Time to Digital Converter（TDC）

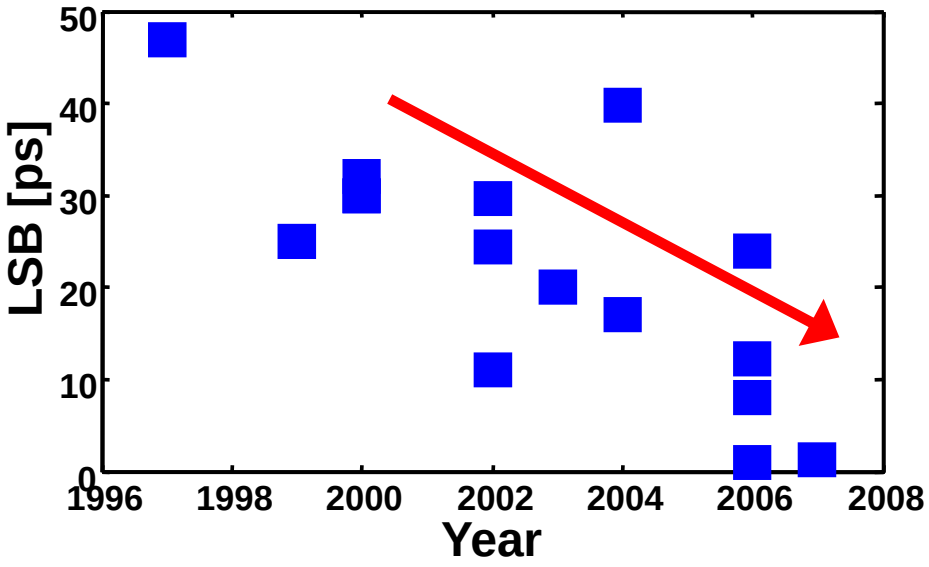
- time interval → Measurement → Digital value



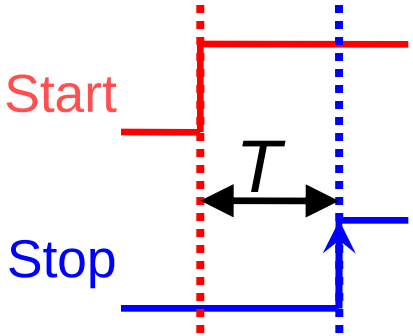


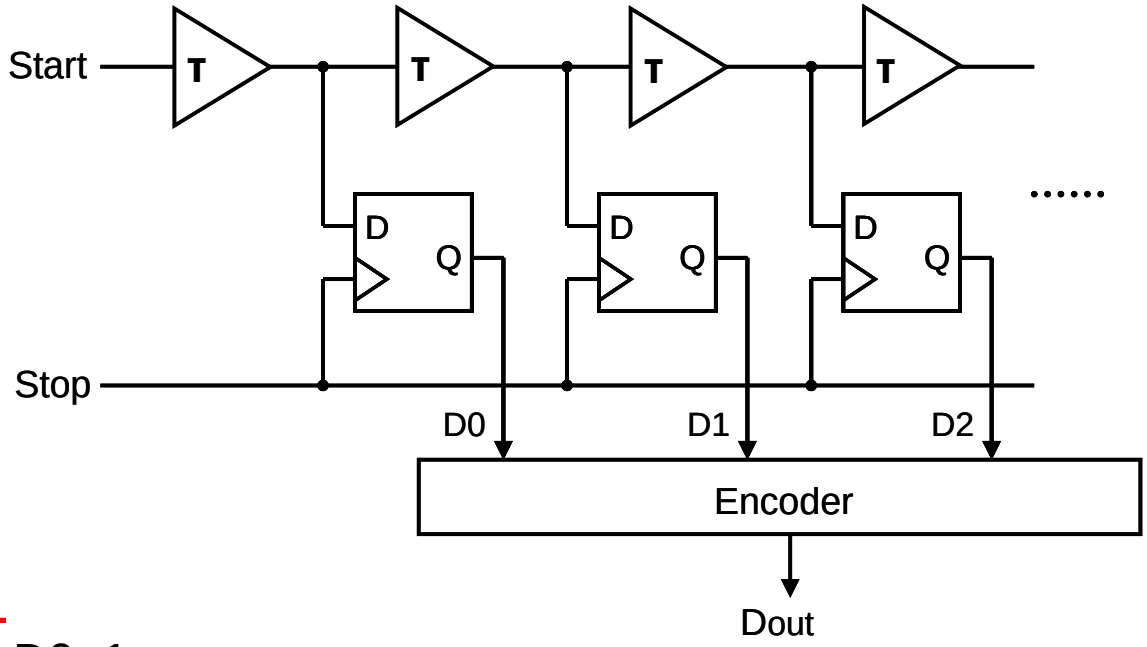
- Key component of time-domain analog circuit
- Higher resolution can be obtained with scaled CMOS

Higher resolution with CMOS scaling

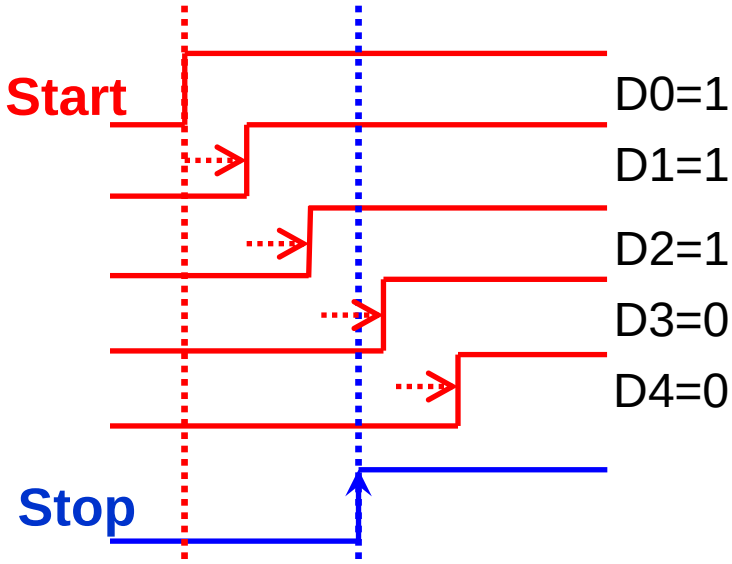


Flash-type TDC





Timing chart

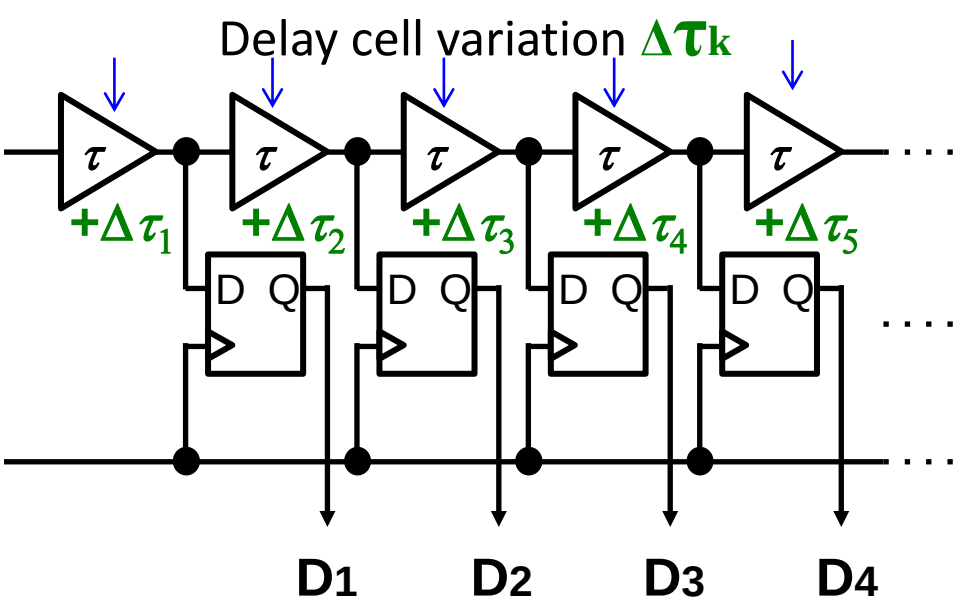


Encoder

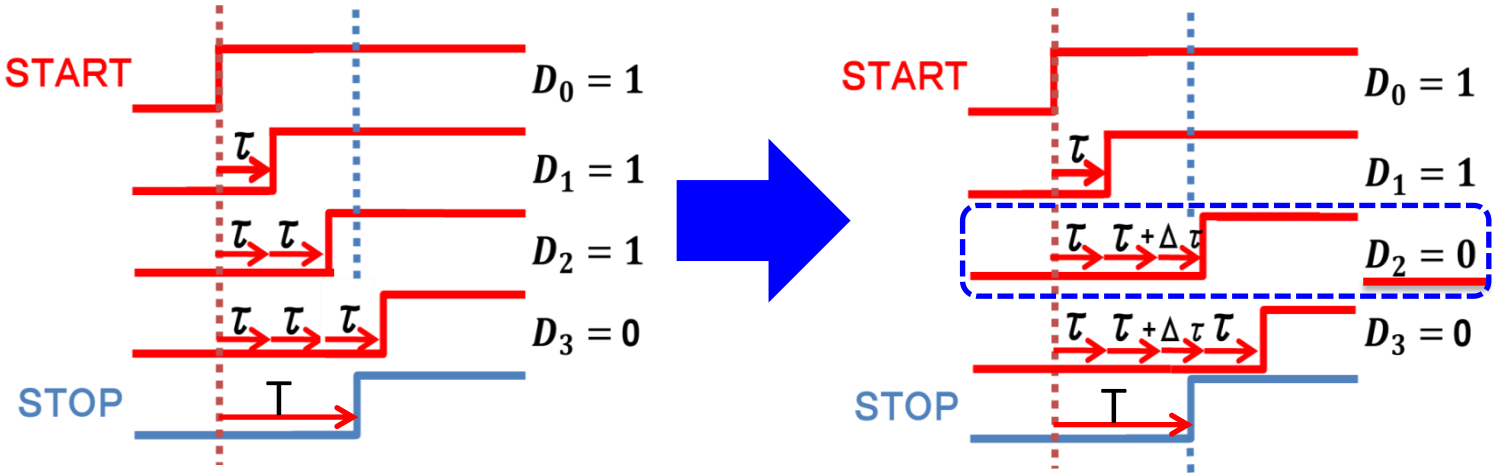
Thermometer code

binary code

Delay Cell Variation Inside TDC Circuit



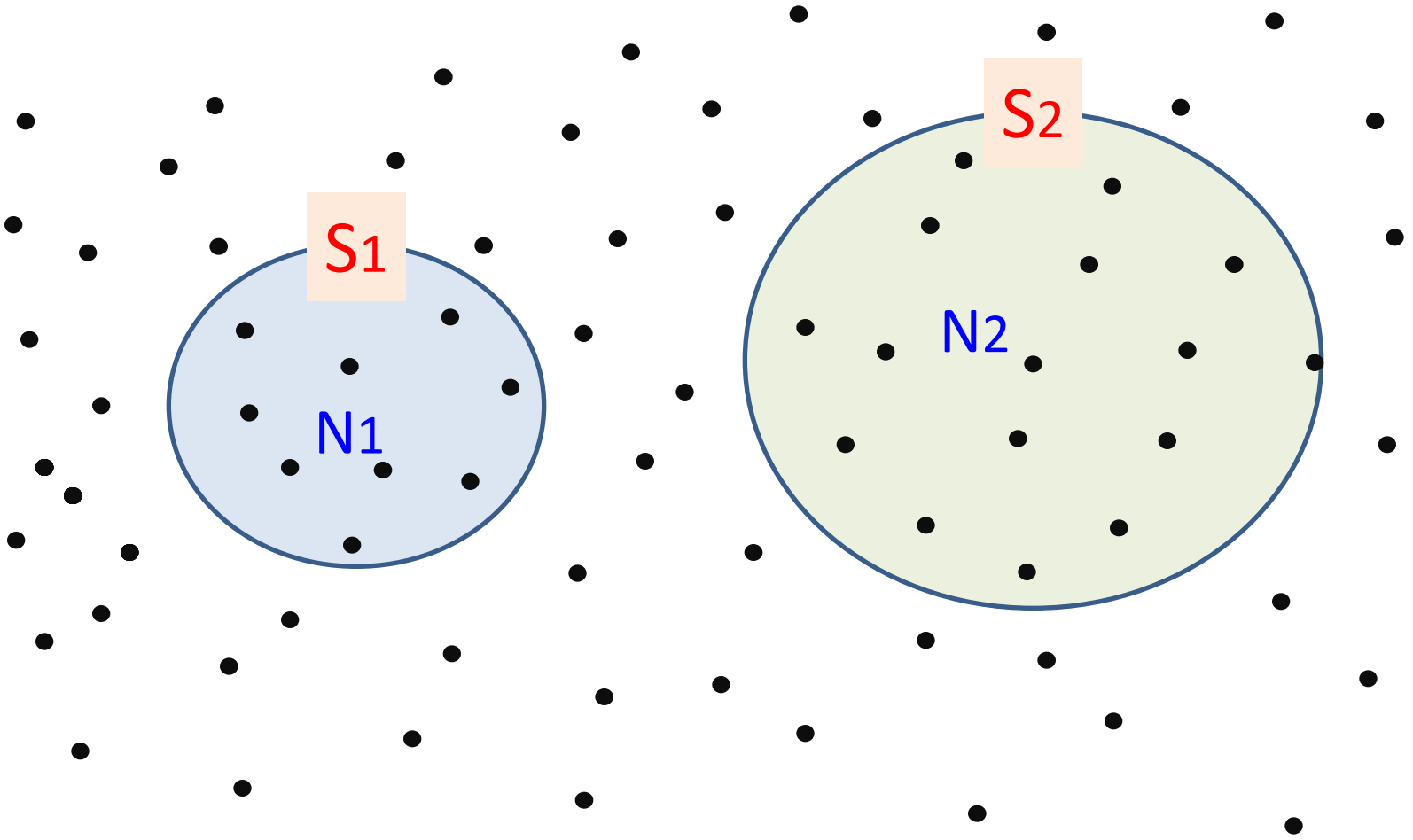
TDC nonlinearity



(a) Without delay variation

(b) With delay variation

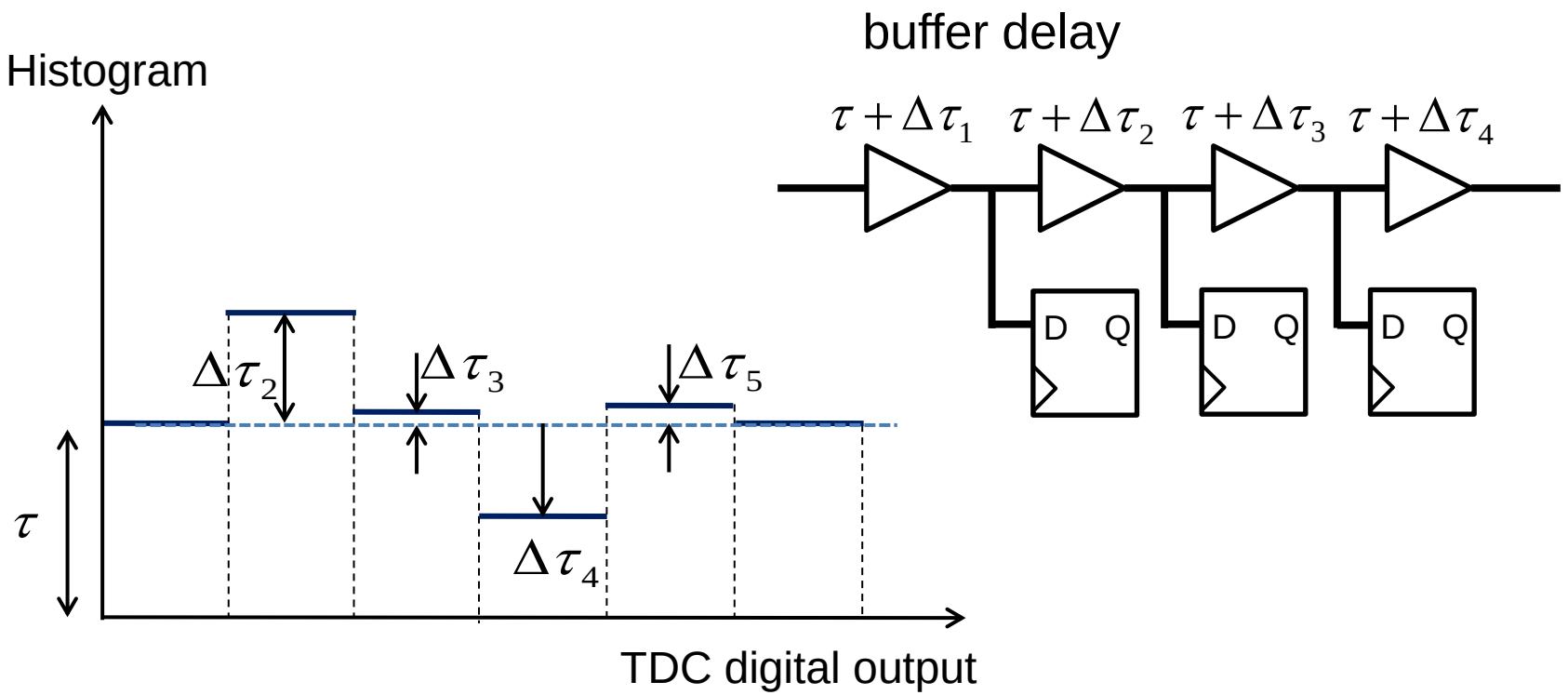
Measurement with Histogram



# of dots ratio $\frac{N1}{N2}$ ⇒ Area ratio $\frac{S1}{S2}$

Delay Variation Measurement with Histogram

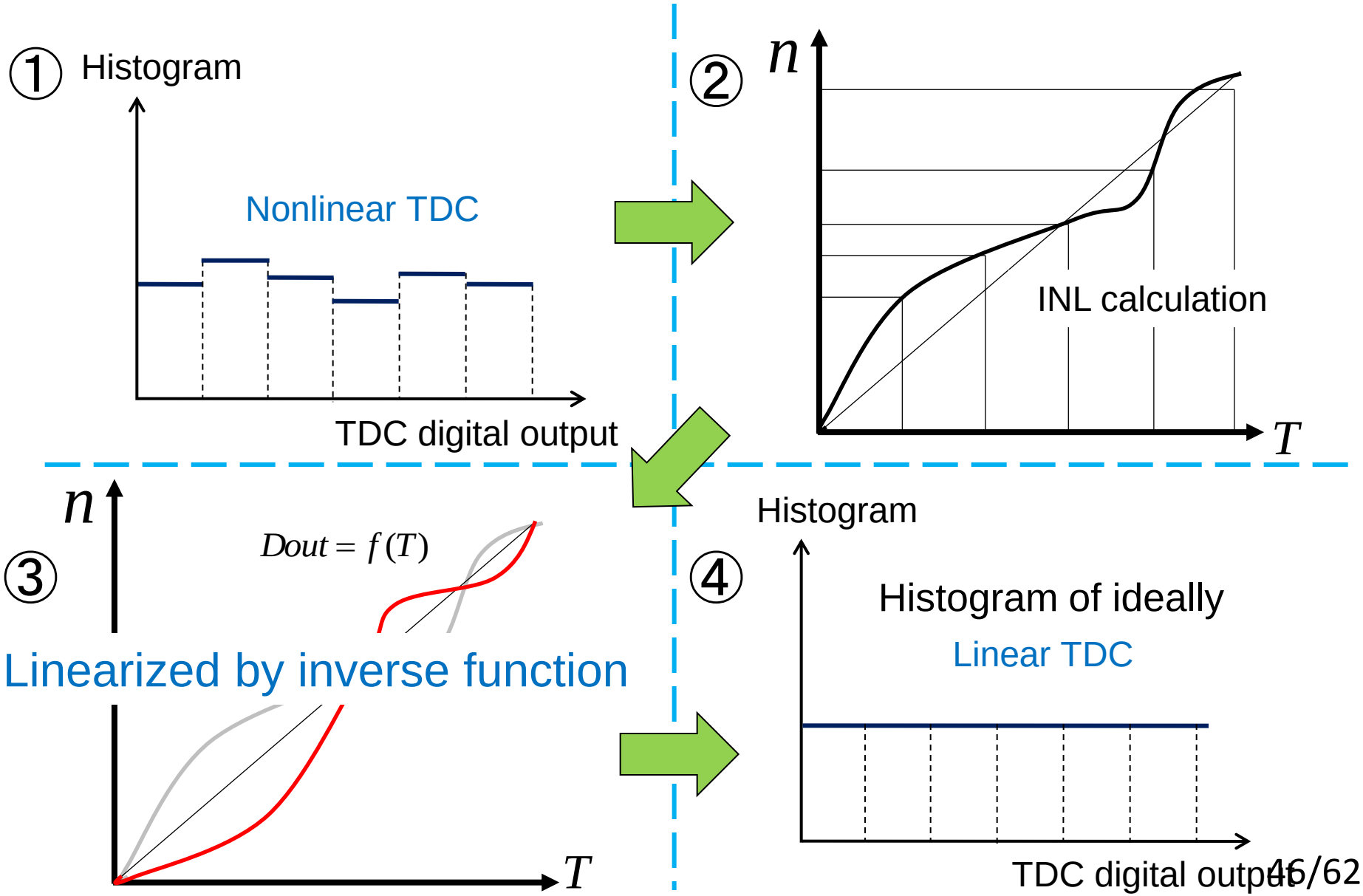
TDC is non-linear due to delay variation



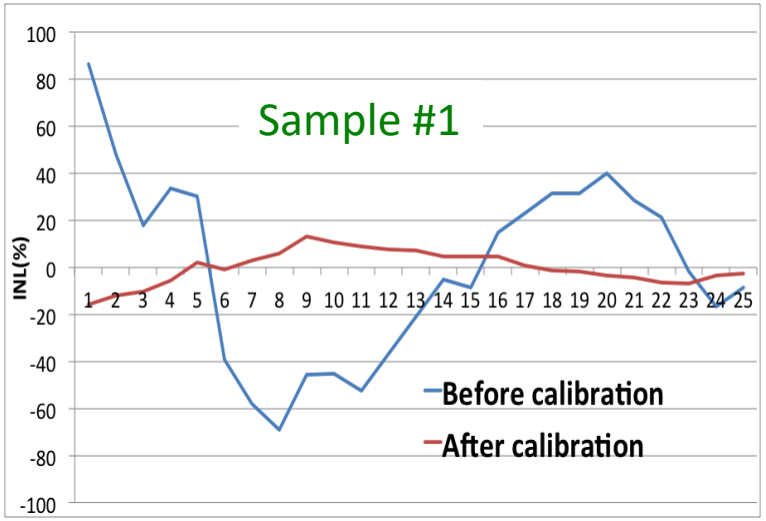
[1] S. Ito, H. Kobayashi, "Stochastic TDC Architecture with Self-Calibration," IEEE APCCAS (Dec. 2010).

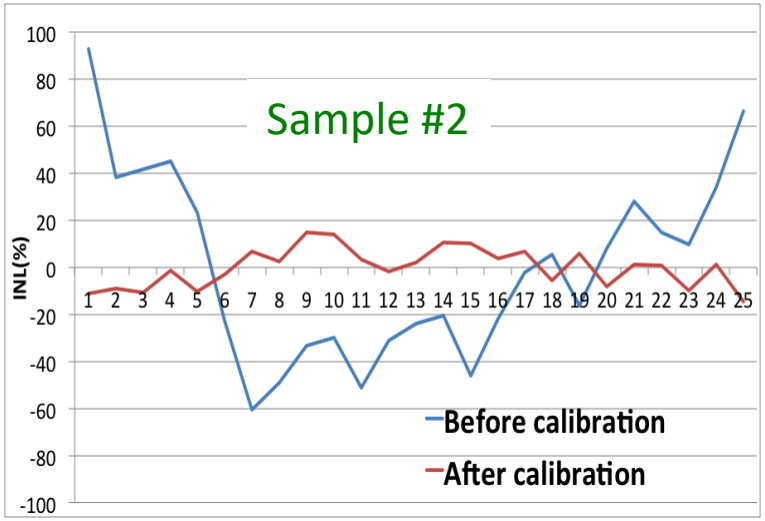
[2] T. Chujo, H. Kobayashi, "Experimental Verification of Timing Measurement Circuit With Self-Calibration", IEEE IMS3TW (Sept. 2014).

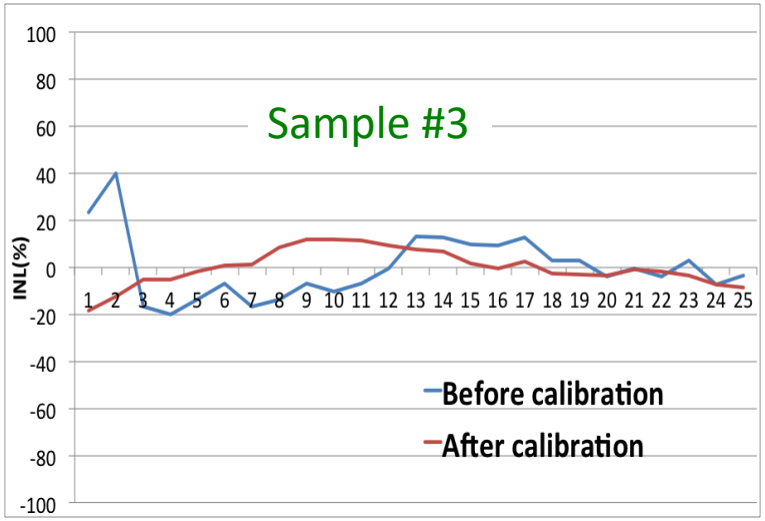
Principle of Self-Calibration

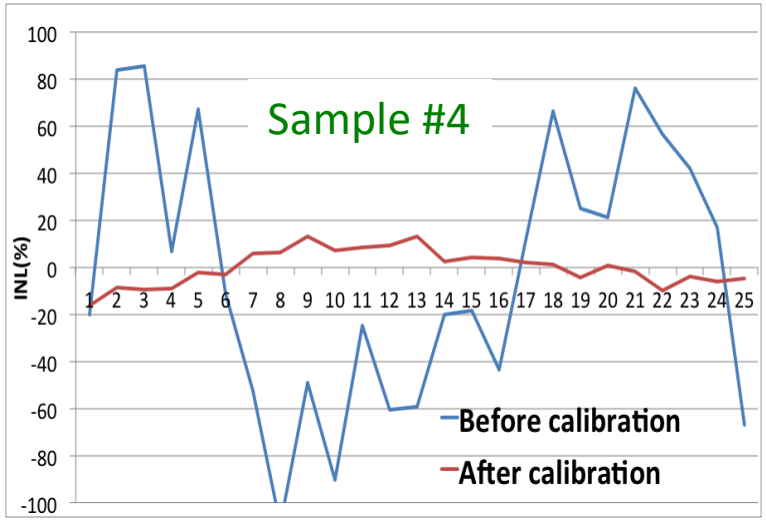


Measurement Results (INL)









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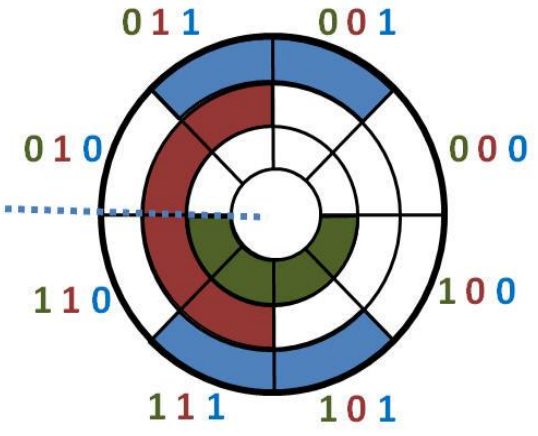
TDC: Time-to-Digital Converter

Concept of Gray code

Gray code is a binary numeral system
where two successive values differ in only one bit.

4-bit Gray code vs. 4-bit Natural Binary Code

Decimal numbers	Natural Binary Code	4-bit Gray Code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

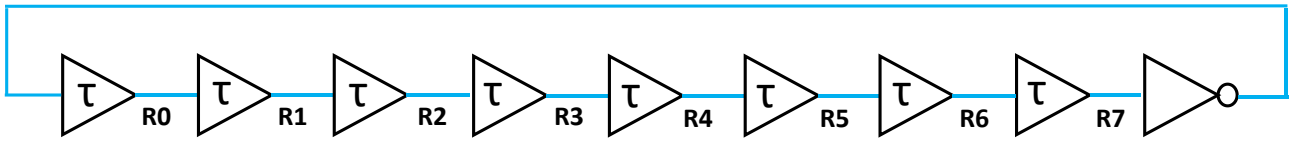


Frank Gray and A. L. Johnsrud in television booth. Behind the glass panels at sides and top are the photo-electric cells.

Gray code was invented by Frank Gray at Bell Lab in 1947.

How to utilize Gray code in TDC

In a ring oscillator, between any two adjacent states, only one output changes at a time.



8-stage Ring Oscillator Output								4-bit Gray Code			
R0	R1	R2	R3	R4	R5	R6	R7	G3	G2	G1	G0
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	1	1
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	1	1	0
1	1	1	1	1	0	0	0	0	1	1	1
1	1	1	1	1	1	0	0	0	1	0	1
1	1	1	1	1	1	1	0	0	1	0	0
1	1	1	1	1	1	1	1	1	1	0	0
0	1	1	1	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	0
0	0	0	0	1	1	1	1	1	0	1	0
0	0	0	0	0	1	1	1	1	0	1	1
0	0	0	0	0	0	1	1	1	0	0	1
0	0	0	0	0	0	0	1	1	0	0	0

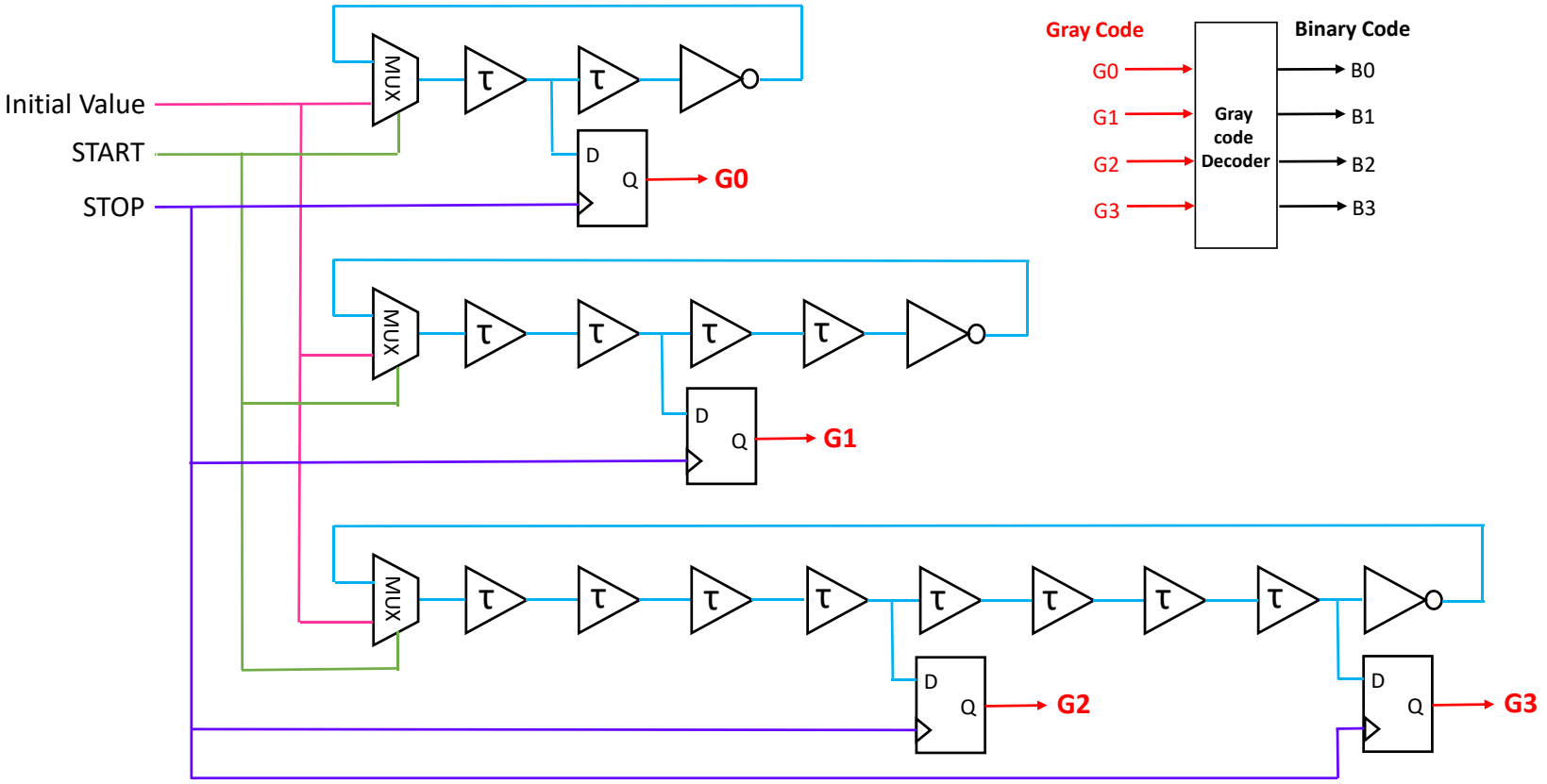
For any given Gray code, each bit can be generated by a certain ring oscillator.

Proposed 4-bit Gray code TDC

A large Flash TDC

Convert

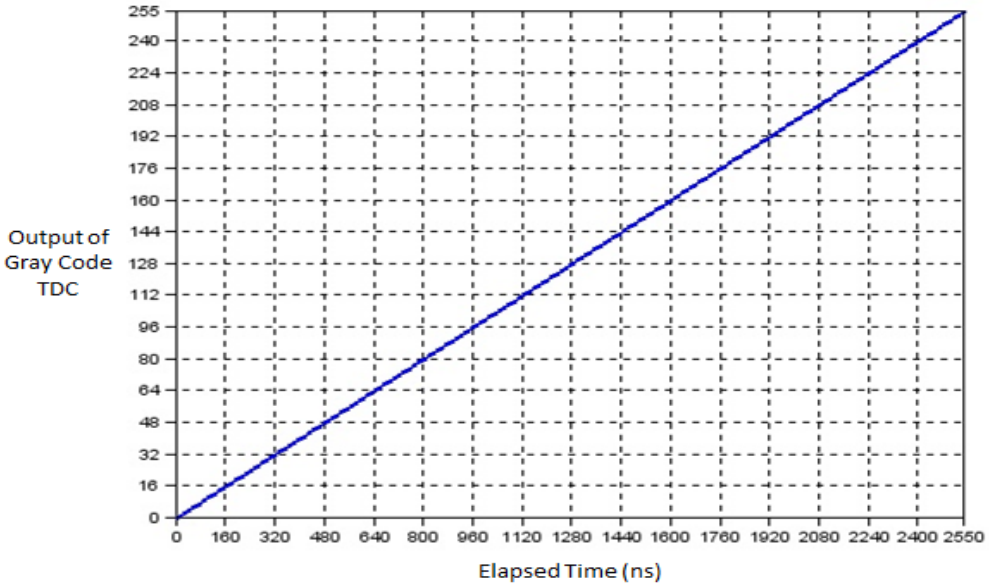
A set of smaller Flash TDCs performed in parallel



Proposed Gray code TDC architecture in 4-bit case

FPGA measurement results of 8-bit Gray code TDC

FPGA implementation of
Gray code TDC



Gray code TDC works with good linearity as expected

[1] C. Li, H. Kobayashi, "A Gray Code Based Time-to-Digital Converter Architecture and its FPGA Implementation", IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), Sendai, Japan (Aug. 26-28, 2015).

Flash TDC vs. Gray code TDC

	Number of delay cells	Number of DFFs	Maximum stage of RO
Gray code TDC	$2^n - 2$	n	2^{n-1}
Flash-type TDC	2^n	2^n	2^n

For large measurement range, the number of flip-flops in Gray code TDC decreases rapidly ($n \ll 2^n$)

Reduction of circuit complexity!!

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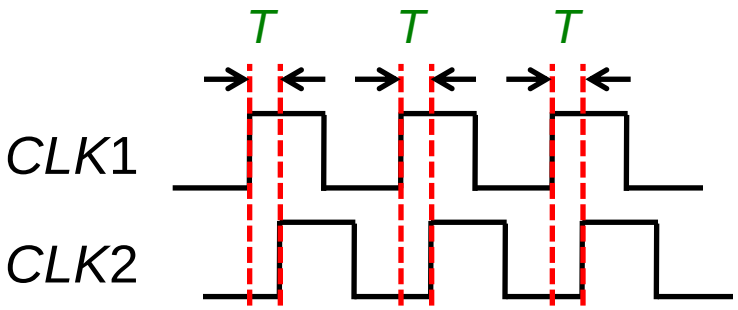
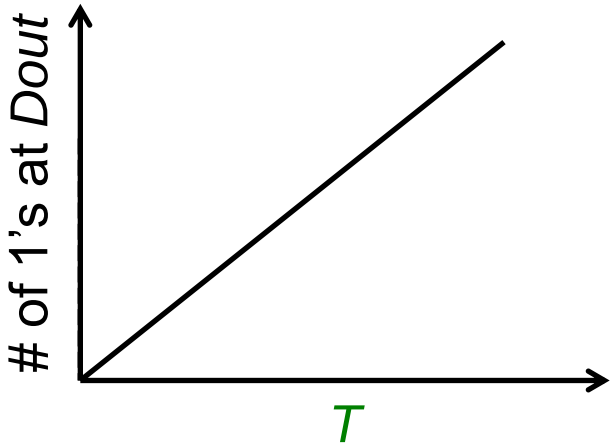
TDC: Time-to-Digital Converter

ΔΣ TDC Features

Timing *T* measurement between CLK1 and CLK2

ΔΣ Time-to-Digital Converter (TDC)

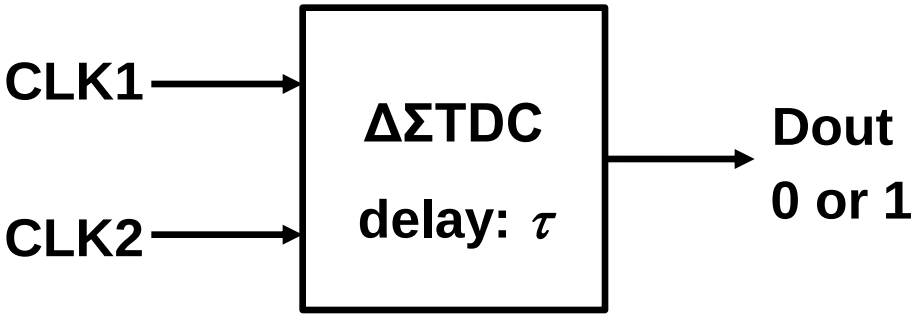


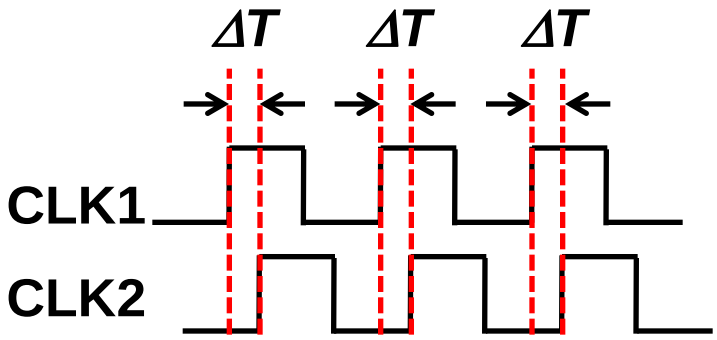


T ∝ # of 1' at *Dout*

- Simple circuit
- High linearity
- Measurement time → longer ⇒ time resolution → finer

Principle of ΔΣTDC





Dout # of 1's is proportional to ΔT

ΔT

# of 1's

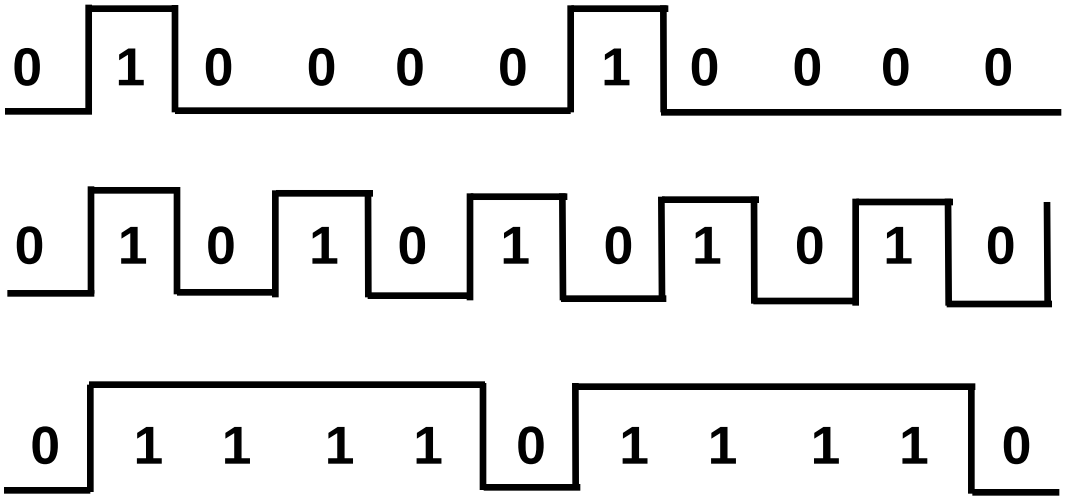
Dout

short

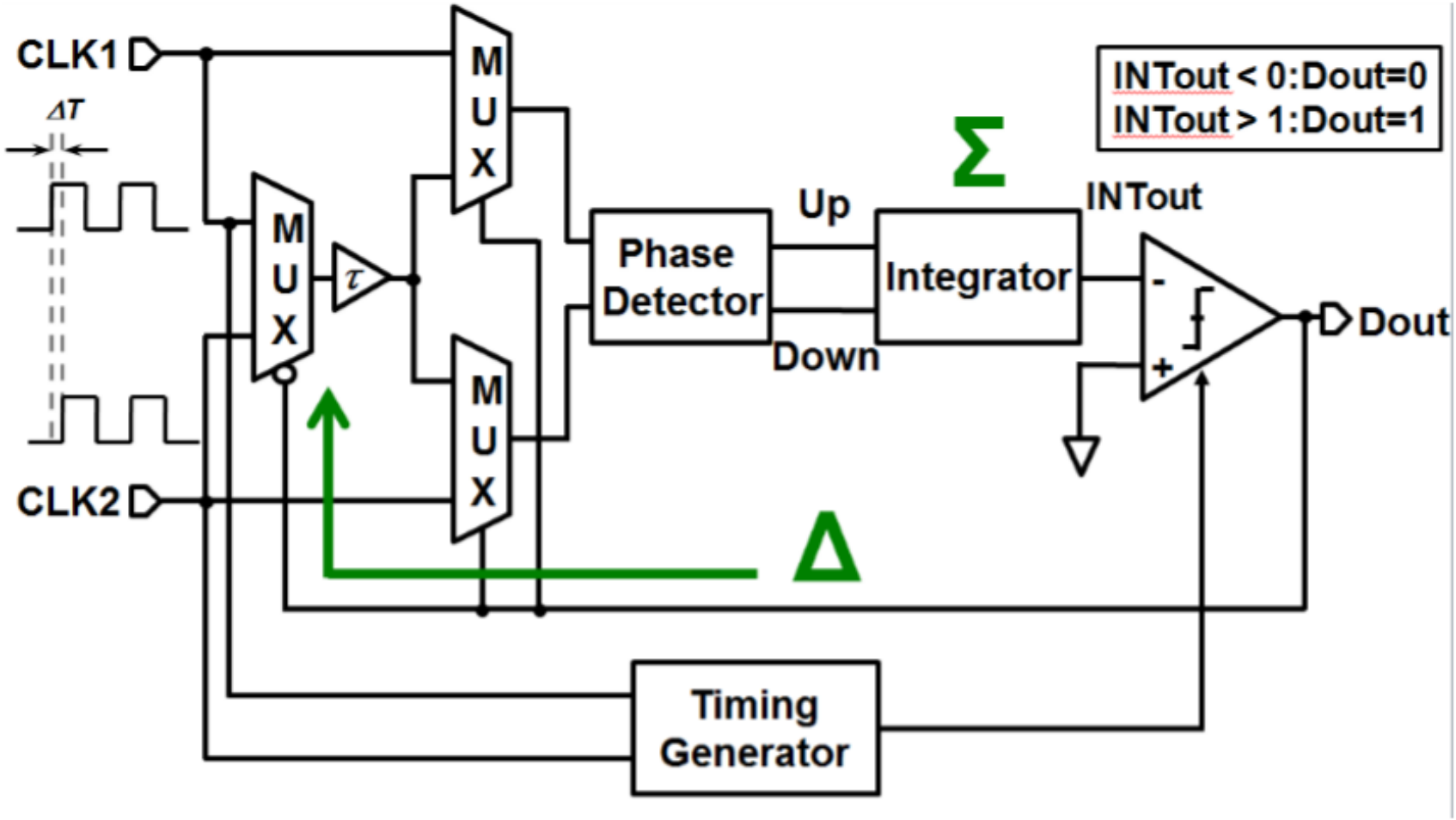
few

long

many



ΔΣTDC Configuration

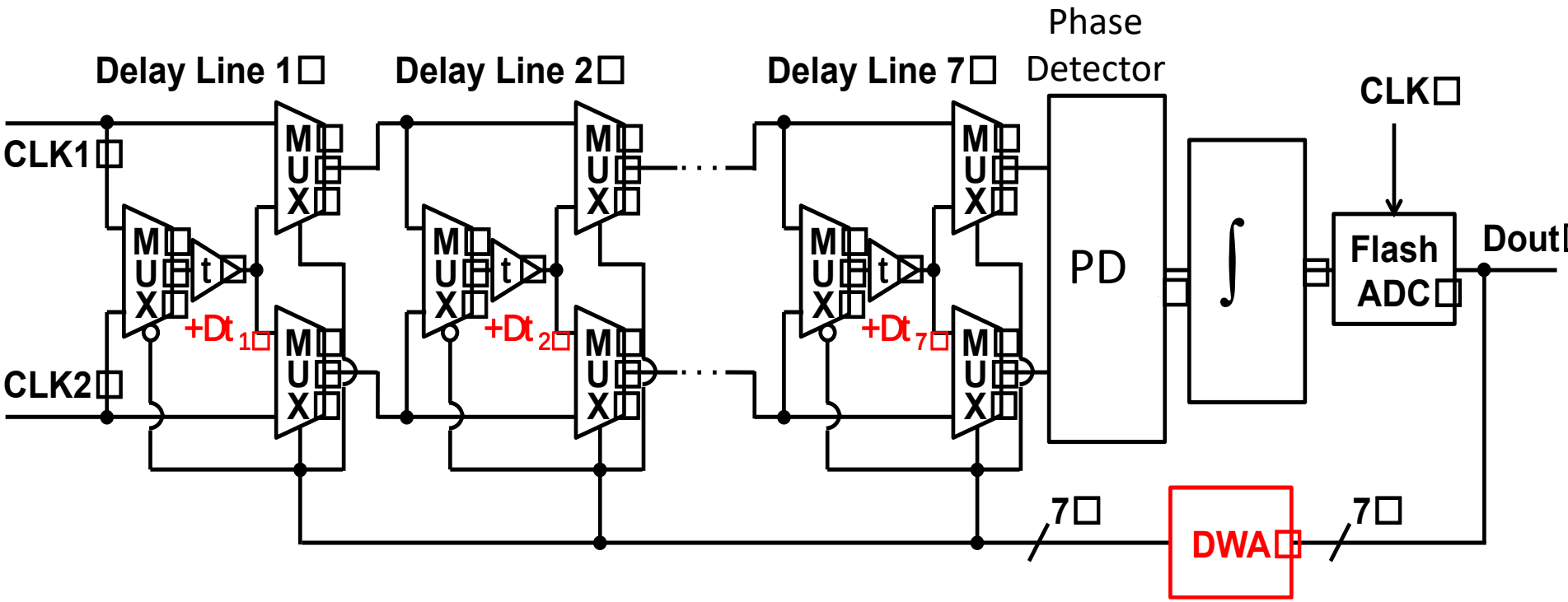


[1] T. Chujo, H. Kobayashi, "Timing Measurement BOST With Multi-bit Delta-Sigma TDC", IEEE IMSTW (June 2015).

[2] Y. Osawa, H. Kobayashi, "Phase Noise Measurement Techniques Using Delta-Sigma TDC", IEEE IMS3TW (Sept. 2014).

Multi-bit ΔΣTDC

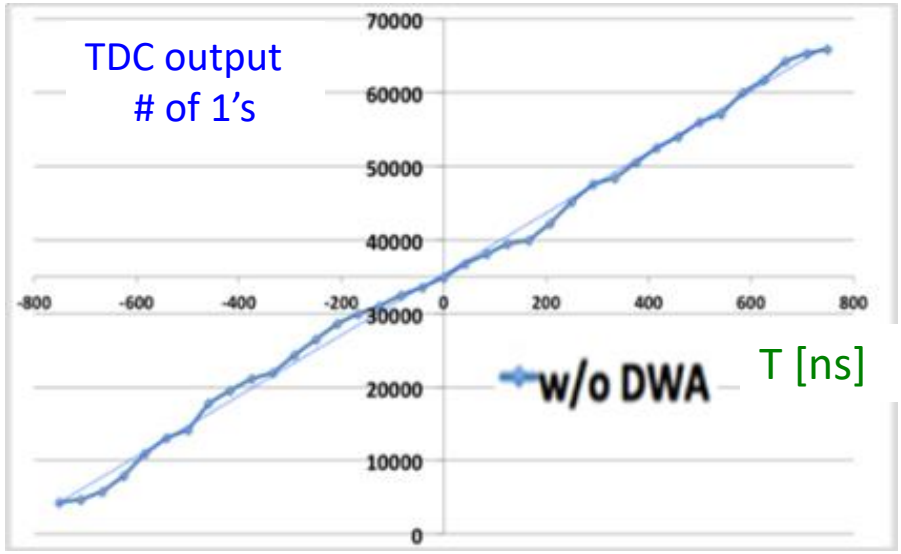
For short measurement time:

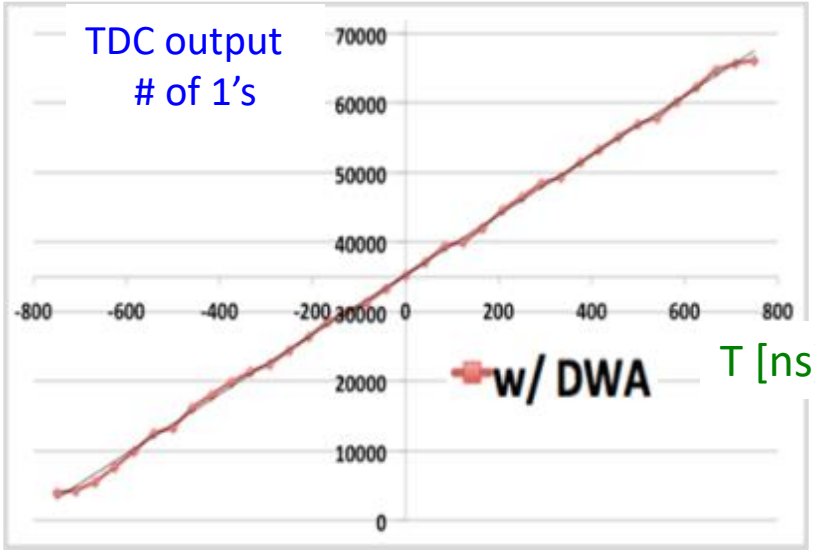


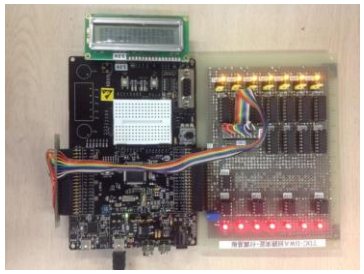
DWA: Data Weighted Averaging

DSP algorithm of compensation for mismatches among delays.

Measured Result

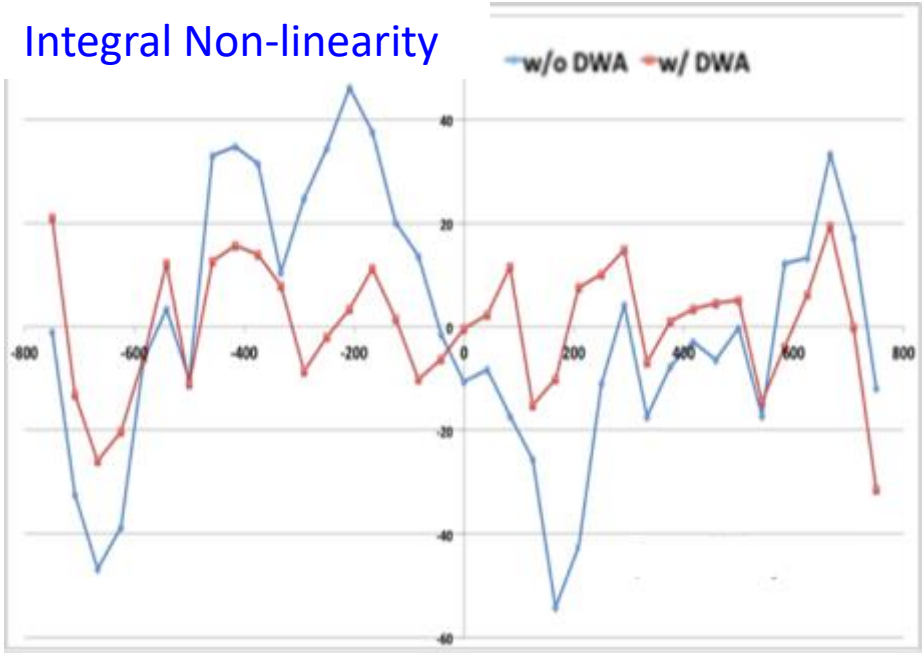






Analog FPGA Implementation

Integral Non-linearity



10,000 TDC output data are measured.

Contents

Conclusion

- Traditionally, people believe that analog / mixed-signal circuit design is art and craft.

- Here we show that mathematics can contribute to the design as science.

Both art and science are used for good analog / mixed-signal circuit design

思而不学則殆

Analog /mixed-signal IC designers
should study mathematics
for sophisticated design.

Kobayashi
Laboratory