DAC Linearity Improvement Algorithm With Unit Cell Sorting Based on Magic Square

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ABSTRACT

This paper proposes a switching algorithm using magic square properties to improve the linearity of a unary DAC by canceling random and systematic mismatch effects among unit current (or capacitor) cells. Simulation results and discussions are provided for DAC linearity comparison in case that the proposed magic square and conventional algorithms are used.

INTRODUCTION

Recently, electronic devices such mobile phones, wireless modems and tablet terminators demand for small-sized, high-speed and high-linearity digital-to-analog-converters (DACs). Especially, in fields of wireless communication, the accuracy (linearity) of the DAC is very important to ensure little interference leakage during transmission. Semiconductor devices on silicon wafer suffer from random and systematic mismatches regarding to characteristics of MOSFETs, resistors, and capacitors, which cause input and output relationships of the DAC to be non-linear.

In this paper we propose a unit cell sorting algorithm based on magic square properties for improvement of the DAC linearity (we consider here both integral nonlinearity (INL) and differential nonlinearity (DNL)). Since not only the static performance but also the dynamic performance are important, we aim to improve spurious free dynamic range (SFDR).

In most cases, a unary DAC decodes a binary code of the digital input into a thermometer code and turns on current source cells depending on it to produce an analog output signal. However in actual chip implementation, the DAC linearity is degraded due to current source mismatches. Hence, we propose here a unit cell sorting algorithm based on magic square calibration to cancel the random and systematic mismatch effects; magic square is a kind of a classical mathematics [1]. We have developed linearity improvement algorithm with one-time calibration by using "constant sum" characteristic of the magic square. We show its simulation results to demonstrate its effectiveness, and provide some considerations.

UNARY DAC ARCHITECTURE

A unary DAC employs a unary weighted (identical) current source structure (FIG.1). The unary weighted structure requires 2^N-1 unit current sources for N-bit resolution where all current source weights are identical as expressed in eq. (1):

$$I_1 = I_2 = \cdots = I_{14} = I_{16} = I \qquad (1)$$

For the operation of the unary weighted structure, a binary-to-thermometer code decoder is required. The unary DAC has characteristics of small glitch and inherent monotonicity. But this architecture suffers from large decoder circuits and many switches which increase silicon chip area.

DAC NONLINEARITY

In practical CMOS technologies, the current source mismatches are influenced by their threshold voltage mismatch and/or by the slope mismatch (Fig.2). Ideal drain current I_d in saturation region is given by

$$I_{d,1} = \frac{\beta}{2}\left(V_{gs} - V_{th1}\right)^2 \qquad (2)$$

Also drain current mismatch is given by

$$\frac{\Delta I_{d1}}{I_{d1}} = \frac{2}{V_{gs} - V_{th1}} \frac{A v_{th} t_{ox}}{\sqrt{WL}} \qquad (3)$$

Current mismatches are dependent on their device sizes. Note that here, we are considering to reduce the DAC nonlinearity effects of the current mismatches due to small device size $\left(\sqrt{WL}\right)$.

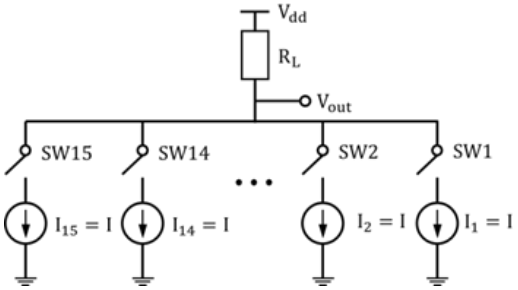


FIG 1. Unary DAC.

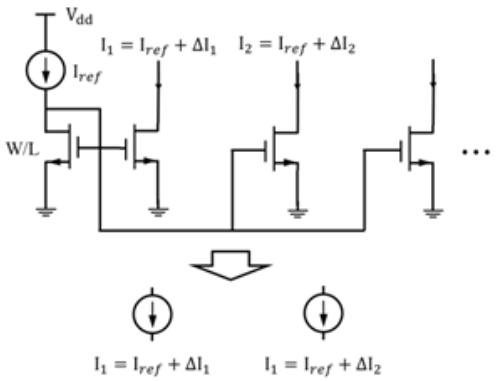


FIG 2. Mismatches among current sources.

MAGIC SQUARE

Characteristic of the magic square is a constant sum of each row, column and diagonal [1]. We consider that this characteristic is good balance for unit cell arrange sorting for DAC linearity improvement by cancelling random and systematic mismatch effects among unit cells. We propose a unary DAC linearity improvement algorithm by using magic square.

Now we explain about the magic square. Magic square is a square matrix where different integers are arranged to begin with 1 into n×n. Furthermore, each row, column, and diagonal have the same sum. Generally, we call the n×n magic square matrix as an *n* class magic square. Constant sum of the *n* class magic square is expressed as follows:

$$S = \frac{n\left(n^2+1\right)}{2} \quad (4)$$

We show a 3×3 magic square in Fig.3, and there we can confirm its constant sum characteristics.

DIGITAL CALIBRATION ALGORITHM

In this section, we propose a digital calibration algorithm based on magic square for the unary current-steering DAC [2-5]. We aim one-time calibration; the new digital algorithm can improve the linearity of the DAC recovering from the effect of the current source mismatches. At the same time, the optimized switching sequence can suppress the distortion especially caused by 2nd and 3rd order harmonics for better dynamic performance. This section discusses the essence of the proposed digital algorithm as well as calibration technique (Fig.4).

Note the current measurement circuit only needs to measure the order of the current sources and does not need their accurate value measurement. The measurement circuit can be simply designed as a ring-oscillator-based circuit [3][7].

1. Current Source Sorting Based on Magic Square

We use a 4-bit unary DAC as an example to explain the proposed algorithm.

① Assume the initial condition of current sources after fabrication

② Then, 16 available current source cells are sorted by their values (Fig.4 ①)

③ The order of the current source values and the magic square algorithm are adopted. For example, the smallest current source (I_5) is adopted to "1" cell in the magic square. The second small current source (I_{15}) is adopted "2" cell in the magic square. Hence, n-th current source (I_n) is adopted "n" cell in magic square (Fig.4②).

④ A current source cell corresponding to the magic square according to the constant sum, turns on corresponding to the digital input to obtain the DAC analog output value (Fig.4③).

We can cancel the random and systematic mismatches by sorting current sources according to constant sum characteristics. We focus on array of the magic square. In Fig.4 ③ of the magic square, we see at the first column that the sums of adjacent two numbers is almost equal (16 for 1, 15 and 18 for 14, 4)). We understand that they are almost the same. It is similar in other lines. Sorting current sources according to constant sum is based on an algorithm to perform switching of current sources with large mismatch and small mismatch to turn on, and we can cancel mismatch effects. In Fig.5, we show look-up table (LUT) of the conventional method of a thermometer-code decoder, and the proposed method of a magic square switching-code decoder.

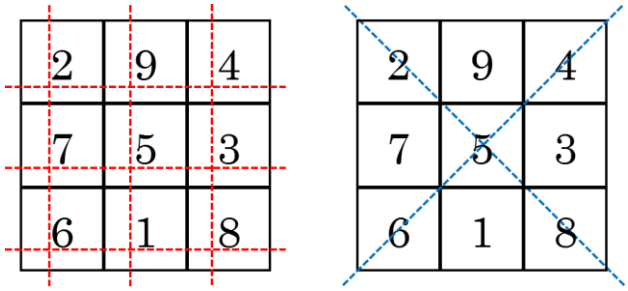


FIG.3 Constant sum characteristics of magic square.

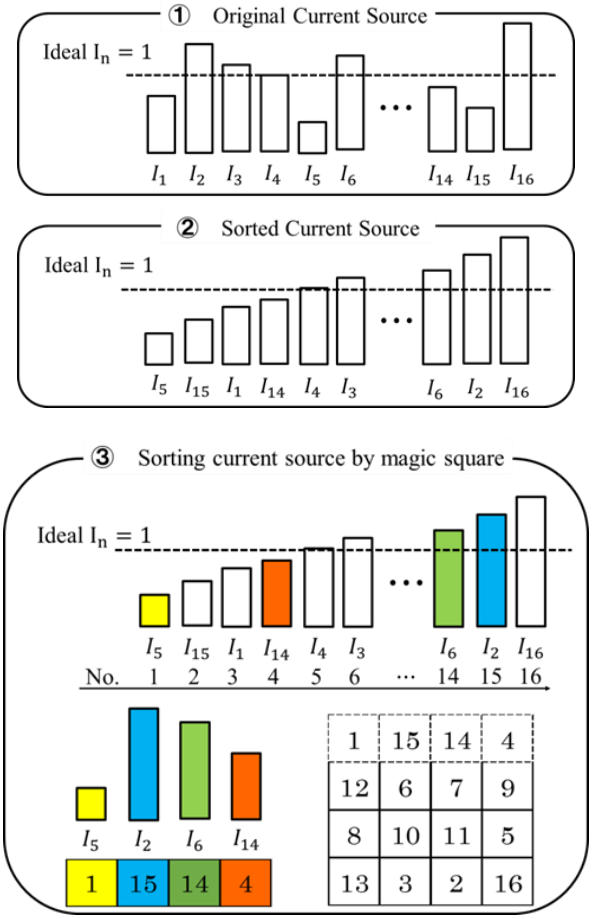


FIG.4 Sorting algorithm based on magic square.

2. Calibration Technique

We consider here a calibration technique with the error measurement approach to meet with our proposed techniques (Fig.6). Our proposed calibration steps are as follows:

① Input test codes are inserted by central processing unit (CPU) that controls the digital calibration circuit. Digital calibration circuit utilizes ring oscillator-based measurement circuit [3].

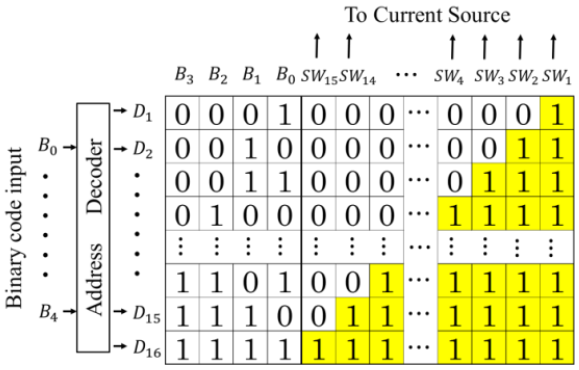
② By implementing current measurement circuit, current source cell values are measured.

③ All measured values are sorted in memory.

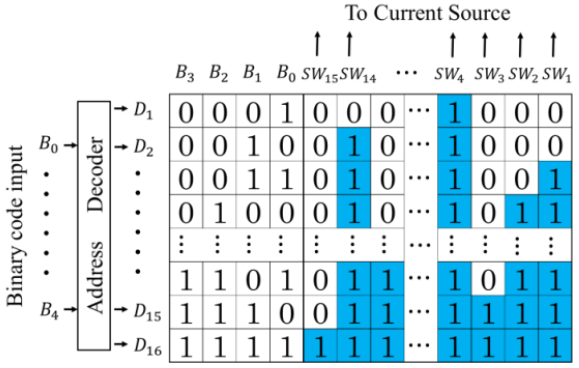
④ Then, these data are fed into digital calibration circuit to perform main calibration process.

⑤ Finally, the optimized switching sequence based on magic square is stored in memory.

The optimized switching sequence is used during DA conversion.



(a) Conventional thermometer-to-binary decoder.



(b) Magic square algorithm decoder

FIG.5 LUT-based decoder.

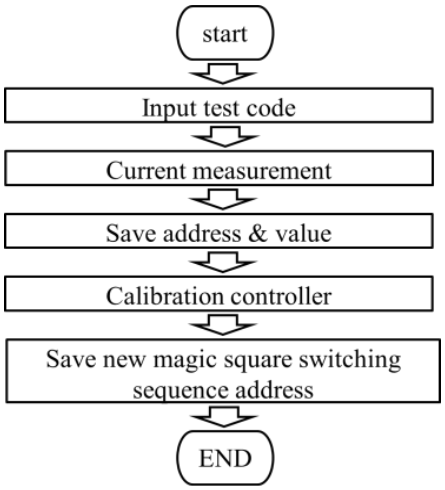


FIG.6 DAC nonlinearity calibration algorithm.

SIMULATION RESULT

We have simulated static and dynamic performances of an 8-bit unary DAC. We have compared the conventional method of the thermometer-code decoder and the proposed current source sorting algorithm based on magic square. The static performance was simulated as INL and DNL. The simulated dynamic performance was obtained as SFDR. In Fig.7, we show the magic square used for the 8-bit unary DAC calibration. The magic square was obtained by MATLAB. Mismatch of current sources was generated as a random number between -1 from +1. We show the simulation results in FIG.8-11.

1. Static Performance

In order to verify the simulated linearity of the proposed DAC, the static performance parameters, INL and DNL have been obtained. The simulation result shows that INL of 7.63 LSB before calibration has been improved to 1.95 LSB using the proposed calibration technique (Fig.8), and also DNL has been improved (Fig.9). We note that INL and DNL are nearly 0.0 in the center of input range Din (=122).

2. Dynamic Performance

In the frequency domain, the conventional method using the thermometer-code decoder unary 8-bit DAC shows the SFDR performance of 14.8 dB (Fig.10). Our proposed calibration technique of current source cell sorting based on magic square obtains SFDR of 22.0dB (Fig.11), and we see that 7dB improvement of the DAC SFDR using the proposed method is obtained.

256	2	3	253	252	6	7	249	248	10	11	245	244	14	15	241
17	239	238	20	21	235	234	24	25	231	230	28	29	227	226	32
33	223	222	36	37	219	218	40	41	215	214	44	45	211	210	48
208	50	51	205	204	54	55	201	200	58	59	197	196	62	63	193
192	66	67	189	188	70	71	185	184	74	75	181	180	78	79	177
81	175	174	84	85	171	170	88	89	167	166	92	93	163	162	96
97	159	158	100	101	155	154	104	105	151	150	108	109	147	146	112
144	114	115	141	140	118	119	137	136	122	123	133	132	126	127	129
128	130	131	125	124	134	135	121	120	138	139	117	116	142	143	113
145	111	110	148	149	107	106	152	153	103	102	156	157	99	98	160
161	95	94	164	165	91	90	168	169	87	86	172	173	83	82	176
80	178	179	77	76	182	183	73	72	186	187	69	68	190	191	65
64	194	195	61	60	198	199	57	56	202	203	53	52	206	207	49
209	47	46	212	213	43	42	216	217	39	38	220	221	35	34	224
225	31	30	228	229	27	26	232	233	23	22	236	237	19	18	240
16	242	243	13	12	246	247	9	8	250	251	5	4	254	255	1

FIG.7 Magic square used for simulation.

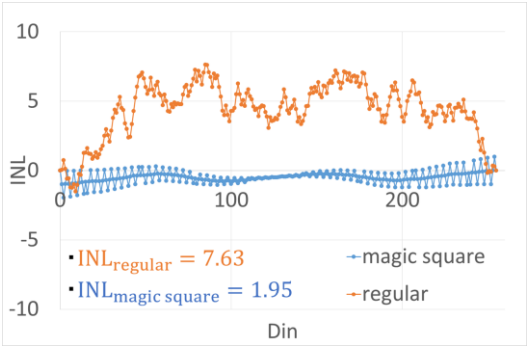


FIG.8 Simulated DAC INL.

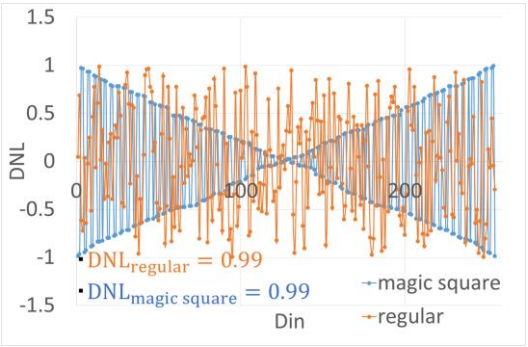


FIG.9 Simulated DAC DNL.

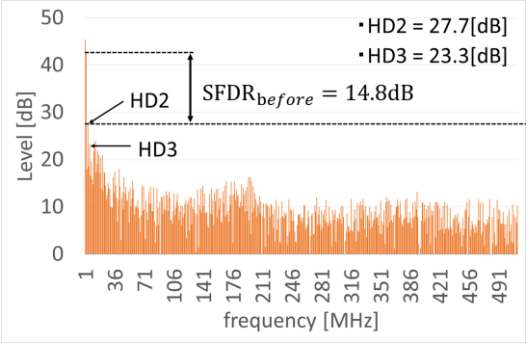


FIG10. Simulated DAC output power spectrum before calibration.

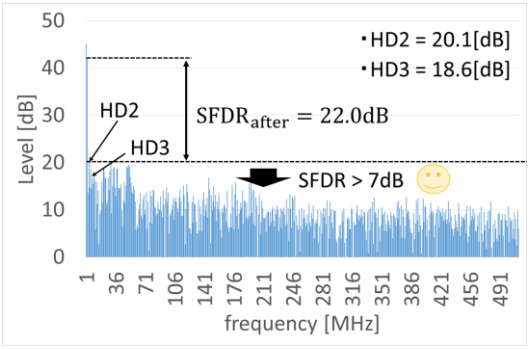


FIG11. Simulated DAC output power spectrum after the proposed calibration algorithm.

CONCLUSION

We have proposed a current source cell sorting algorithm based on magic square for unary DAC linearity improvement. The technique improves INL, and also DNL in the center of the input range. The better SFDR can be obtained with second and third harmonics suppression. The current measurement circuit only needs to measure the order of the current sources and does not need their accurate value measurement. It can cancel random and systematic mismatch effects of current sources by sorting current sources using the constant sum property of the magic square. We have shown in simulation that our proposed algorithm could improve static and dynamic performance with one calibration.

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REFERENCES

[1] K. Omori, The World of Magic Square, Nippon Hyoron Sha (Aug.2013)

[2] S. N. Mohyar, M. Murakami, A. Motozawa, H. Kobayashi, O. Kobayashi, T. Matsuura ”SFDR Improvement Algorithms for Current-Steering DACs,”Key Engineering Materials, pp.101-108 (2015).

[3] S. N. Mohyar, H. Kobayashi, “Digital Calibration Algorithm for Half-Unary Current-Steering DAC for Linearity Improvement,” 11th International SoC Design Conference, Jeju, Korea (Nov. 2014)

[4] T. Chen, G. Gielen, “A 14-bit 200-MHz Current-steering DAC with Switching-Sequence Post-Adjustment Calibration,” IEEE J. Solid-State Circuits (Nov.2007).

[5] Hans Van de Vel, Joost Briaire et. al., “A 240mW 16bit 3.2GHz/s DAC in 65nm CMOS with <-80dBc IM3 up to 600MHz,” Tech. Digest of ISSCC (Feb. 2014).

[6] Geert A. M. Van der Plas, Jan Vandenbussche, Willy Sansen, Michel S. J. Steryaert, and Georges G. E. Gielen, “A14-bit Intrinsic Accuracy Q^2 Random Walk CMOS DAC,” IEEE Journal of Solid-State Circuits (Dec. 1999).

[7] Y. Arakawa, Y. Oosawa, H. Kobayashi, O. Kobayashi, “Linearity Improvement Technique of Multi-bit Sigma-Delta TDC for Timing Measurement,” IEEE 3rd International Workshop on Test and Validation of High-Speed Analog Circuits, Anaheim, CA (Sept. 2013).