DAC Linearity Improvement Algorithm
With Unit Cell Sorting Based on Magic Square

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ABSTRACT

This paper proposes a switching algorithm using magic square properties to improve the linearity of a unary DAC by canceling random and systematic mismatch effects among unit current (or capacitor) cells. Simulation results and discussions are provided for DAC linearity comparison in case that the proposed magic square and conventional algorithms are used.

INTRODUCTION

Recently, electronic devices such mobile phones, wireless modems and tablet terminators demand for small-sized, high-speed and high-linearity digital-to-analog converters (DACs). Especially, in the field of wireless communication, the accuracy (linearity) of the DAC is very important to ensure little interference leakage during transmission. Semiconductor devices on silicon wafer suffer from random and systematic mismatches regarding to characteristics of MOSFETs, resistors, and capacitors, which cause input and output relationships of the DAC to be non-linear.

In this paper we propose a unit cell sorting algorithm based on magic square calibration to cancel the random and systematic mismatch effects; magic square is a kind of a classical mathematics [1]. We have developed linearity improvement algorithm with one-time calibration by using “constant sum” characteristic of the magic square. We show its simulation results to demonstrate its effectiveness, and provide some considerations.

UNARY DAC ARCHITECTURE

A unary DAC employs a unary weighted (identical) current source structure (FIG.1). The unary weighted structure requires \(2^n-1\) unit current sources for \(N\)-bit resolution where all current source weights are identical as expressed in eq. (1):

\[
I_1 = I_2 = \cdots = I_{14} = I_{16} = I
\]

For the operation of the unary weighted structure, a binary-to-thermometer code decoder is required. The unary DAC has characteristics of small glitch and inherent monotonicity. But this architecture suffers from large decoder circuits and many switches which increase silicon chip area.

DAC NONLINEARITY

In practical CMOS technologies, the current source mismatches are influenced by their threshold voltage mismatch and/or by the slope mismatch (FIG.2). Ideal drain current \(I_d\) in saturation region is given by

\[
I_{d,1} = \frac{\beta}{2} \left( V_{gs} - V_{th} \right)^2
\]

Also drain current mismatch is given by

\[
\frac{\Delta I_{d1}}{I_{d1}} = \frac{2}{V_{gs} - V_{th}} \frac{\Delta V_{th}}{V_{th}} \frac{\Delta I_{ox}}{I_{ox}} \sqrt{\frac{WL}{L}} \]

Current mismatches are dependent on their device sizes. Note that here, we are considering to reduce the DAC nonlinearity effects of the current mismatches due to small device size \(\sqrt{WL}\).

FIG 1. Unary DAC.

FIG 2. Mismatches among current sources.
MAGIC SQUARE

Characteristic of the magic square is a constant sum of each row, column and diagonal [1]. We consider that this characteristic is good balance for unit cell arrange sorting for DAC linearity improvement by cancelling random and systematic mismatch effects among unit cells. We propose a unary DAC linearity improvement algorithm by using magic square.

Now we explain about the magic square. Magic square is a square matrix where different integers are arranged to begin with 1 into n×n. Furthermore, each row, column, and diagonal have the same sum. Generally, we call the n×n magic square matrix as an n-class magic square. Constant sum of the n-class magic square is expressed as follows:

\[ S = \frac{n(n^2 + 1)}{2} \] (4)

We show a 3×3 magic square in Fig.3, and there we can confirm its constant sum characteristics.

DIGITAL CALIBRATION ALGORITHM

In this section, we propose a digital calibration algorithm based on magic square for the unary current-steering DAC [2-5]. We aim one-time calibration; the new digital algorithm can improve the linearity of the DAC recovering from the effect of the current source mismatches. At the same time, the optimized switching sequence can suppress the distortion especially caused by 2nd and 3rd order harmonics for better dynamic performance. This section discusses the essence of the proposed digital algorithm as well as calibration technique (Fig.4).

Note the current measurement circuit only needs to measure the order of the current sources and does not need their accurate value measurement. The measurement circuit can be simply designed as a ring-oscillator-based circuit [3][7].

1. Current Source Sorting Based on Magic Square

We use a 4-bit unary DAC as an example to explain the proposed algorithm.

① Assume the initial condition of current sources after fabrication

② Then, 16 available current source cells are sorted by their values (Fig.4①)

③ The order of the current source values and the magic square algorithm are adopted. For example, the smallest current source (I_5) is adopted to “1” cell in the magic square. The second small current source (I_15) is adopted “2” cell in the magic square. Hence, n-th current source (I_n) is adopted “n” cell in magic square (Fig.4②).

④ A current source cell corresponding to the magic square according to the constant sum, turns on corresponding to the digital input to obtain the DAC analog output value (Fig.4③).

We can cancel the random and systematic mismatches by sorting current sources according to constant sum characteristics. We focus on array of the magic square. In Fig.4 ③ of the magic square, we see at the first column that the sums of adjacent two numbers is almost equal (16 for 1, 15 and 18 for 14, 4)). We understand that they are almost the same. It is similar in other lines. Sorting current sources according to constant sum is based on an algorithm to perform switching of current sources with large mismatch and small mismatch to turn on, and we can cancel mismatch effects. In Fig.5, we show look-up table (LUT) of the conventional method of a thermometer-code decoder, and the proposed method of a magic square switching-code decoder.
2. Calibration Technique

We consider here a calibration technique with the error measurement approach to meet with our proposed techniques (Fig.6). Our proposed calibration steps are as follows:

① Input test codes are inserted by central processing unit (CPU) that controls the digital calibration circuit. Digital calibration circuit utilizes ring oscillator-based measurement circuit [3].

② By implementing current measurement circuit, current source cell values are measured.

③ All measured values are sorted in memory.

④ Then, these data are fed into digital calibration circuit to perform main calibration process.

⑤ Finally, the optimized switching sequence based on magic square is stored in memory.

The optimized switching sequence is used during DA conversion.

![Diagram of DAC nonlinearity calibration algorithm.](image)

FIG.6 DAC nonlinearity calibration algorithm.

SIMULATION RESULT

We have simulated static and dynamic performances of an 8-bit unary DAC. We have compared the conventional method of the thermometer-code decoder and the proposed current source sorting algorithm based on magic square. The static performance was simulated as INL and DNL. The simulated dynamic performance was obtained as SFDR. In Fig.7, we show the magic square used for the 8-bit unary DAC calibration. The magic square was obtained by MATLAB. Mismatch of current sources was generated as a random number between -1 from +1. We show the simulation results in Fig.8-11.

1. Static Performance

In order to verify the simulated linearity of the proposed DAC, the static performance parameters, INL and DNL have been obtained. The simulation result shows that INL of 7.63 LSB before calibration has been improved to 1.95 LSB using the proposed calibration technique (Fig.8), and also DNL has been improved (Fig.9). We note that INL and DNL are nearly 0.0 in the center of input range \(D_{in} (=122)\).

2. Dynamic Performance

In the frequency domain, the conventional method using the thermometer-code decoder unary 8-bit DAC shows the SFDR performance of 14.8 dB (Fig.10). Our proposed calibration technique of current source cell sorting based on magic square obtains SFDR of 22.0dB (Fig.11), and we see that 7dB improvement of the DAC SFDR using the proposed method is obtained.
CONCLUSION

We have proposed a current source cell sorting algorithm based on magic square for unary DAC linearity improvement. The technique improves INL, and also DNL in the center of the input range. The better SFDR can be obtained with second and third harmonics suppression. The current measurement circuit only needs to measure the order of the current sources and does not need their accurate value measurement. It can cancel random and systematic mismatch effects of current sources by sorting current sources using the constant sum property of the magic square. We have shown in simulation that our proposed algorithm could improve static and dynamic performance with one calibration.

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REFERENCES