Study of R-2R DAC and Gray Code Input DAC for Glitch Reduction

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Outline

- Research Objective
- Introduction to DAC
- Voltage Mode R-2R DAC
- Current Mode R-2R DAC
- Glitches
- Gray Code vs. Binary Code
- Gray Code Input DAC
  - Design of Switch
  - Voltage Mode Gray Code Input DAC
  - Current Steering Mode Gray Code Input DAC
- Conclusion

Research Objective

- ✓Transistor level implementation of R-2R DACs
- ✓Transistor level implementation of Gray code input DAC for glitch reduction

  *(difficult to design)

Approach

- ✓Use MOSFETs to design DACs
- ✓Utilization of Gray code input for glitch reduction

Introduction to DAC (1/2)

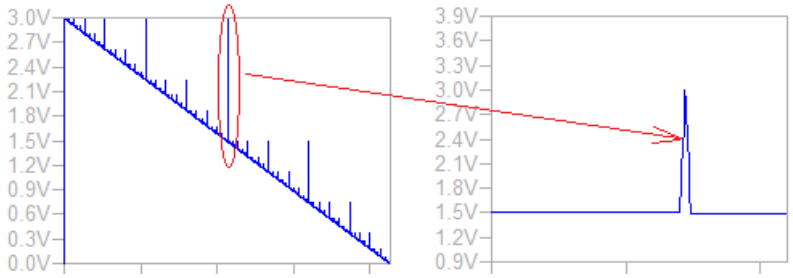
- Convert digital signal to analog

- Signal to be recognized by human senses
- Widely used in signal processing

DAC: Digital-to-Analog Converter

Introduction to DAC (2/2)

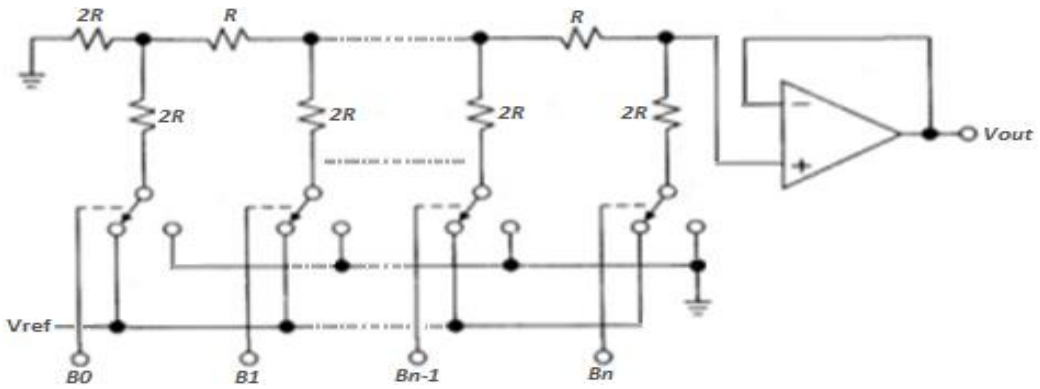
- R-2R ladder DAC is very popular.
  - Easy to design and use
  - Less components
- Vulnerable to glitches (voltage spikes)



- Types : Voltage mode DAC, Current mode DAC

Voltage Mode R-2R DAC

- R-2R DACs consist of:
  - ✓R, 2R resistors
  - ✓N Switches
  - ✓OPAMP
- Structure



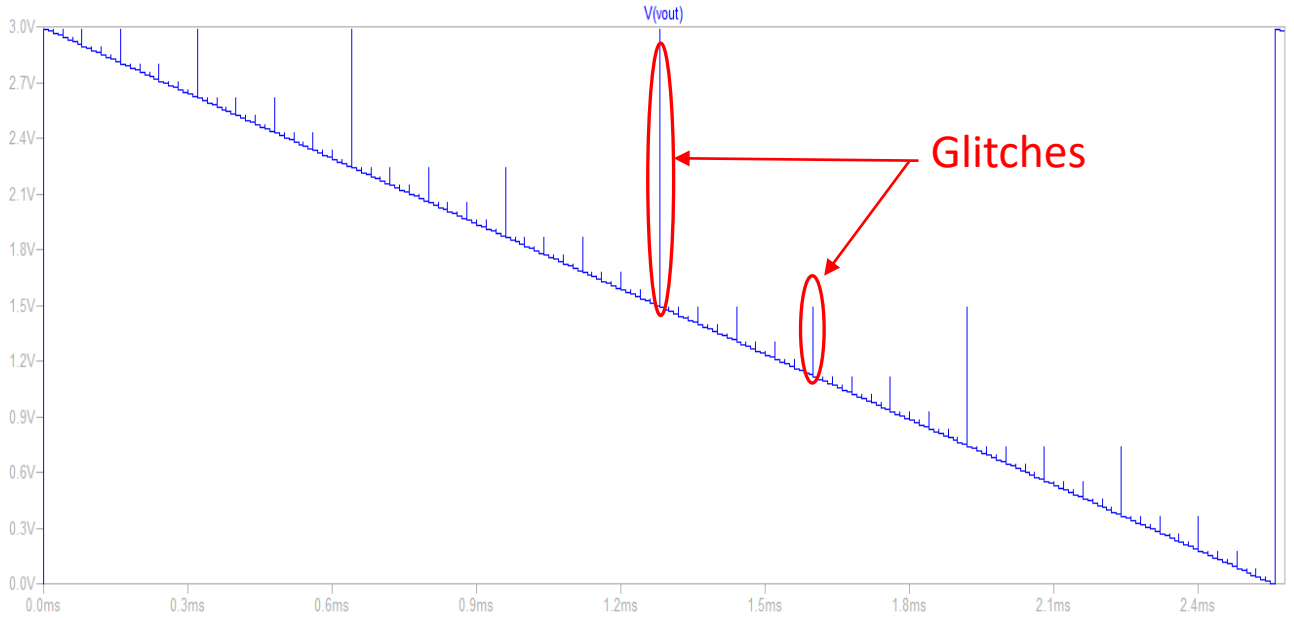
- Digital input → each resistor switched to ground or to OPAMP.
- Output voltage
- $Vout = \frac{Vref}{2} b_{n-1} + \frac{Vref}{2^2} b_{n-2} + \cdots + \frac{Vref}{2^{n-1}} b_1 + \frac{Vref}{2^n} b_0$

Digital Inputs	Output
0000	0
0001	0.1875
0010	0.375
0011	0.5625
0100	0.75
0101	0.9375
0110	1.125
0111	1.3125
1000	1.5
1001	1.6875
1010	1.875
1011	2.0625
1100	2.25
1101	2.4375
1110	2.625
1111	2.8125

Simulation Results of Voltage Mode R-2R DAC

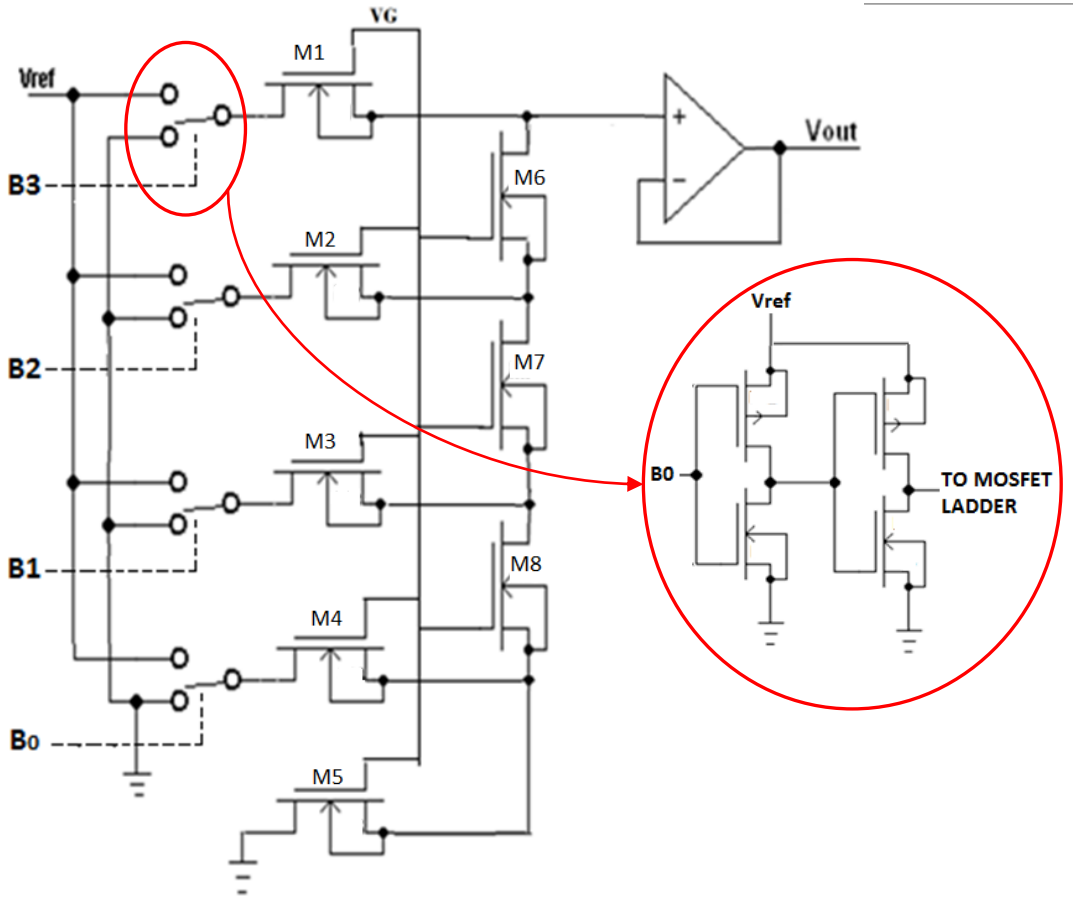
4-bit case

8-bit case



R=10k, 2R=20k, Vref=3V

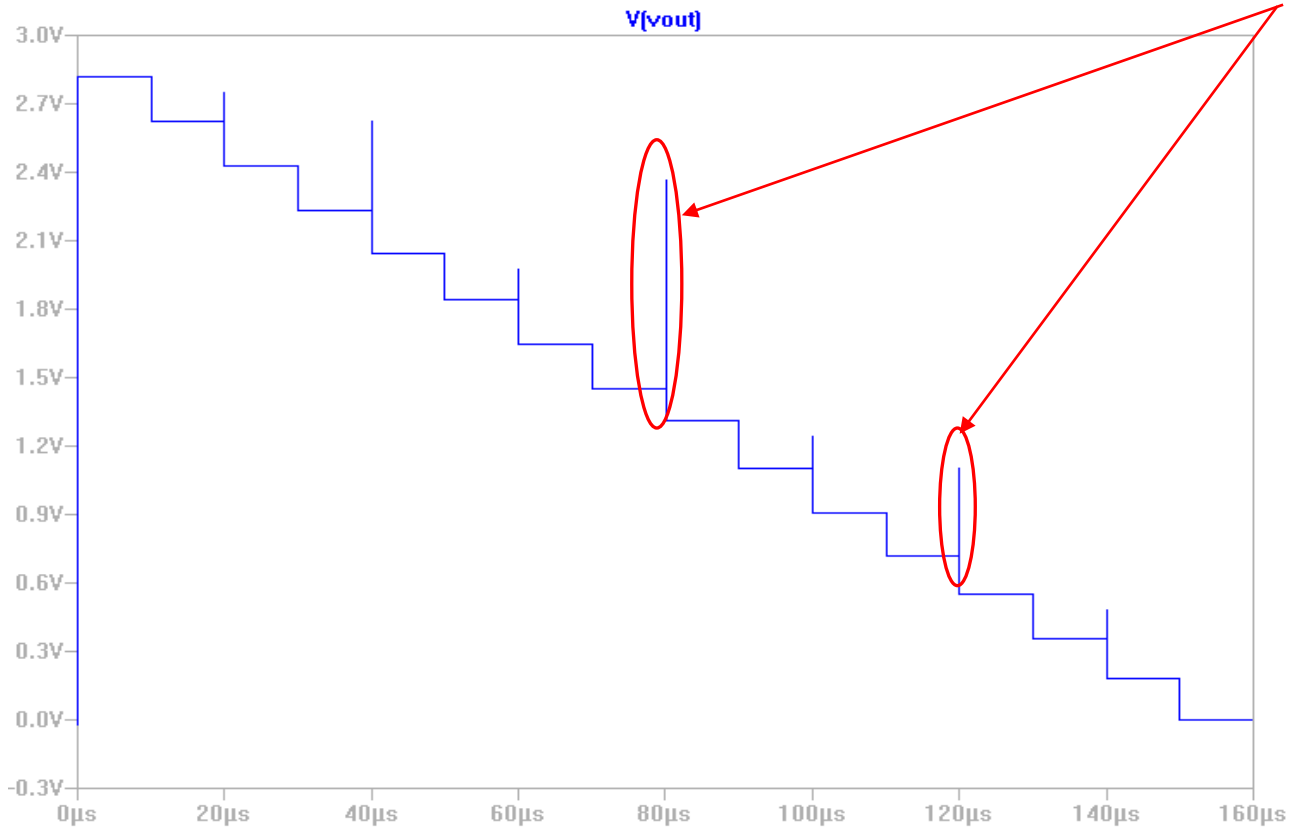
MOSFET Implementation of Voltage Mode R-2R DAC



- Switch is SPST (Single-Pole Single-Throw)
- Switches implementation
  → Two cascaded inverters
- W/L for R , 2R is calculated using
- $R, 2R = \frac{V_{DS}}{Id_{SAT}} = \frac{V_{DS}}{\frac{u_n C_{ox}}{2} \times \left(\frac{W}{L}\right) \times (V_{GS} - V_{TH})^2}$

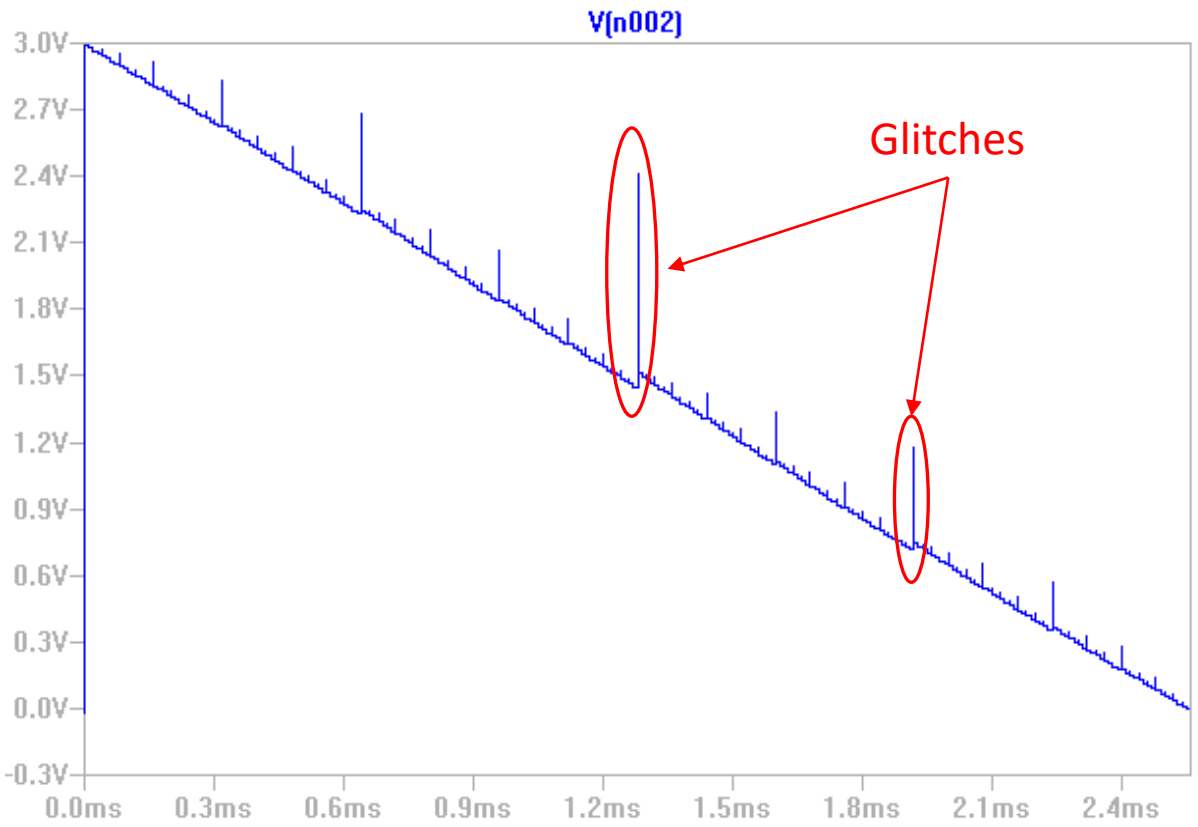
Simulation Results Of Voltage Mode R-2R DAC (MOSFET Implementation)

4-bit case



Glitches

8-bit case



Glitches

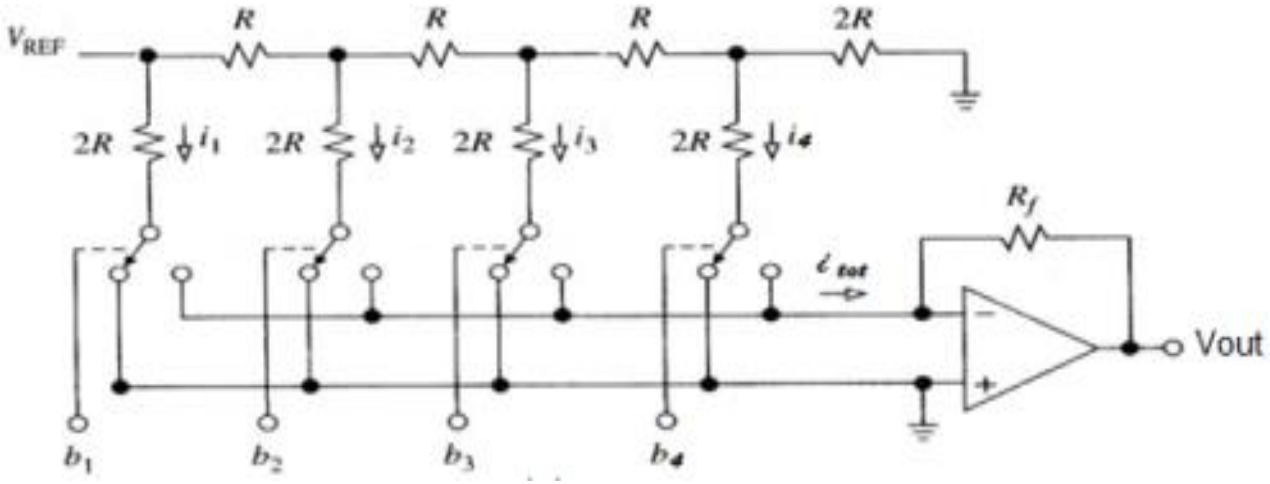
W/L=3.81u/2.1u for R, 2R=7.61u/2.1 for 2R, Vref=3V

Current Mode R-2R DAC

- Currents through 2R resistors → Binary weight relationship
- *I* through 2R → diverted either to OPAMP or ground
- Output voltage

$$Vout = -i_{tot} \times Rf$$

Here $i_{tot} = \sum_{K=0}^{N-1} \frac{B_K \times Vref}{2^{N-K}} \times \frac{1}{2R}$

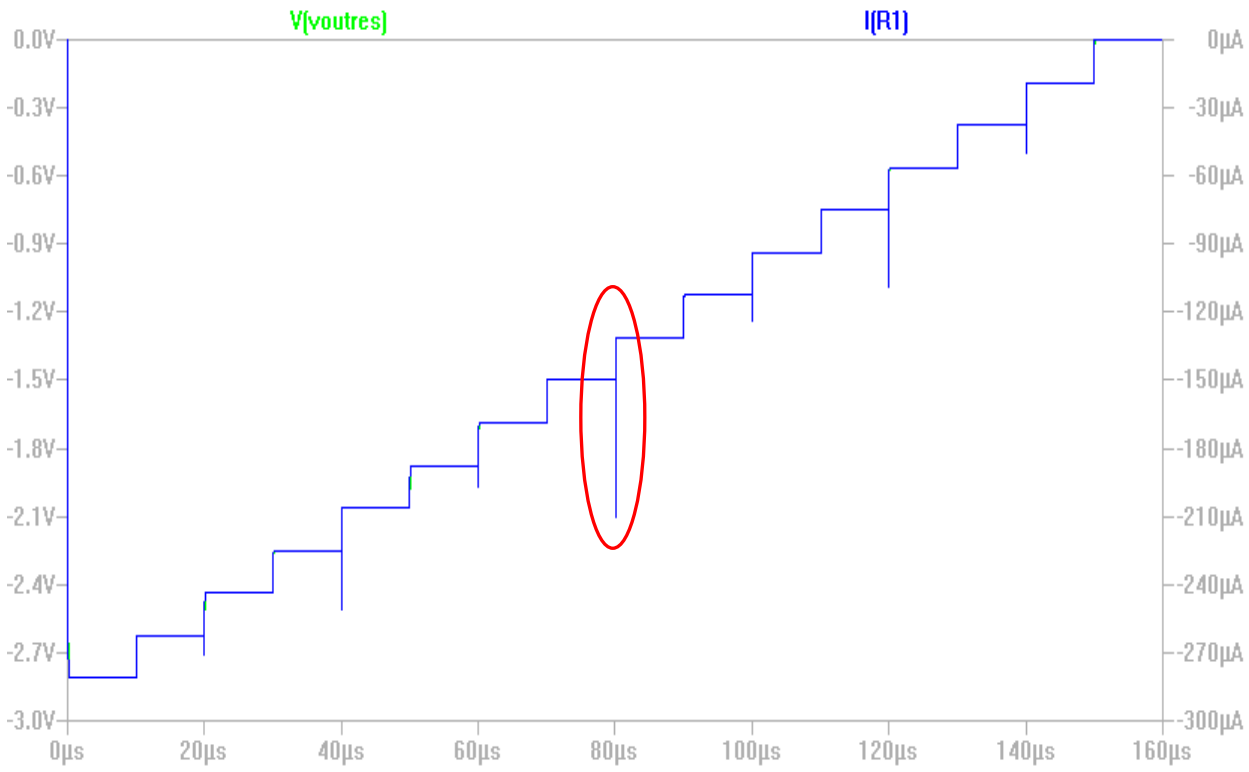


4-bit DAC output

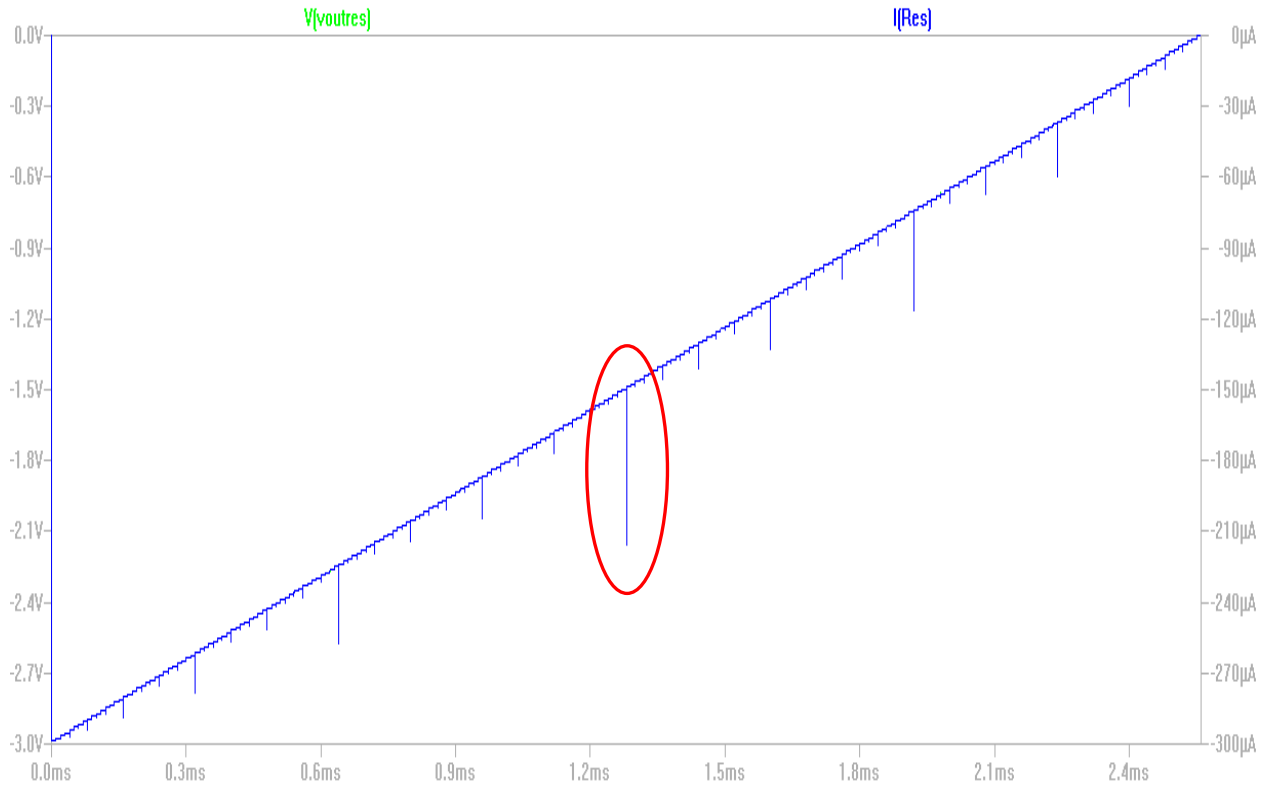
Decimal	Output
0	0
1	0.1875
2	0.375
3	0.5625
4	0.75
5	0.9375
6	1.125
7	1.3125
8	1.5
9	1.6875
10	1.875
11	2.0625
12	2.25
13	2.4375
14	2.625
15	2.8125

Simulation Results of Current Mode R-2R DAC

4-bit case

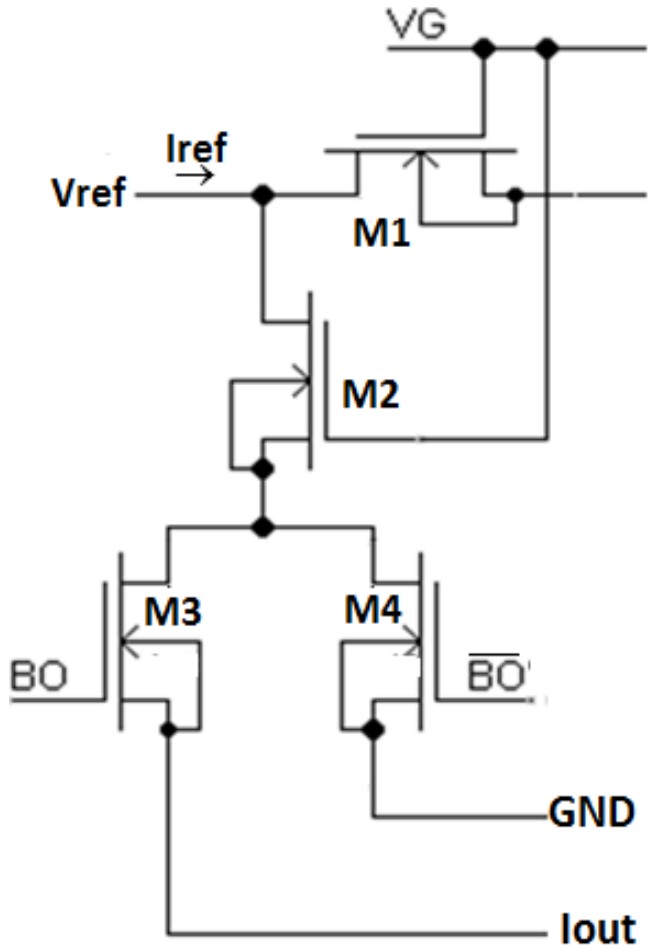


8-bit case



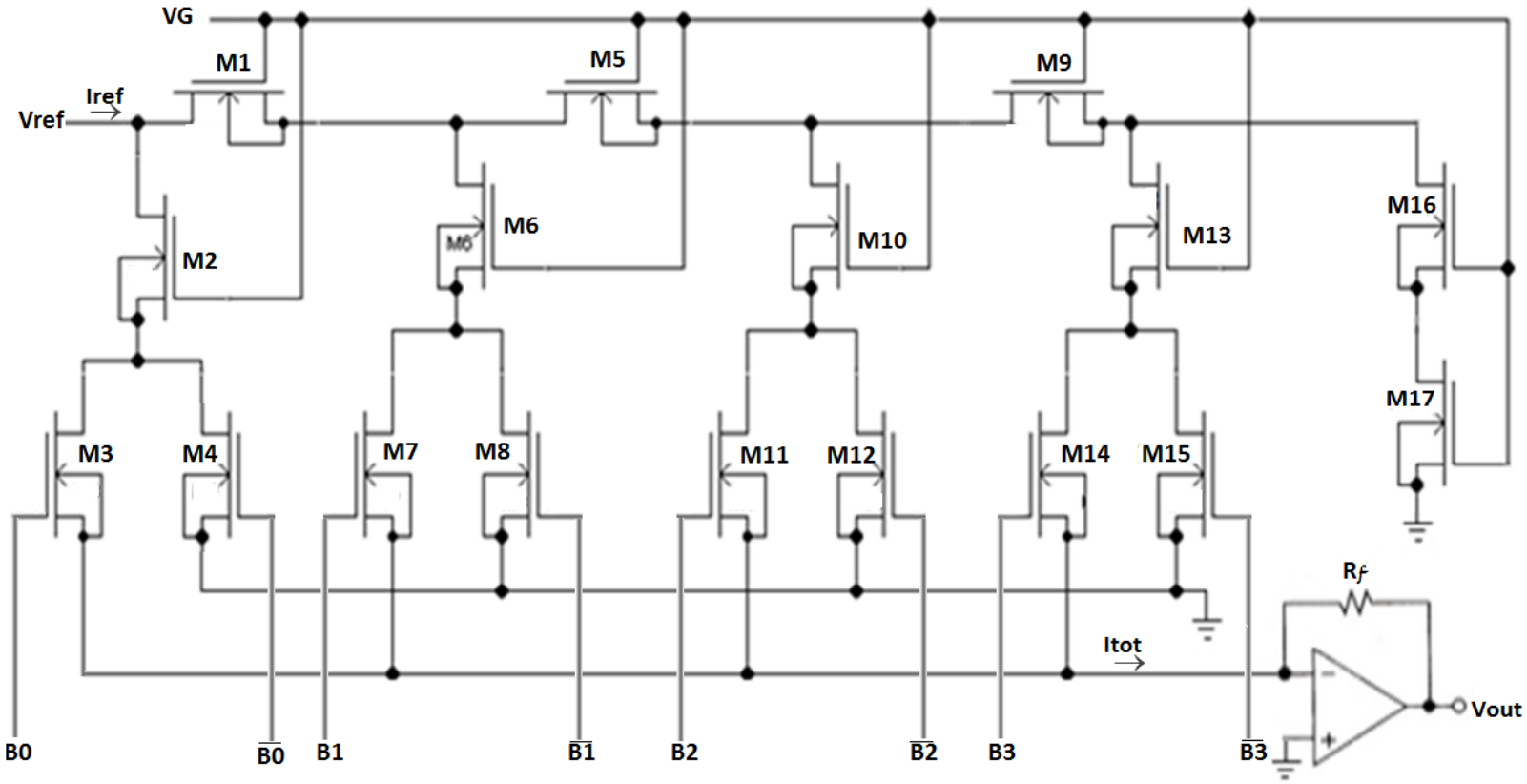
MOSFET Implementation of Current Mode R-2R DAC (1/2)

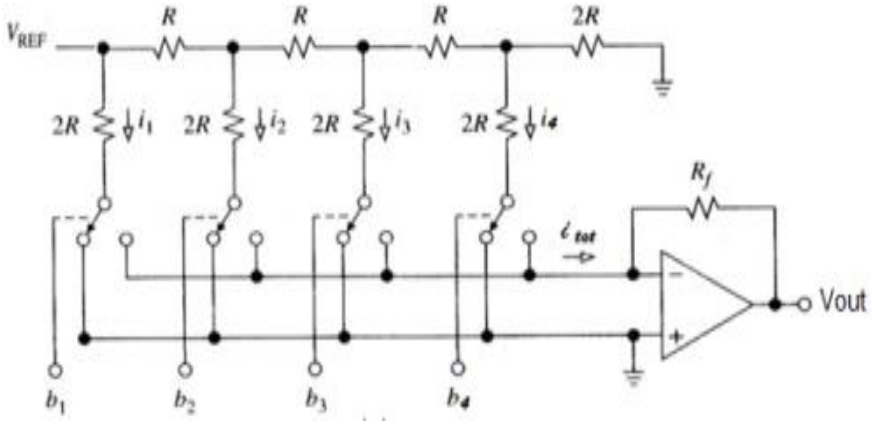
- M1 forms R
- M2 + M3 or M2+M4 forms 2R
- $I_{ref} \rightarrow$ divided to M1, M2.
- Current through M2 $\rightarrow$
  Switched to I_{out} by M3 or ground by M4
- Full resolution $\rightarrow$ Cascade this cell.
- $R = \frac{V_{DS}}{Id_{SAT}} = \frac{V_{DS}}{\frac{u_n C_{ox}}{2} \times \left(\frac{W}{L}\right) \times (V_{GS} - V_{TH})^2}$



MOSFET Implementation of Current Mode R-2R DAC (2/2)

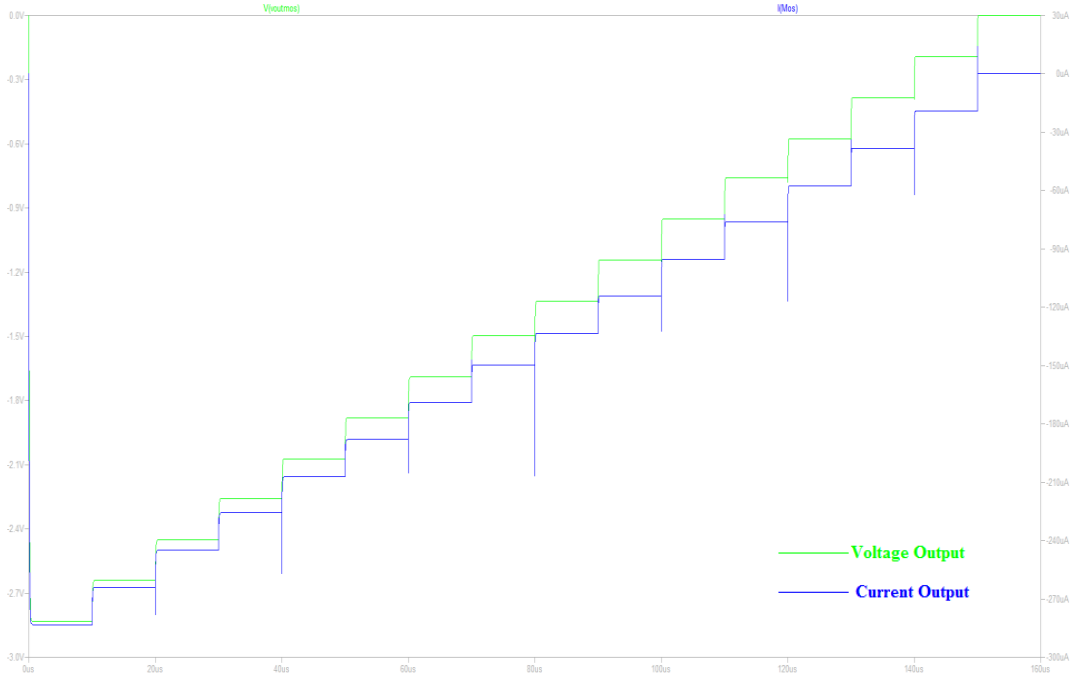
M16 , M17 form terminal 2R resistor



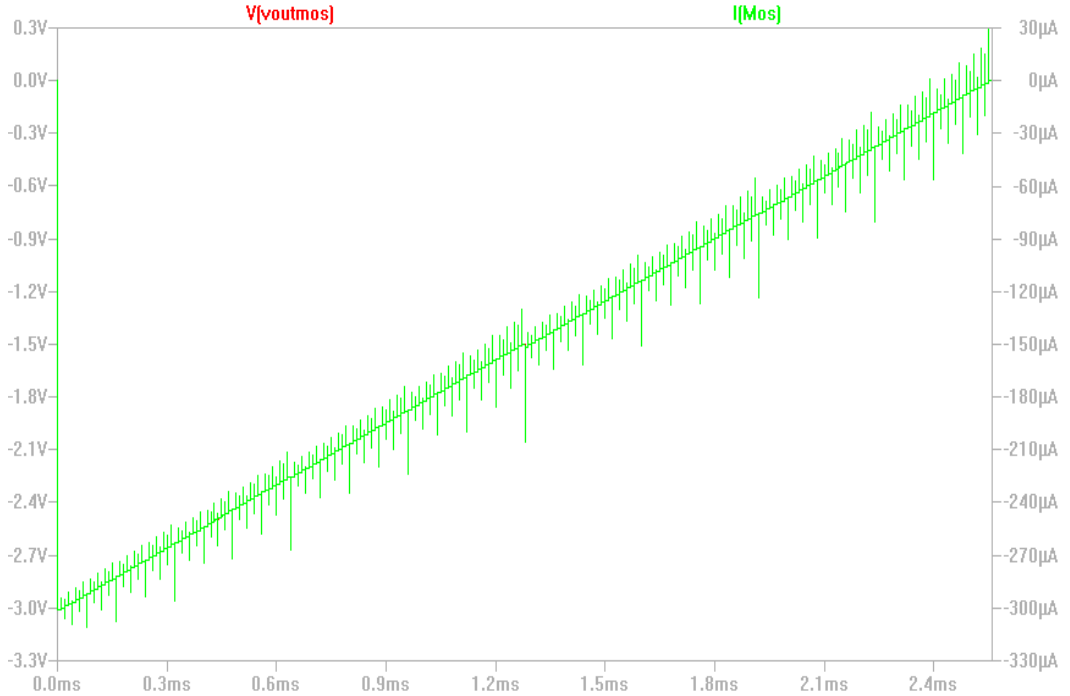


Simulation Results of MOSFET Implementation of Current Mode R-2R DAC

4-bit case

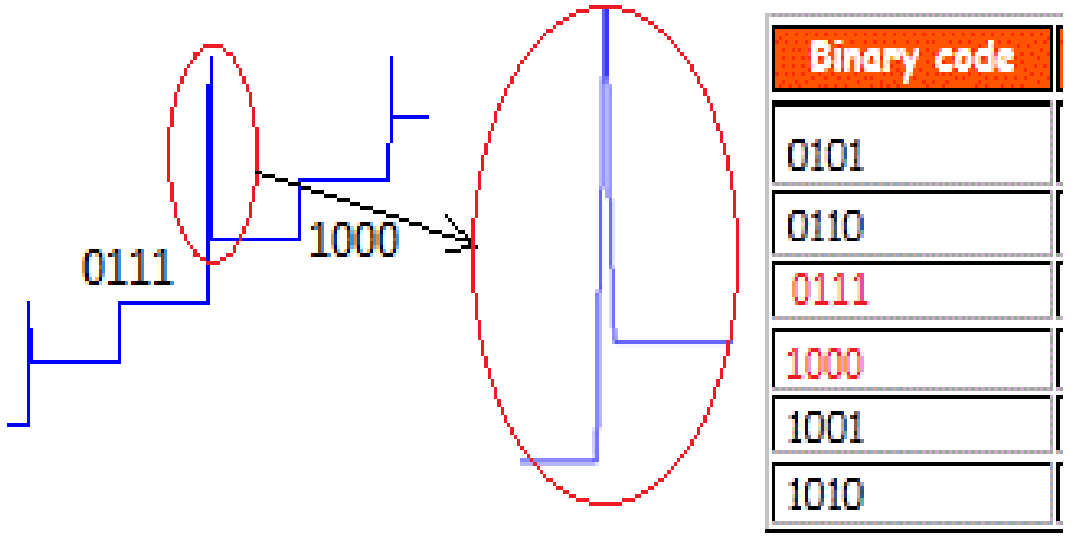


8-bit case



Glitches (1/2)

- ✓Voltage spikes
- ✓Reasons for glitch
  - Capacitive coupling
  - Differences in Switching



- ➢Glitch behavior → Dominated by difference in switching
- ➢Switching of MSB → Most significant glitches

(Some switches change from ON to OFF, others from OFF to ON at once)

Glitches (2/2)

Effects of glitch

- Serious deterioration of images, videos, sounds

Remedy

- High-order reconstruction filter usage
- Track/Hold circuitry usage at output.

} Extra Space in IC, Expensive

- Using Gray code input DAC topologies ✓

Gray Code vs. Binary Code

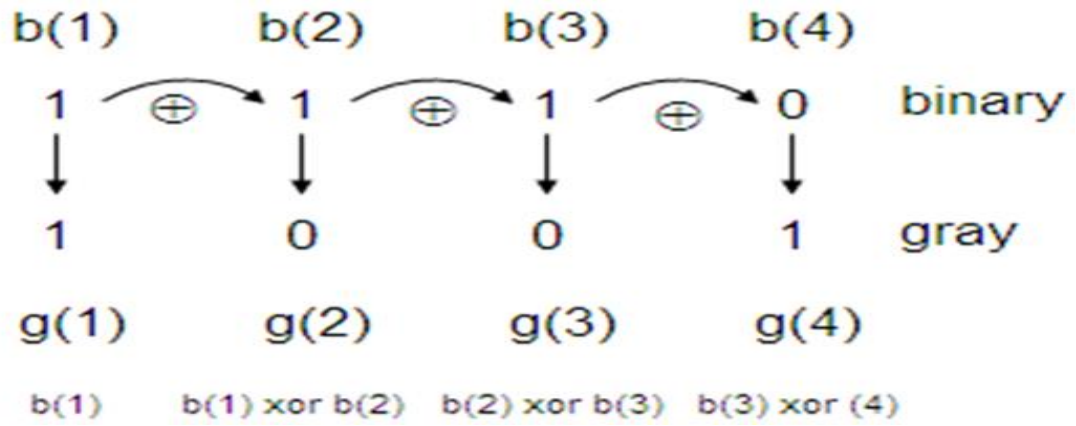
Binary Code Multiple bits change for 1-LSB change

Trigger more switches

Gray Code Only one bit changes for 1-LSB change

Trigger one switch

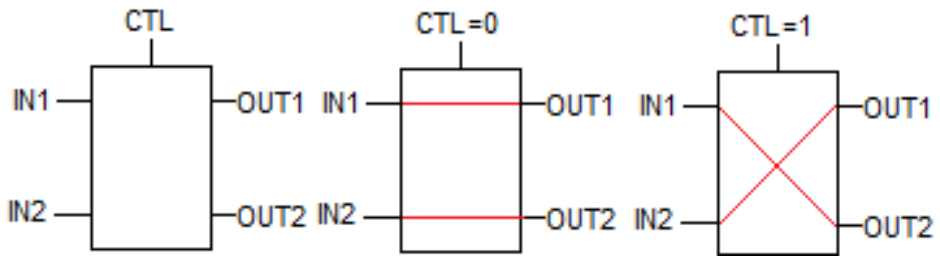
Less glitches

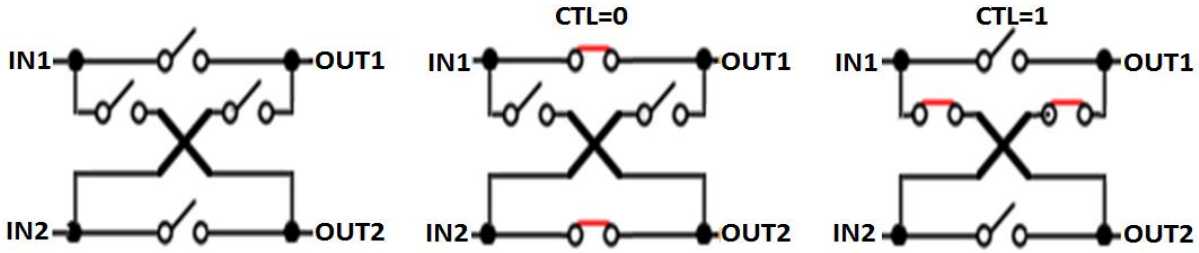


Decimal	Binary	Gray
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

Gray Code Input DAC

Design of Switch(1/2)





Switch is DPDT (Double-Pole Double-Throw)

CTL → LOW:

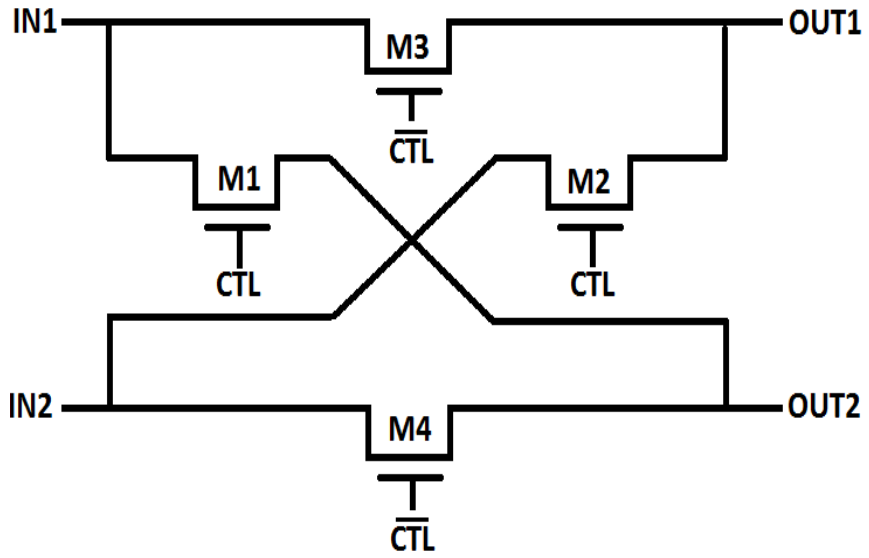
M3 , M4 → ON, M1, M2 → OFF

IN1 = OUT1, IN2 = OUT2

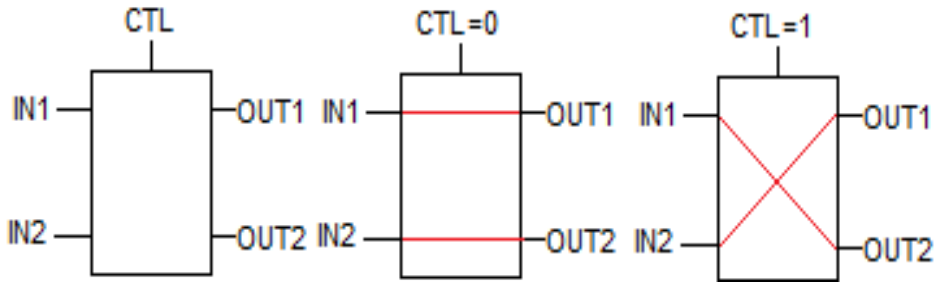
CTL → HIGH:

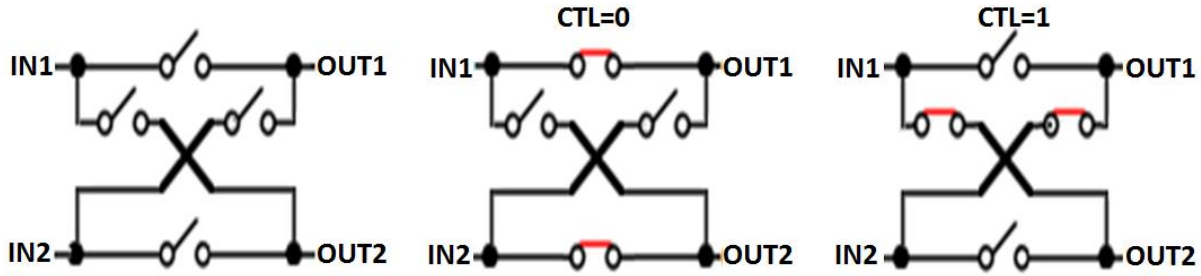
M1, M2 → ON, M3, M4 → OFF

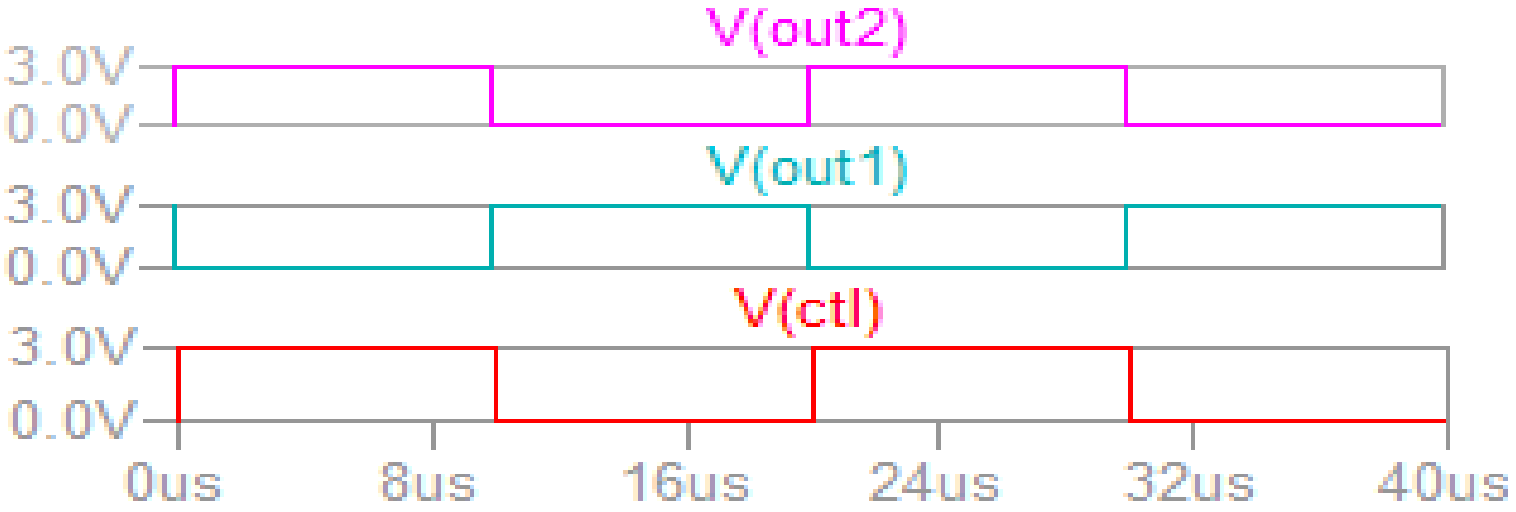
IN1 = Out2 , IN2 =OUT2

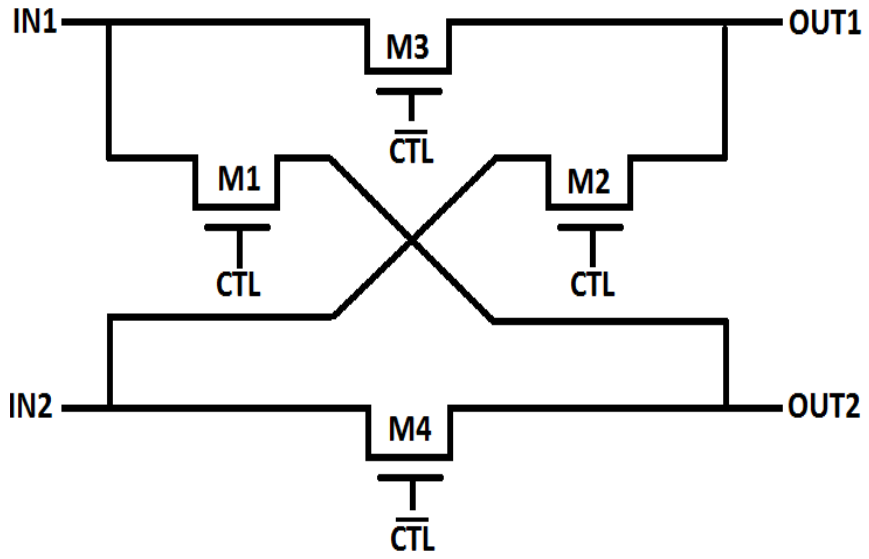


Design of Switch (2/2)



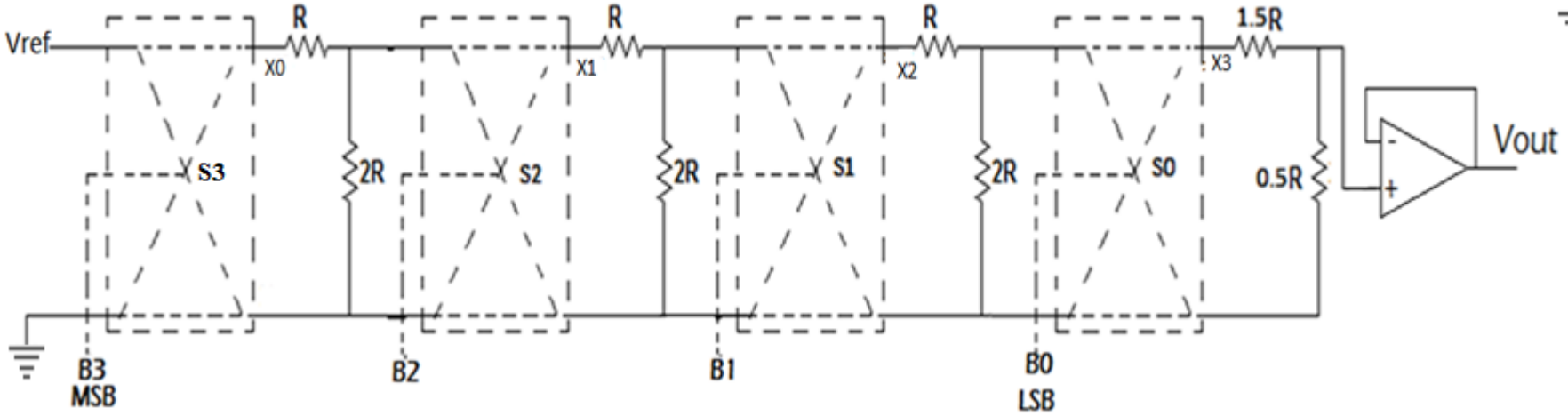


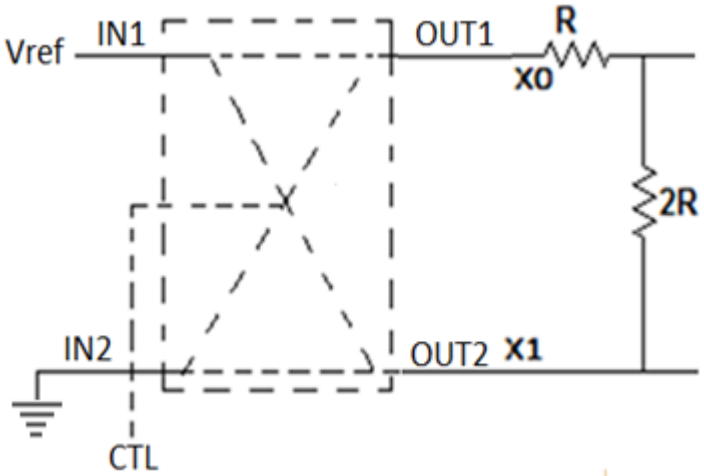




Voltage Mode Gray Code Input DAC

- IN1 = Vref
- IN2 = 0
- CTL ← Gray code input
- OUT1, OUT2 → Connected with R-2R Ladder





$$Vout(D) = \frac{Vref}{2^{n+1}} |(2D - 1)|$$

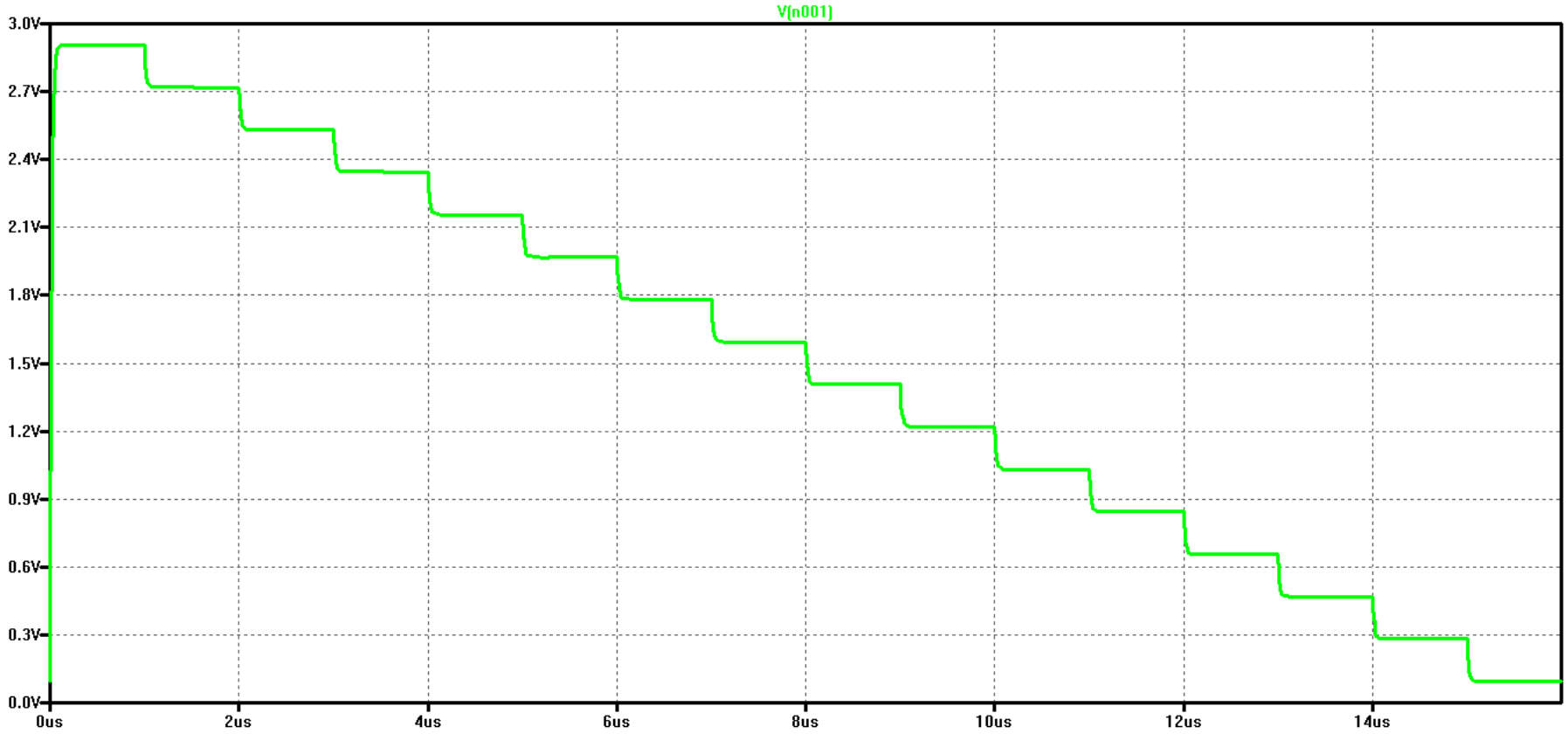
n : number of bits

D =1, 2, 3...n+1

- Final stage → terminated with 1.5R, 0.5R resistors.

Voltage Mode Gray Code Input DAC Simulation Results

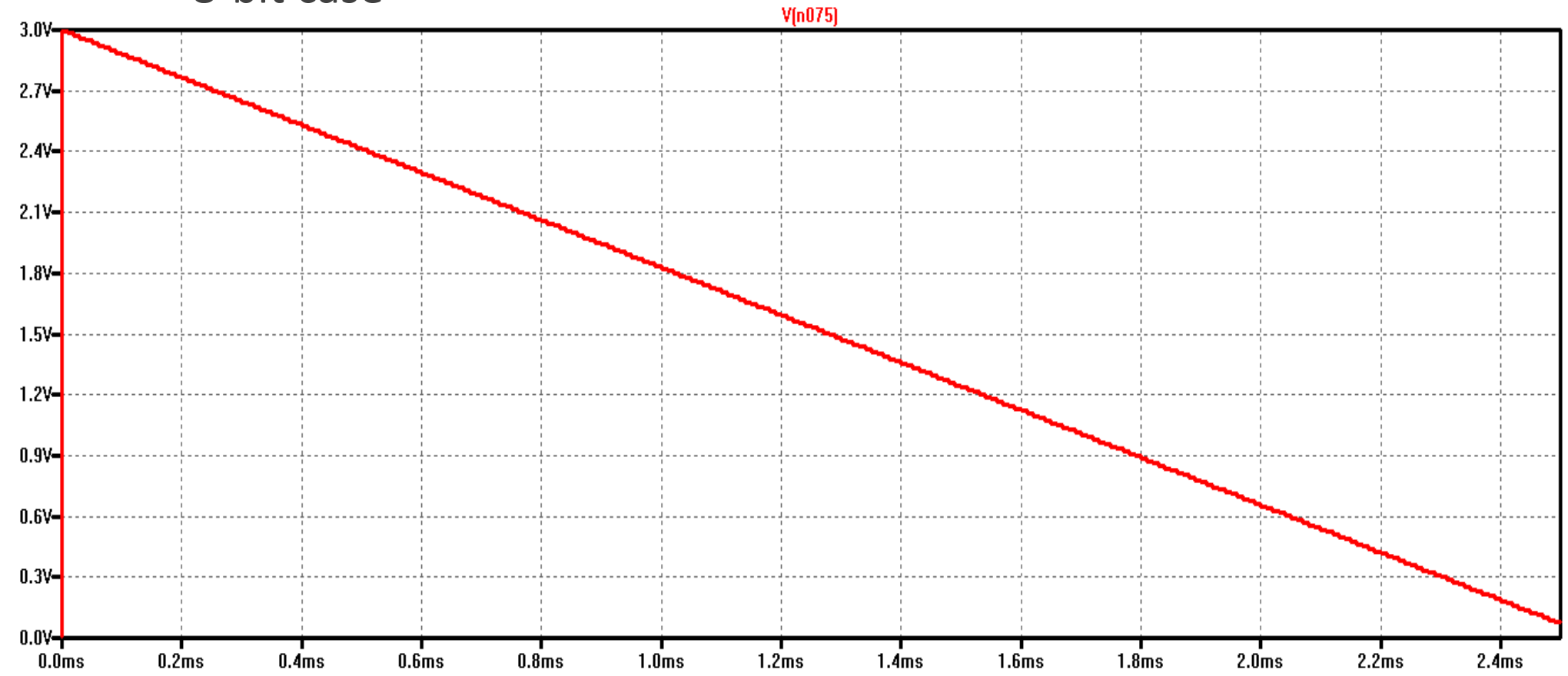
4-bit case



Bits	X0	X1	X2	X3	Vout
0000	1	½	¼	1/8	1/32
0001	1	½	¼	3/32	3/32
0011	1	½	0	¼	5/32
0010	1	½	0	1/8	7/32
0110	1	0	½	3/8	9/32
0111	1	0	½	¼	11/32
0101	1	0	¼	½	13/52
0100	1	0	¼	3/8	15/32
1100	0	1	6/8	5/8	17/32
1101	0	1	6/8	1/2	19/32
1111	0	1	½	6/8	21/32
1110	0	1	½	5/8	23/32
1010	0	½	1	7/8	25/32
1011	0	½	1	6/8	27/32
1001	0	½	6/8	1	29/32
1000	0	½	6/8	7/8	31/32

Voltage Mode Gray Code Input DAC Simulation Results

8-bit case

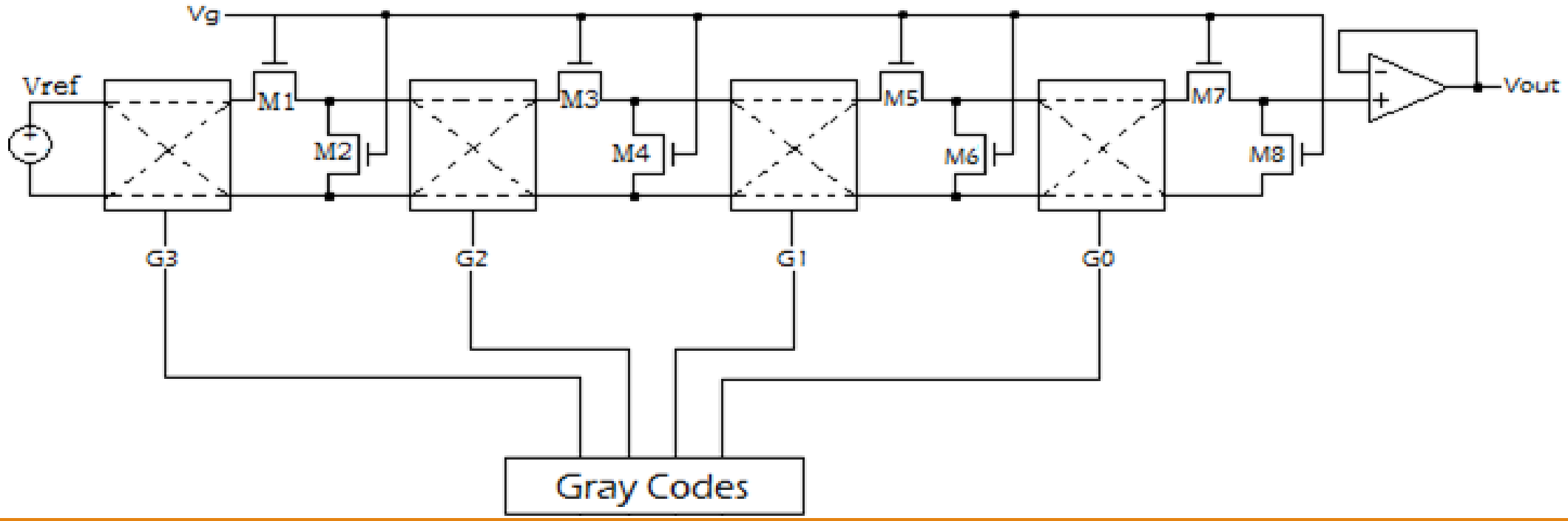


NO GLITCHES

Voltage Mode Gray Code Input DAC MOSFET Implementation

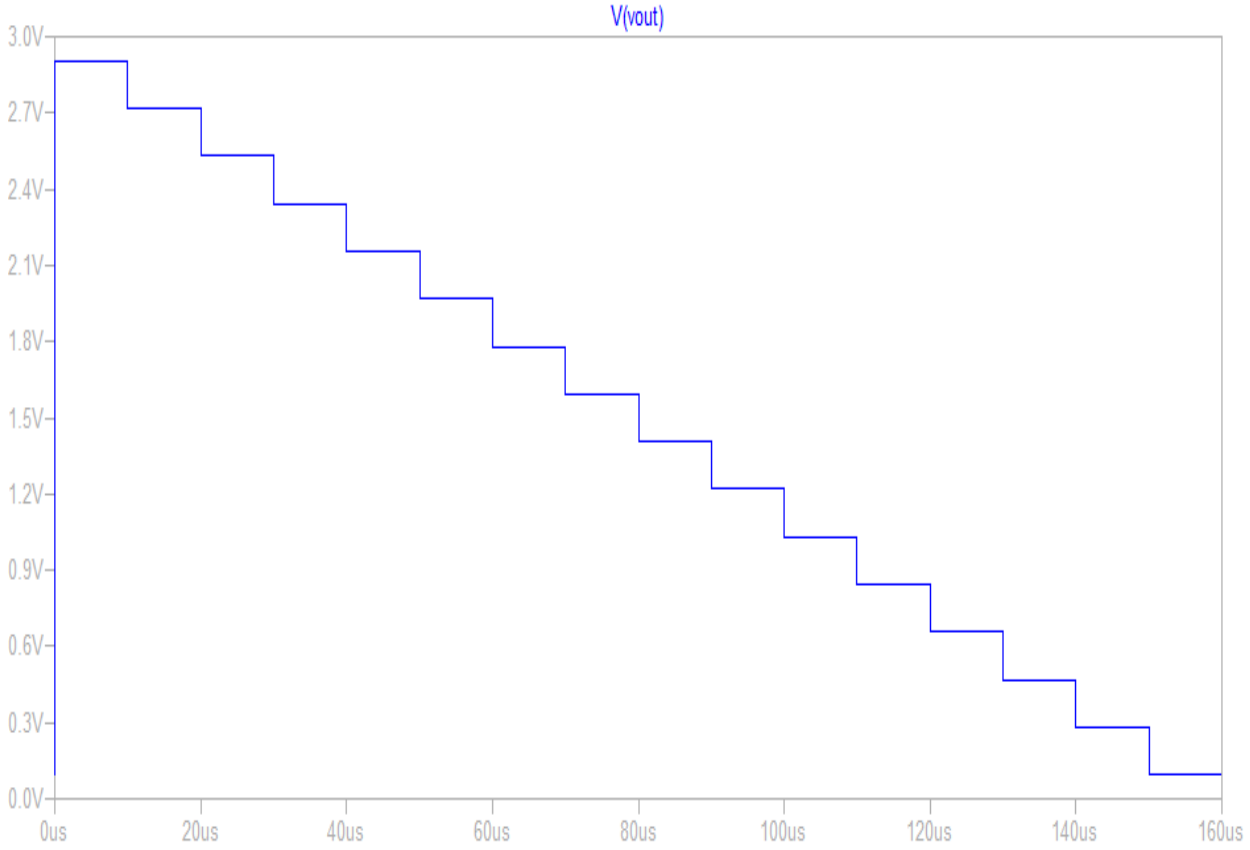
Aspect ratios W/L for R, 2R, 1.5R, 0.5R

$$R = \frac{V_{DS}}{Id_{sat}} = \frac{V_{DS}}{\frac{u_n C_{ox}}{2} \times \left(\frac{W}{L}\right) \times (V_{GS} - V_{TH})^2}$$

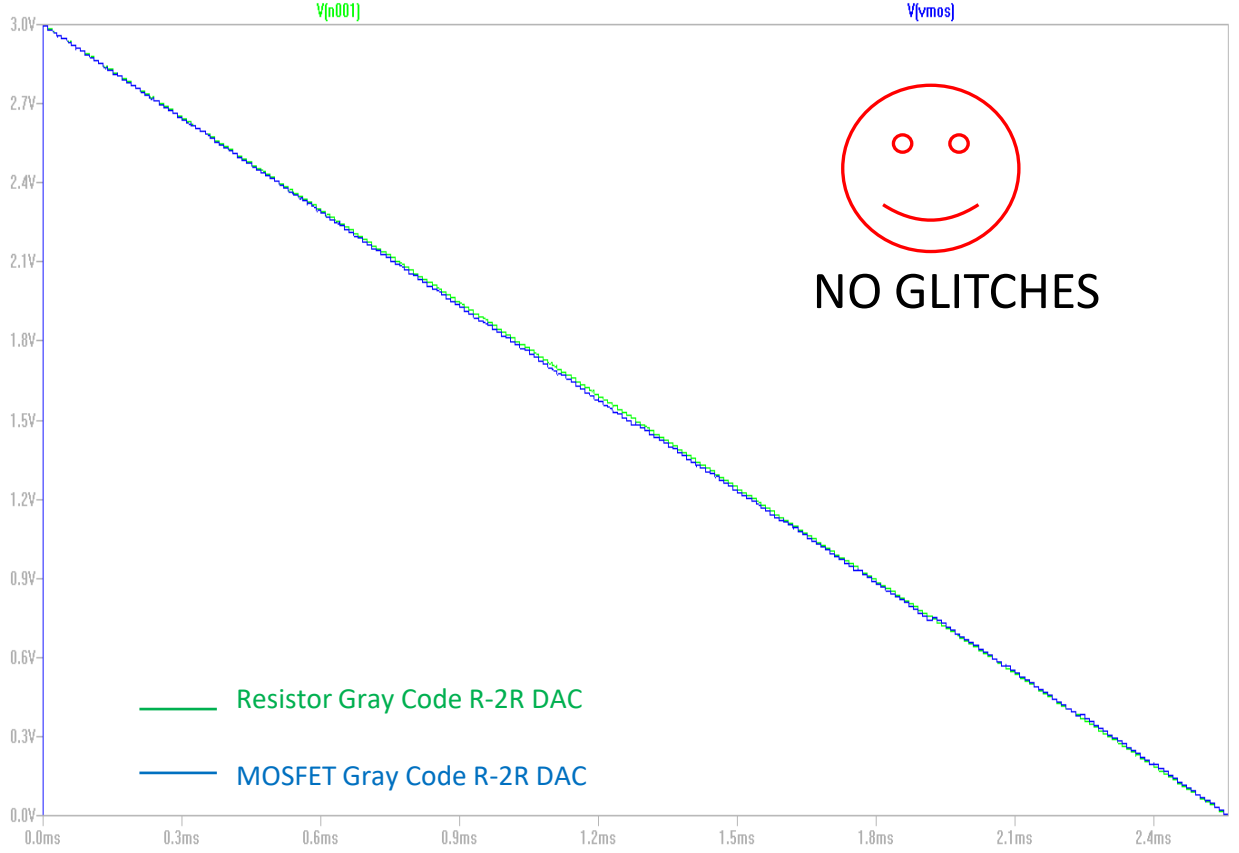


Voltage Mode Gray Code Input DAC MOSFET Implementation Simulation Results

4-bit case

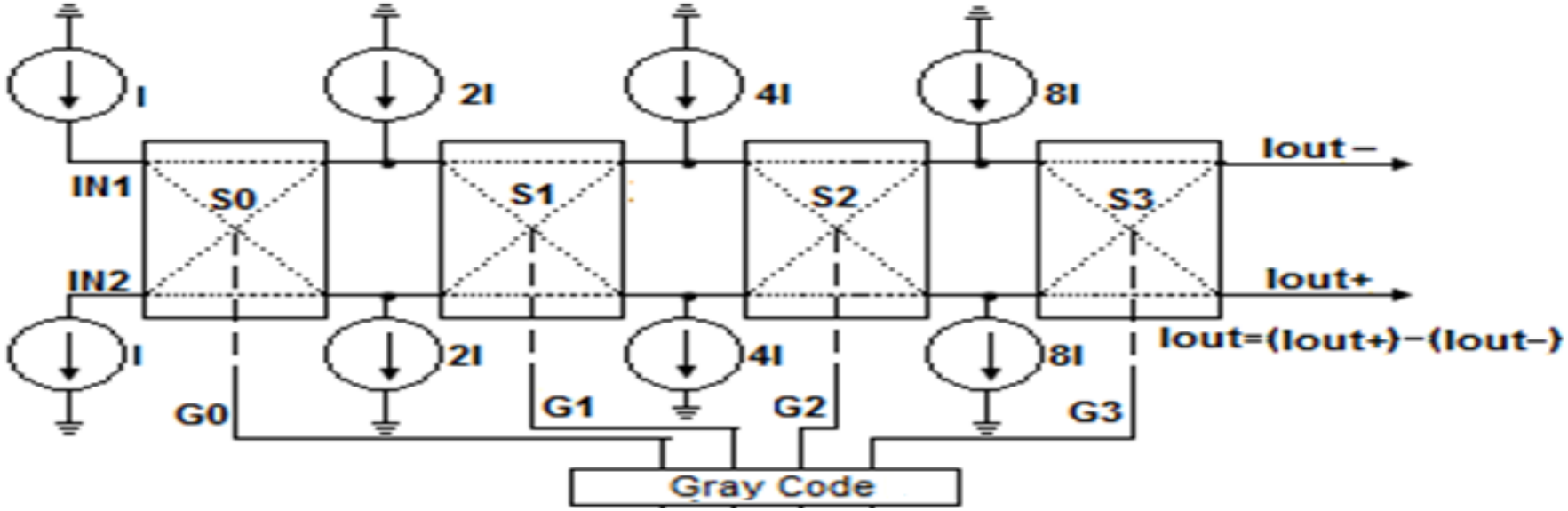


8-bit case



Current Steering Mode Gray Code Input DAC (1/2)

- IN1, IN2, intermediate stages →binary weighted current sources.
- Gray code alters the way the switches are triggered
- Iout=Iout+ – Iout –



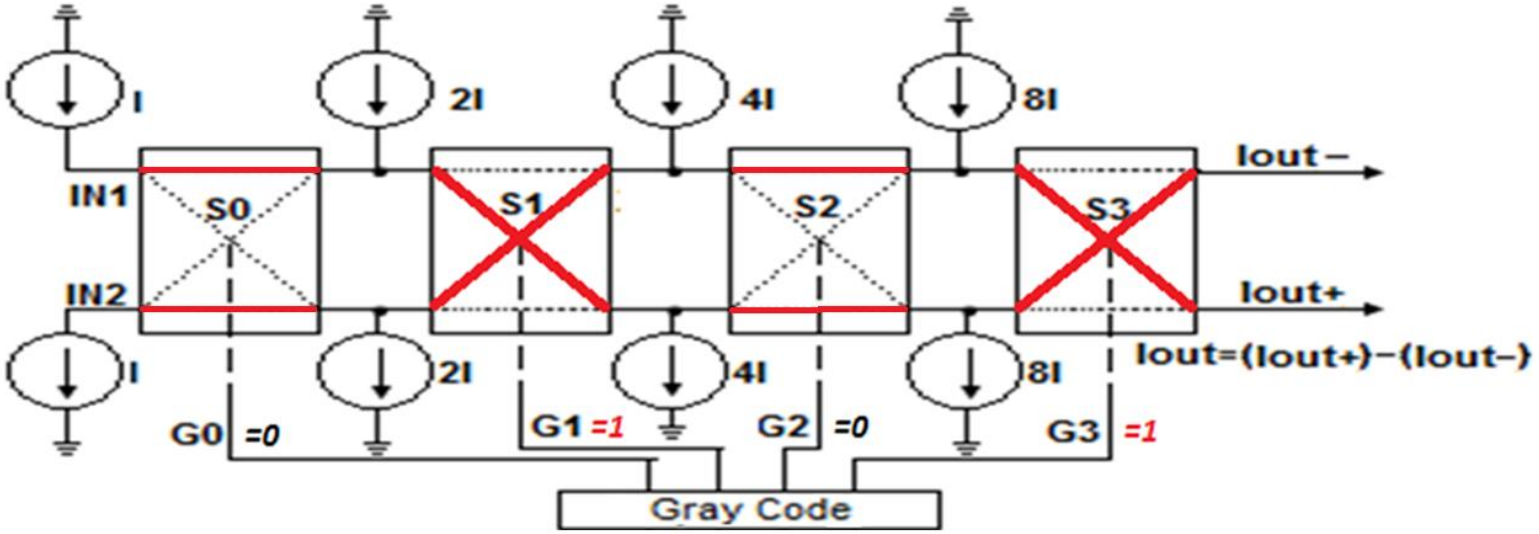
Current Steering Mode Gray Code Input DAC(2/2)

For 1010 Gray code,

S3, S1 $\rightarrow$ ON, the other switches $\rightarrow$ OFF

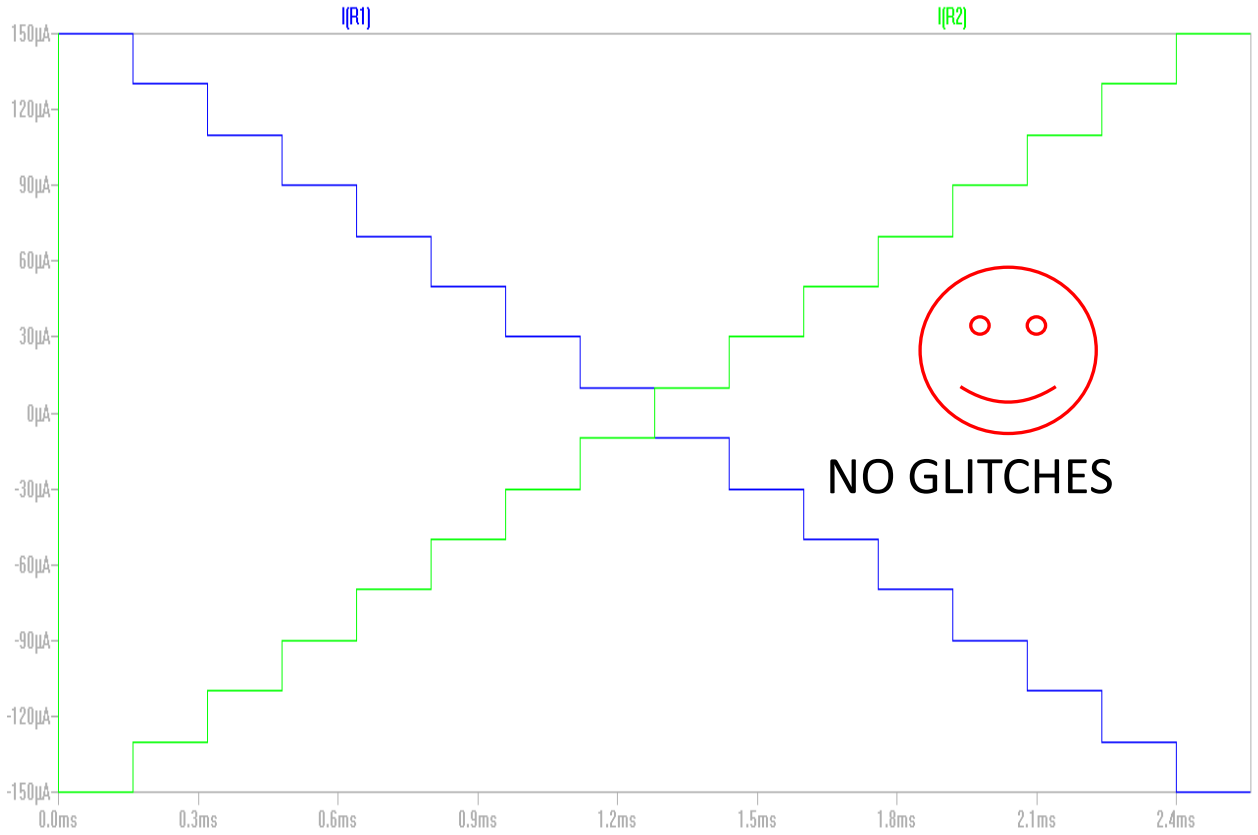
$$Iout -= I + 2I - 4I - 8I = -9I$$

$$Iout += -I - 2I + 4I + 8I = 9I$$

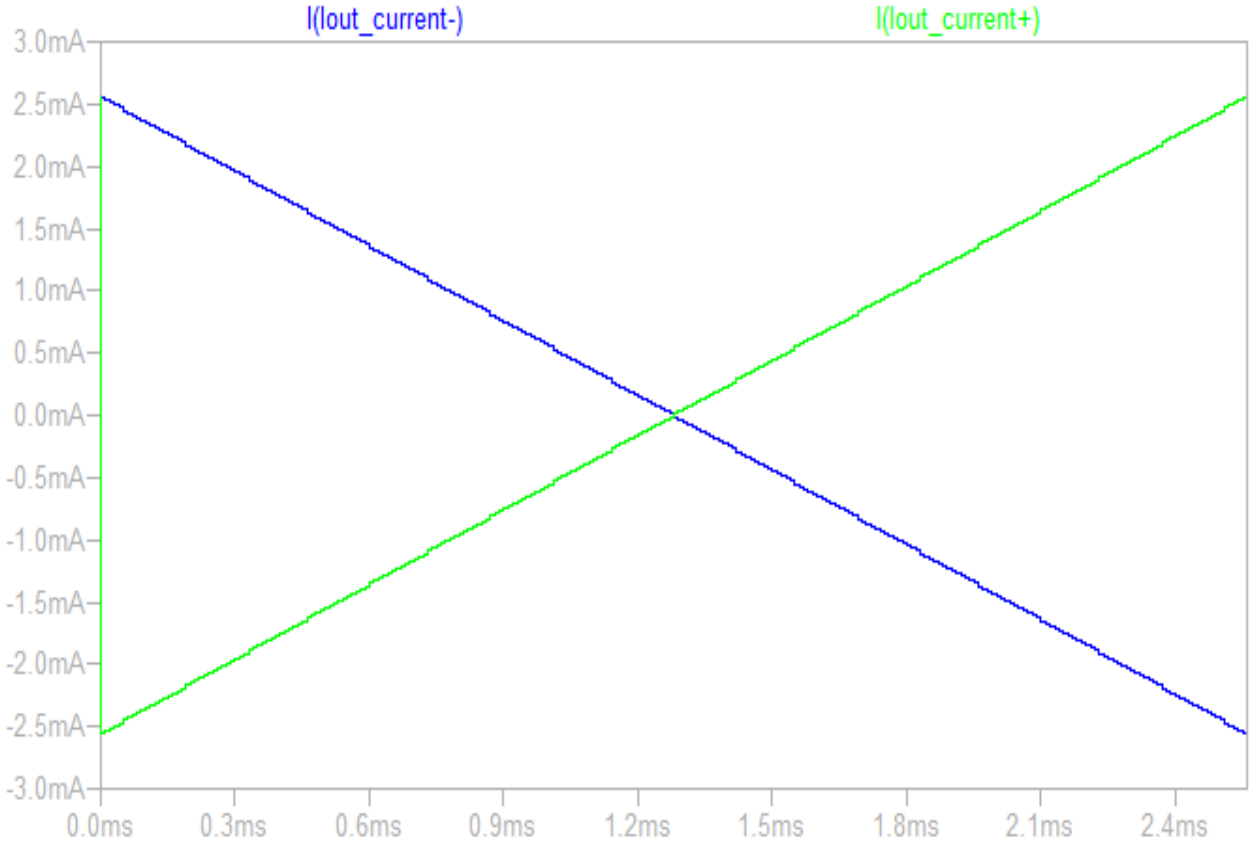


Current Steering Mode Gray Code Input DAC Simulation Results

4-bit case



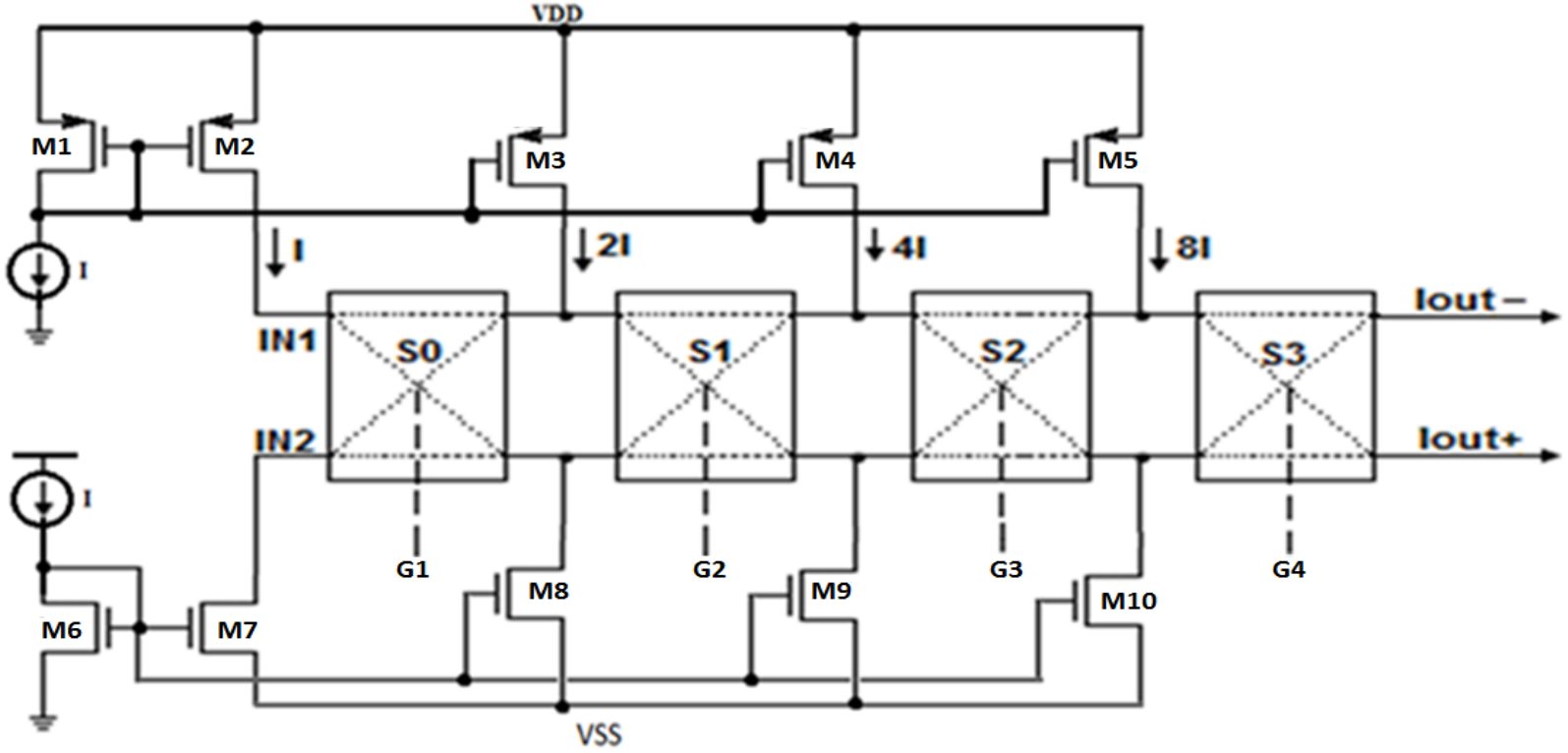
8-bit case



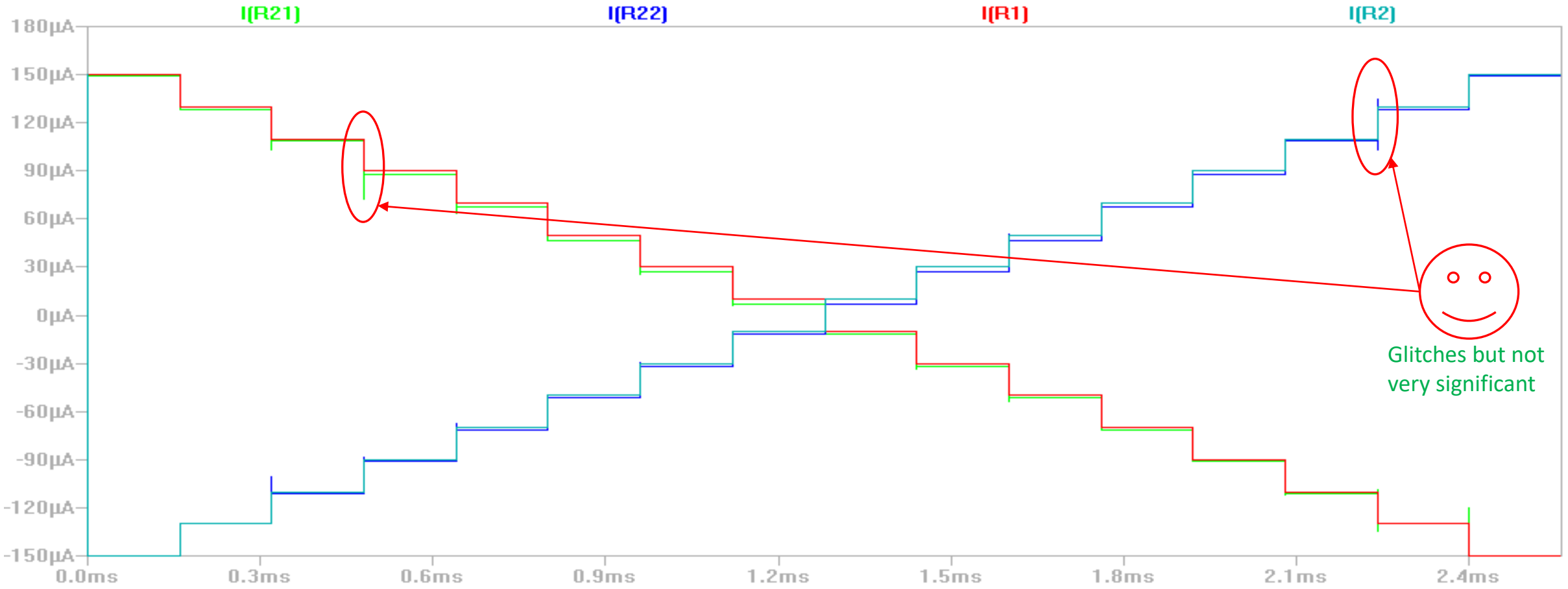
Current Steering Mode Gray Code Input DAC MOSFET Implementation

$M2,\ M3,\ M4,\ M5$ generate$I,\ 2I,\ 4I, 8I$ (current source)

$M6,\ M7,\ M8,\ M9$ generate $I,\ 2I,\ 4I, 8I$ (current sink)



Current Steering Mode Gray Code Input DAC MOSFET Implementation Simulation Results



Conclusion

- ✓ Successful design and Implementation of R-2R DACs using MOSFETs.
  - ✓ Prone to glitches → multiple bits switching at a time.
- ✓ Claims of Gray Code DACs being difficult to design

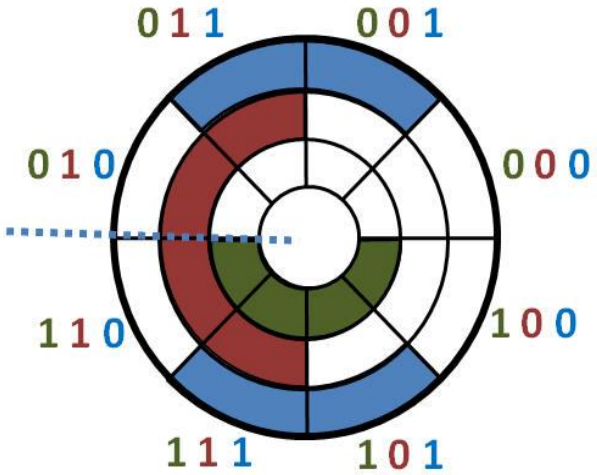
  but we successfully designed and simulated
  - ✓ Gray code Input DACs reduce glitches considerably
  - ✓ No extra space needed for IC design
  - ✓ No extra circuit needed to remove glitch.

Final Statement

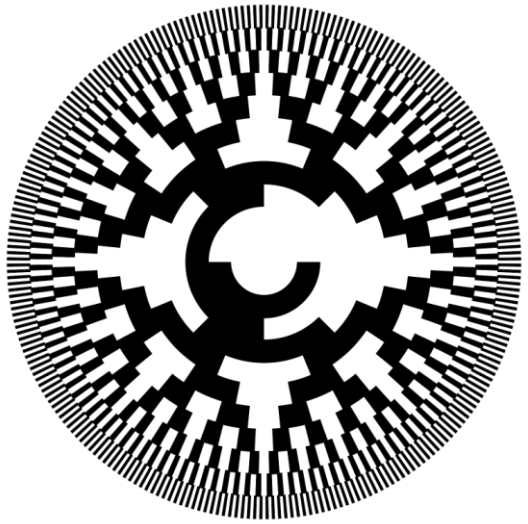
Coding method can lead to robust mixed-signal circuit design.

Gray code was invented by Frank Gray at Bell Lab in 1947.

FRANK GRAY and A. L. Johnsrud in television booth. Behind the glass panels at sides and top are the photo-electric cells.



$Q_2Q_1Q_0$
000
001
011
010
110
111
101
100



Thank you