Self-Calibration and Trigger Circuit for Two-Step SAR TDC

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This paper presents a 2-step successive-approximation-register time-to-digital converter (SAR TDC) architecture with its linearity self-calibrations for absolute (average) delay array variations^{[1][2]}. It also employs a trigger circuit which enables to measure one-shot timing with the SAR ADC; if the trigger circuit is not used in front of our SAR TDC, it can only measure the repetitive clock timing but not the one-shot timing. Their configurations, principles and operations as well as some simulation results are described.

Fig. 1 shows a circuit diagram of the proposed 2-step SAR TDC. Fig. 2 shows a schematic diagram of the algorithm for performing the linearity self-calibration of the absolute variation in the average value of the delay value. By collecting a lot of samples and taking their average to estimate the delay values[τ] of the actual delay elements can be estimated.

Fig. 3 shows a trigger circuit example ^[3]; when the trigger input changes from low to high at time *to* C, then the trigger circuit starts to output the cosine wave whose phase is zero at s at time *to*. T(Fig. 3). By employing this trigger circuit in front of the SAR TDC, they can measure one-shot timing (Fig. 4). Fig. 5 shows timing chart for the circuit in Fig. 4.



Fig.1. Two-step SAR TDC with coarse 3-bit and fine 3-bit configuration.



Fig.3. Trigger circuit in front of the SAR TDC.





Fig.2. Explanation of the self-calibration algorithm



Fig. 5. Timing chart in Fig. 4.

Fig.4. Trigger circuit in front of the SAR TDC.

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