1st IEEE International Workshop on Automotive Reliability & Test

ART-2016

IEEE Philadelphia Section

tttc

1st IEEE International Workshop on Automotive Reliability & Test

in conjunction with ITC / Test Week 2016
Fort Worth Convention Center, TX, USA
November 17-18, 2016

The ART workshop focuses exclusively on test and reliability of automotive and mission-critical electronics, including design, manufacturing, burn-in, system-level integration and in-field test, diagnosis and repair solutions, as well as architectures and methods for reliable and safe operations under different environmental conditions. With increasing system complexity, security, stringent runtime requirements for functional safety and cost constraints of a mass market the reliable operation of electronics in safety-critical domains is still a major challenge. The ART Workshop offers a forum to present and discuss challenges and solutions among researchers and practitioners alike.

Organizing Committee

General Chair:	Y. Zorian, Synopsys
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Panel:	P. Sarson, AMS
Finance:	S. Natarajan, Intel
Publication:	L. Anghel, TIMA Laboratory
Publicity:	P. Bernardi, Polito Torino
Registration:	T. McLaurin, ARM

ART-2016 Schedule

Preliminary Program

17th November, 2016

4:00 – 4:10 P.M. **Opening Remarks**

Moderator: D. Appello, STMicroelectronics – I
General chair: Y. Zorian, Synopsys - USA
Program chair: H-J Wunderlich, Stuttgart U. - D

Keynote 1 – Sanjive Agarwala

Senior Director, Texas Instruments, US

4:10 – 4:40 P.M.

Automotive and Industrial trends and opportunities

Session 1 – In-System Test for Functional Safety

4:40 – 5:20 P.M.

Deterministic ATPG-Based Runtime Test for Realizing Functional Safety in ISO 26262
Y. Maeda, J. Matsushima (Renesas System Design, J)
R. Press (Mentor Graphics, US)

From manufacturing to functional safety use, how infield Build-In Self-Test architecture must evolve to support real time system constraints
C. Eychenne (BOSCH, FR)

Session 2 – Test Generation and Application

5:20 – 6:00 P.M.

Bridge Over Troubled Waters: Critical Area Based Pattern Generation
P. Maxwell (ON Semiconductor, US),
F. Hapke, M. Ryynaenen (Mentor Graphics, D)

Very low supply voltage room temperature test to screen low temperature soft blown fuse fails which result in a resistive bridges
P. Sarson (AMS, A)

Technical Program Committee

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P. van Staa, Bosch
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R. Wagner, Bosch
M. Wahl, Siegen U.

ART-2016 Schedule

Preliminary Program

Panel – What is needed to make a paradigm shift in the level of Quality and Reliability in semiconductors to a level < 10ppb

6:00 – 7:00 P.M.

Moderator and Organizer: P. Sarson, AMS, A

Panelists:
L. Anghel, TIMA Laboratory, FR
W. Dobbelaere, ON Semiconductor, B
R. Van Rijsinge, NXP, NL
Y. Zorian, Synopsys, US

The semiconductor business is at a junction where the required quality level of products is increasing at an exponential rate, whereas the test cost per device is being driven lower. More stringent quality requirements are the result of the concentration on market penetration for one product rather than multiple different products and hence the volume of any one-semiconductor device increases at the same rate as the acceptance of individual products into the market. Whilst quality levels have actually decreased in some cases, more returns have been received from end customers for analysis by the semiconductor providers. Therefore, without significantly increasing quality assurance personnel, semiconductor providers would be at a loss to deal with this changing environment. In this panel, each panelist is asked to give their view on how this seemingly contradictory statement can be resolved and how this stalemate could eventually lead us to a paradigm shift in quality to a level of less than 10ppb.

Workshop Reception

7:00 – 9:30 P.M.

18th November, 2016

7:00 – 8:00 A.M. Breakfast

Keynote 2 – Dave de Maria
Vice President, Synopsys, US

8:00 – 8:30 A.M.

Session 3 – Analog Test and Reliability

8:30 – 9:30 A.M.

Simultaneous Improvement of Fault Coverage and Test Cost using Structured Analog Testing
R. Vanhooren, W. Dobbelaere (ON Semiconductor, B)
A. Coyette, B. Esen, G. Gielen (KU Leuven, B)

Efficient Fault Coverage Assessment for Analog Circuit Test Evaluation with Graph-based Circuit Partition
Z. Liu, S. Chaganti, D. Chen (Iowa State University, US)

Redundant SAR ADC Algorithms for Reliability Based on Number Theory
Y. Kobayashi, T. Arafune, S. Shibuya, H. Kobayashi, H. Arai (Gunma University, J)

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Session 4 – Online Test for Processors

9:30 – 10:10 A.M.

Online LBIST for Automotive on a Multicore Processor
T. McLaurin (ARM, US)

Automotive Microcontrollers On-Line testing, How to Take Advantage of SBST programs
P. Bernardi, R. Cantoro, E. Sanchez (Polito Torino, I)
S. De Luca, A. Sansonetti (STMicroelectronics, I)

10:10 A.M. Poster Introduction

Poster Session and Coffee Break

10:15 – 10:45 A.M.

Poster 1: **The Challenges to Model Reliability and Robustness in Automotive Domain against Aging, Temperature and Complexity of Process Scaling in Micro Electronics**
D. Sharma, S. Reddy, B. Simhadri (Globalfoundries India, IN)

Poster 2: **A New Approach for Automotive Electronics Quality Improvement Using Big Data Analytics**
R. Dixit, H. Reddy (Optimal+, US)

Poster 3: **Scan-based checksum generation for high Diagnostic Coverage**
J. Schat (NXP, D)
R. van Rijsinge (NXP, NL)

Poster 4: **Functional Testing with Structural Coverage of Requirements Models in UML**
S. Bugga, P. Kalyansundaram, A. Gadkari (KPIT Technologies, IN)
S. Ramesh (General Motors, US)

Poster 5: **Doubling Schemes for Defect-Tolerant Clock-Delivery TSVs in 3D ICs**
T.-C. Huang, S.-Y. Huang (Taiwan National Tsing-Hua University, TW)

Session 5 – Dependability

10:45 – 12:05 A.M.

A Fail-Functional Automotive CPU Subsystem Architecture for Mitigating Single Point of Failures
B. Venu, E. Ozer, X. Iturbe, A. Robinson (ARM, UK)

On Mitigating Sense Amplifier Offset Voltage Degradation
D. Kraak, I. Agbo, M. Taouil, S. Hamdioui (Delft, NL)
F. Catthoor, P. Weckx (IMEC, B)
S. Cosemans (surecore, B)
W. Dehaene (Katholieke Universiteit Leuven, B)

Improving the Dependability of AMR Sensors Used in Automotive Applications
A. Zambrano, H. Kerkhoff (Twente U / CTIT-TDT, NL)

A DMA-based RAM Memory Stress Schema for Burn-In
D. Appello (STMicroelectronics, I)
P. Bernardi, R. Cantoro, E. Sanchez, M. Restifo, F. Venini (Politecnico di Torino, I)

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Lunch

12:05 – 1 P.M.

Special Session – Safety and Reliability: From ICs to Automotive

1:00 – 2:30 P.M.

Moderator and Organizer: R. Parekhji, TI, IN

Functional Safety and Reliability for automotive IC Design
R. Mariani (Intel, I)

Functional Safety & Reliability – Impact on Semiconductor Test & Ecosystem
R. Knoth, (Cadence, US)

Evolving with the Automotive Industry
B. Richardson (Texas Instruments, US)

Meeting IP Requirements for Automotive SOCs
Ron DiGiuseppe (Synopsys, US)

Session 6 – AUTOSAR and Error Management

2:30 – 3:50 P.M.

The increasing demand in automotive systems for functional safety is driving the need for integrated random and systematic error management in processors
J. Scobie (ARM, UK)

Integration Testing of AUTOSAR Components
S. Ramesh (General Motors, US)
A. Petrenko (CRIM, C)

AUTOSAR Software Debug and Analysis using Virtual Platforms
M. Safar (Department of Computers and Systems Engineering, Ain-Shams University, EGY)
A. Bakr, M. El-Moursy, A. Salem (Mentor Graphics, EGY)

Safety Analysis of AUTOSAR WatchDog Manager: A Case Study
G. Bahig (Mentor Graphics, EGY)
A. El-Kadi (American University in Cairo, EGY)
A. El-Hamedy, A. Salem (Mentor Graphics, EGY)

Closing Discussions

3:50 P.M.

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