

# Redundant SAR ADC Algorithms for Reliability Based on Number Theory

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**Abstract**— This paper describes SAR ADC algorithms to ensure reliability with possible targets for automotive applications. The SAR ADC has beneficial characteristics of low power and small chip area, and hence it is widely used, especially in automotive applications together with micro-controllers. There, digital error correction method using redundant comparison is an effective method to improve its reliability and conversion speed because it realizes correction of misjudgment at a comparator and incomplete settling of an internal DAC. Then this paper describes two effective redundancy design algorithms based on number theory: (i) The first one uses Fibonacci sequence and its property called Golden ratio Especially, several interesting properties are clarified that contribute to solve SAR ADC design problems, such as radix standard and shortening required settling time. (ii) The second one uses pseudo silver ratio (square root of 2) for the SAR ADC, which leads to simple SAR logic design and fast conversion speed in case of multiple clock period usage.

**Keywords**—SAR ADC, Reliability, Redundancy, Error Correction, Fibonacci Sequence, Golden Ratio, Silver Ratio

## I. INTRODUCTION

**S**UCCESSIVE approximation resistor A-D converters (SAR ADCs) are gathering attention thanks to their useful characteristics for automotive applications. Its performance improvement of conversion reliability and speed is demanded to match with high technology, and we study here about redundancy design of SAR ADCs for their realization.

Redundancy design enables digital error correction to improve SAR ADC performance [1-7]. One redundancy design method is to use a non-binary search algorithm instead of a binary search algorithm. There, extra comparison steps and a non-binary weighted DAC are needed for a redundant SAR ADC and we have to determine its non-binary weighted values. Generally, their values are determined using a non-binary radix method or selected flexibly by the SAR ADC designer. However the efficient and systematic redundant SAR ADC algorithm design method has not been studied well yet.

In this paper, we discuss two methods to design redundant SAR algorithms based on number theory, i.e., (i) Fibonacci sequence (or golden ratio) and (ii) Pseudo silver ratio methods. Then we obtain well-balanced non-binary weight values.

This paper is organized as follows: Section II overviews SAR ADCs, and Section III outlines their redundancy design. Section IV presents our first method of redundancy design using Fibonacci sequence and Section V shows the incomplete settling problem of an internal DAC inside the SAR ADC. Section VI shows our second method of redundancy design using pseudo-silver-ratio for the SAR ADC using multiple

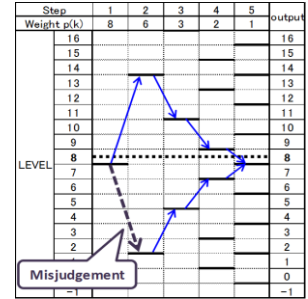


Fig. 3 Operation of a 4-bit 5-step SAR ADC in case of correct and incorrect judgments.

clock periods. Section VII provides conclusion.

## II. OVERVIEW OF SAR ADC

The SAR ADC consists of a sample-and-hold circuit, a comparator, a DAC, an SAR logic and a timing generator as shown in Fig. 1. Conversion of the SAR ADC is based on principle of balance and generally it uses the binary search algorithm. Firstly, the sample-and-hold circuit samples analog

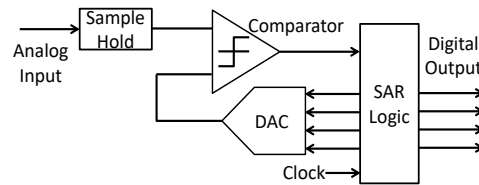


Fig. 1 Block diagram of an SAR ADC.

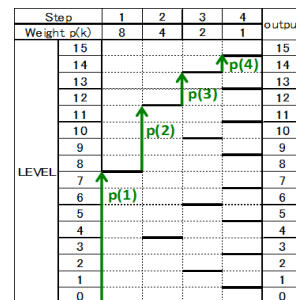


Fig. 2 Binary search algorithm of a 4-bit 4-step SAR ADC.

input voltage regularly. Secondly, the comparator compares the sampled voltage and the reference voltage which is generated by the DAC and decides 1-bit digital output. Thirdly, SAR logic provides digital code for the DAC input based on the comparator output. The sampled input voltage and the updated DAC output voltage are compared by the comparator. These operations are repeated and finally SAR ADC obtains the whole digital output.

Fig. 2 shows the binary search algorithm of a 4-bit SAR ADC. The bold line in Fig. 2 indicates the reference voltage value to compare with the sampled input voltage at each step. Their

values are calculated by either sum or difference between the last step reference voltage and the weighted voltage  $p(k)$  of each step as shown in Fig. 2. The comparator outputs 1 if the input voltage is larger than the reference voltage; otherwise it outputs 0. Then we obtain the digital output at each step.

Usually,  $p(k)$  which is defined as a reference voltage weight of the DAC is a binary weighted value because the binary search algorithm is efficient. However, in reality, there is possibility of comparator misjudgment due to DAC incomplete settling and sample-and-hold circuit incomplete settling as well as noise. In the binary weighted SAR ADC, one misjudgment of the comparator leads to incorrect output and low reliability. Hence this paper investigates redundancy design of the SAR ADC to enable digital error correction for misjudgment of the comparator.

### III. REDUNDANCY DESIGN OF SAR ADC

Redundancy design is a technique to improve circuit and system performance. In the SAR ADC, redundancy design method adding extra comparison is often utilized [1-7]. This method changes binary weights to non-binary weights for the DAC that makes reference voltage and realizes digital error correction with redundancy property.

Fig. 3 shows an example of two redundant search operations of a 4-bit 5-step SAR ADC. There, the input voltage is 8.6-LSBs and the reference voltage weights  $p(k)$  are 1, 2, 3, 6 and 8. The one operation (solid arrows) assumes that the comparison is correct, whereas the other (dotted arrows) assumes that it is incorrect. However both obtain the correct digital output of 8 by digital error correction. In the 4-bit 5-step SAR ADC as shown in Fig. 3, there are  $2^5$  comparison patterns against  $2^4$  output patterns. In other words, a given output level can be expressed by multiple comparison patterns. Therefore even if comparator decision is wrong at some steps, the correct ADC output may be obtained. This is the basic principle of the digital error correction. In addition, even if the number of the comparison steps is increased, the digital error correction enables high-speed AD conversion as a whole, because the digital error correction can take care of the DAC incomplete settling [1-7]; thus redundancy design has potential for reliable and high-speed SAR AD conversion.

#### A. Generalization of redundant SAR ADC design

We generalize SAR ADC redundancy design from using some equations [3]. If we realize an  $N$ -bit resolution SAR ADC by  $M$ -step comparison ( $M \geq N$ ), the reference voltage  $V_{ref}(k)$  at  $k$ -th step and ADC output  $D_{out}$  are defined by (1) and (2), respectively. Here  $k = 1, 2, 3, 4, \dots, M$  and  $p(k)$  is the reference voltage weight value for addition to (or subtraction from) the DAC input in the previous step. Moreover, each  $d(k)$  is decided by the comparator output. If the comparator digital output at  $k$ -th step is 1, then  $d(k) = 1$ , and if the comparator digital output at  $k$ -th step is 0, then  $d(k) = -1$ . Furthermore  $d(0) = 1$ .

$$V_{ref}(k) = \sum_{i=1}^k d(i-1) \cdot p(i). \quad (1)$$

We can also define ‘‘the redundancy at  $k$ -th step  $q(k)$ ’’ as (2).

$$q(k) = -p(k+1) + 1 + \sum_{i=k+2}^M p(i). \quad (2)$$

Here  $q(k)$  indicates correctable difference between the input voltage and the reference voltage at  $k$ -th step[3]. Even if the comparator result is wrong in the  $k$ -th step, we can obtain the correct output as long as (3) is satisfied.

$$q(k) > |V_{in} - V_{ref}(k)|. \quad (3)$$

Fig. 4 shows  $q(k)$  as an example of Fig. 3. In Fig. 4, one-way arrows indicate  $q(k)$ , while two-way arrows show correctable input ranges which means that these input ranges have multiple expressions. As shown in Fig. 4, since the input voltage 8.6-LSBs satisfies (3), the SAR ADC can obtain the correct output in Fig. 3. Therefore  $q(k)$  expresses the digital error correction capability. Moreover  $q(k)$  is defined by only the reference voltage weight  $p(k)$  in (2), and thus  $p(k)$  is an important parameter in the redundant SAR ADC algorithm design.

#### B. Conventional method to decide reference voltage weight

Only reference voltage weight  $p(k)$  decides correction capability of the redundant SAR ADC; if the design of the reference voltage weight  $p(k)$  is not appropriate, the SAR ADC cannot have the maximum compensation ability. The ratio of the reference voltage weights  $p(k+1)/p(k)$  must be between 1 (unary) and 2 (binary). In conventional methods, we can obtain the  $k$ -th step reference voltage weight  $p(k)$  based on the radix  $r$  in (4). Here,  $N$  is the ADC resolution, and  $M$  is the number of the whole steps.

$$p(k) = r^{M-k}. \quad (4)$$

Here  $1 < r < 2$  and  $p(1) = 2^{N-1}$ . We set  $p(1)$  to  $2^{N-1}$  which is half of the full scale range, to make the SAR algorithm efficient. Additionally, the total number of steps  $M$  has to satisfy (5) to enable all output level expression.

$$2^{N-1} - 1 \leq \sum_{i=0}^{M-2} p(M-i). \quad (5)$$

We can systematically decide conditions for redundancy design

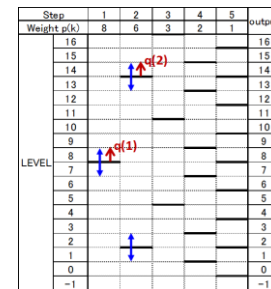


Fig. 4 4-bit 5-step SAR ADC algorithm and definition of correctable difference  $q(k)$ .

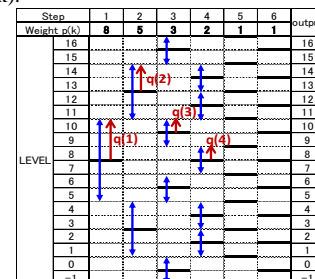


Fig. 5 Non-binary search algorithm using Fibonacci sequence of a 4-bit 6-step SAR ADC.

based on the above equations.

### C. Problems of Conventional methods

Conventional methods may have some issues. First, the reference voltage weight  $p(k)$  in (5) is not an integer which is not suitable for the circuit design. Since the reference voltage weights  $p(k)$  must be integers for conversion accuracy, its rounding to an integer is needed to determine  $p(k)$ . However rounding causes change of the radix and variability of the correction capability  $q(k)$ , which may disturb performance improvement.

In addition, there is difficulty of an appropriate radix choice. Fig. 3 shows an example in case of radix 1.80 and rounding. However in Fig. 4, two-way arrows indicate that correctable input range cannot cover all input range, which means that there are some ranges that cannot be corrected. In Fig. 4, if the ADC input is not within the range of 1~3, 7~9, 13~15 LSBs, redundancy design becomes meaningless because these input ranges cannot be expressed in multiple. Thus the inappropriate selection of a radix loses redundancy design effectiveness. On the other hand, the selection of a small radix for larger values of  $q(k)$  induces an increase in the number of SAR ADC comparison steps and hence conversion time. In this way, there is a trade-off between correction capability and conversion speed, and the SAR ADC designer is forced to search a radix that is the most suitable for SAR ADC; these are causes of design difficulty.

### D. Time redundancy and circuit redundancy

In this paper, we consider the time redundancy or step redundancy for the SAR ADC. Also circuit redundancy may be possible. For example, we previously investigated to use three comparators in the SAR ADC and there digital error correction was incorporated for high reliability and fast conversion [8]. However, we consider from our experiences that the time redundancy would be more effective, especially for low power.

## IV. REDUNDANCY DESIGN USING FIBONACCI SEQUENCE

Here, we propose a redundancy design method using *Fibonacci sequence*.

### A. Fibonacci sequence

Fibonacci sequence is defined with a recurrence formula as shown in (6), where  $n$  in (6) is an integer greater than or equal to 0. It was presented in 1202 by Leonardo Fibonacci [9].

$$F_{n+2} = F_n + F_{n+1}. \quad (6)$$

Here,  $F_0 = 0$  and  $F_1 = 1$ . Fibonacci numbers are expressed as the following by calculating (6) :

$$0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, 233, 377, 610, \dots$$

In short, the sum of neighboring two terms is next term. In addition, the closest terms ratio of Fibonacci sequence converges to about 1.62 as shown in (7).

$$\lim_{n \rightarrow \infty} F_n / F_{n-1} = 1.6180339887 \dots = \varphi. \quad (7)$$

This ratio is called ‘‘Golden ratio’’, and widely recognized as the most beautiful ratio. We can find Fibonacci sequence and Golden ratio in various places such as nature and human societies, and they have many interesting properties [9].

### B. Fibonacci sequence application to SAR ADC design

Equation (6) indicates that Fibonacci sequence numbers are integers, and (7) indicates that the closest term ratio of Fibonacci number converges to about 1.62 called Golden ratio. In other words, Fibonacci sequence can generate a number string at radix 1.62 with only integer terms. In general, multiplication result of an integer and a decimal fraction is a decimal fraction, nevertheless multiplication result of an integer and a decimal fraction (1.62..) is an integer in Fibonacci sequence. Therefore we can apply Fibonacci sequence to the redundancy algorithm design of the SAR ADC using effective properties of the fixed rate and integer terms.

We select the reference voltage weight  $p(k)$  by using Fibonacci sequence as shown in (8).

$$p(k) = F_{M-k+1}. \quad (8)$$

Here,  $p(1) = 2^{N-1}$ . In short, we set  $p(k)$  to Fibonacci number in ascending order. Since  $p(k)$  follows the property of Fibonacci sequence, the proposed method can realize radix 1.62 by using only integers. Here the total number of steps  $M$  satisfies (5). Fig. 5 shows correctable difference in a redundant search of a 4-bit 6-step SAR ADC using Fibonacci sequence as shown in (8). One-way arrows indicate  $q(k)$  and two-way arrows show correctable input range just like in Fig. 4.

### C. Discovered Properties and Effectiveness

We have discovered two interesting properties in Fig. 5 as follows:

**Property 1:** Correctable difference  $q(k)$  of  $k$ -th step is always Fibonacci number  $F_{M-k-1}$ .

$$q(k) = F_{M-k-1}. \quad (9)$$

**Property 2:**  $q(k)$  of  $k$ -th step is exactly in contact with  $q(k+1)$  of  $(k+1)$ -th step without overlap. In other words, the tips of two-way arrows of  $k$ -th step and  $(k+1)$ -th step points are exactly the same level.

The property 2 is important for design of redundant SAR ADC algorithm due to the following two reasons:

First, the property can be a standard for all redundancy designs in the viewpoints of the radix of Fibonacci sequence which is golden ratio 1.62..., and the boundary condition of  $q(k)$ . Hence, we can confirm that  $q(k)$  becomes overlapped, separated or contact by using golden ratio. If the radix value is larger than the golden ratio, the redundancy is small and  $q(k)$  boundaries are separated as shown in Fig. 4. On the other hand, if the value of the radix is smaller than the golden ratio, the redundancy is large and  $q(k)$  boundaries are overlapped, which means that all input range have multiple expressions. Thus we can easily select the radix by considering the golden ratio as the standard.

Second, the redundancy design using Fibonacci sequence can be considered as the most efficient design. The property 2 indicates that  $q(k)$  covers all input range by minimum extra comparison steps. Therefore, we can realize the redundancy design without waste by only integer terms. Moreover even if we change the first step reference voltage, the property 2 holds because of (2), which means that the redundancy design using Fibonacci sequence is flexible.

## V. DAC INCOMPLETE SETTLING

### A. Summary and Generalization of DAC incomplete settling

An SAR ADC contains a DAC that outputs a reference voltage by the comparison result at previous step. Since the DAC output must change from the previous reference voltage to next one, the DAC output takes some time to settle. In the binary search algorithm which does not have redundancy, the DAC must take time to settle between the output voltage of the DAC and next reference voltage within 0.5-LSB for accurate conversion. This DAC settling time often dominates the SAR ADC conversion time. Besides, this settling time is much longer for a high resolution SAR ADC due to requirement for very small settling error. On the other hand, in the non-binary search algorithm which has finite correctable difference  $q(k)$ , the DAC can decrease required settling time, thanks to redundancy and digital error correction at the following steps as shown in Fig. 6.

Difference between the DAC output voltage and the next reference voltage can be smaller than  $q(k)$  to accurate conversion when conversion step has correctable difference  $q(k)$ . We generalize SAR ADC incomplete settling by using a first-order system model as shown Fig. 6. Firstly, we can obtain the output voltage of the DAC as (10) from Fig. 6.

$$V_{DAC}(t) = V_{ref}(k) + \{V_{ref}(k-1) - V_{ref}(k)\} \exp(-t/\tau). \quad (10)$$

Here,  $\tau$  is a time constant of the DAC output.

To satisfy correctable condition at the redundant SAR ADC, difference between the input voltage of the comparator and the reference voltage has to be smaller than  $q(k)$ . Thus we can use comparison voltage  $V_{com}(k)$ , that has distance  $q(k)$  from the original reference voltage, to compare the input voltage. Consequently settling time  $T_{settle}(k)$  which is the time to make the  $k$ -th step comparison voltage to change from the previous comparison voltage  $V_{com}(k-1)$  to next comparison voltage  $V_{com}(k)$ . As we should consider the longest settling time to decide each step settling time, we obtain  $k$ -th step settling time  $T_{settle}(k)$  as (11).

$$T_{settle}(k) = \tau \ln\{[p(k) + q(k-1)]/q(k)\}. \quad (11)$$

Note that if correctable difference  $q(k)$  is less than 1-LSB, we can regard  $q(k)$  as 0.5-LSB. Finally, a variable clock SAR ADC takes sum of  $T_{settle}$  as total settling time. However, for a fixed clock SAR ADC total settling time is equal to the longest span of  $T_{settle}$  multiplied by the number of steps of SAR ADC used.

### B. Analysis of Fibonacci SAR ADC settling time

We consider the settling time of the redundant SAR ADC using Fibonacci sequence in theory. In the Fibonacci sequence SAR ADC, we can transform (11) to (12) by using (8) and (9).

$$T_{settle}(k) = \tau \ln\{(F_{M-k+1} + F_{M-k})/F_{M-k-1}\}. \quad (12)$$

Here we transform (13) using (6) as follows:

$$\begin{aligned} T_{settle}(k) &= \tau \ln\{(F_{M-k} + F_{M-k-1}) + F_{M-k}\} / F_{M-k-1} \\ &= \tau \ln\{(2F_{M-k} / F_{M-k-1}) + 1\}. \end{aligned} \quad (13)$$

Therefore we obtain the settling time of  $k$ -th step at the SAR ADC using Fibonacci sequence as shown (14) by using (7).

$$T_{settle}(k) = \tau \ln(2\varphi + 1) \approx 1.444\tau. \quad (14)$$

Equation (14) indicates that settling time is constant regardless of step number  $k$  or usage of variable clock. On the other hand, the conventional method using radix cannot realize constant settling time, because its reference voltage weight  $p(k)$  does not have relationship for correctable difference  $q(k)$ .

### C. Settling time comparison of each method

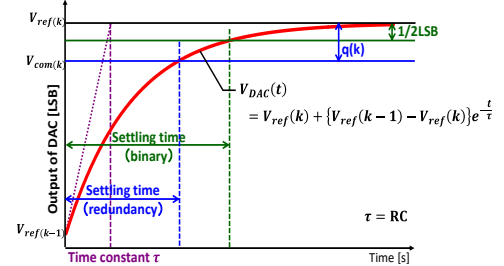


Fig. 6 Principle of settling time acceleration with incomplete settling of the internal DAC.

We have compared the Fibonacci sequence method and the radix one in terms of the redundant SAR ADC settling time. We have carried out comparison at 8-bit SAR ADC under the conditions of variable and fixed clocks, and obtained the results shown in Fig. 7 using (10). We found that total settling time using Fibonacci sequence is the shortest in fixed clock frequency for each ADC resolution.

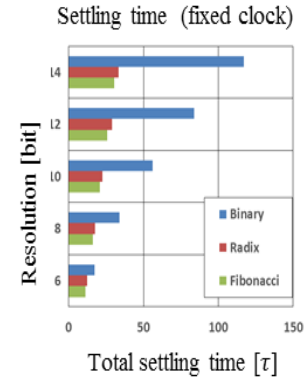


Fig. 7 the comparison of the settling time of ADC at each resolution.

## VI. REDUNDANT ALGORITHM USING PSEUDO-SILVER-RATIO

Redundancy design has possibility for a great ADC, but we need further investigation of designing the redundant algorithm. Then, we derive pseudo-silver-ratio sequence by considering effective utilization of correctable input range, and we propose another redundancy design method using the sequence.

### A. Derivation of reference voltage weight $p(k)$ that can realize decrease of settling time

Here, we consider to reduce the settling time to shorten AD conversion time. If the reference voltage weight  $p(k)$  is equal to correction capability  $q(k)$ , the redundant ADC can make the most of correction capability to decrease the settling time. Therefore we decide reference voltage  $p(k)$  values as shown in (15) while step number  $k$  satisfies  $2 \leq k \leq M-2$ .

$$p(k) = q(k) \quad (15)$$

From (2), we have to determine  $p(M)$  and  $p(M-1)$  to derive reference voltage weight  $p(k)$  by using (16). Then we decide  $p(M)=1$  and  $p(M-1)=1$ . We can calculate reference voltage weight  $p(k)$  as follows:

$$p(M-2) = q(M-2) = -p(M-1) + 1 + \sum_{i=M}^M p(i) = 1$$

$$p(M-3) = q(M-3) = -p(M-2) + 1 + \sum_{i=M-1}^M p(i) = 2$$

$$p(M-4) = q(M-4) = -p(M-3) + 1 + \sum_{i=M-2}^M p(i) = 2$$

Then we obtain following numbers:

1, 1, 1, 2, 2, 4, 4, 8, 8, 16, 16, 32, 32, 64, 64, 128, 128 ...

These numbers are used in order for the SAR ADC weights,  $p(k)$  as (16).

For  $1 < k < M$ , we have

$$p(k) = \sqrt{2}^{M-k-4} \left( (1 + \sqrt{2}) - (-1)^{M-k+1} (1 - \sqrt{2}) \right) \quad (16)$$

$$\text{Also, } p(1) = 2^{N-1}, p(M) = 1$$

$p(1)$  is determined by  $N$ , that is the ADC resolution. We assume the number of total step  $M$  is shown in Eq. (17) by using (5).

$$M = 2(N - 1) \quad (17)$$

Fig. 8 shows a redundant search operation of a 4-bit SAR ADC using (17). We notice the correctable range is extended without space and the reference voltage weight  $p(k)$  satisfies (15).

### B. Silver ratio

Term of a series derived by (16) doubles every two terms. It means that the terms are obtained by multiplication of a term and square root of 2 every one term. Therefore we call this weighted method as a pseudo-silver-ratio method.

Silver ratio (square root of 2) is a ratio between one side of a square and the diagonal line of the square. Silver ratio is recognized as one of the most beautiful ratio especially in Japan like Golden ratio in Western world, and Silver ratio has been used frequently for architectures, arts, and characters in Japan.

### C. Analysis settling time of Pseudo-Silver-ratio method

Here, we calculate incomplete settling time by using (11). Incomplete settling time depends on step number  $k$ . When step number  $k$  satisfies  $2 \leq k \leq M - 2$ , we can transform (11) using (15) as follows:

$$T_{\text{settle}}(k) = \tau \ln(p(k) + p(k-1)/p(k))$$

By using (16), the closest term ratio ( $=p(k-1)/p(k)$ ) are as follows:

$$p(k) + p(k-1)/p(k) = \begin{cases} 1 & (k = 2n + 1) \\ 2 & (k = 2n) \end{cases}$$

Here,  $n = 1, 2, 3, \dots$ . Then we obtain the following settling time:

$$T_{\text{settle}}(k) = \begin{cases} \tau \ln\{(p(k) + p(k))/p(k)\} \\ \tau \ln\{(p(k) + 2p(k))/p(k)\} \end{cases}$$

Step	1	2	3	4	5	6	Output
Weight $p(k)$	8	2	2	1	1	1	
LEVEL	15						15
	14						14
	13						13
	12						12
	11						11
	10						10
	9						9
	8						8
	7						7
	6						6
	5						5
	4						4
	3						3
	2						2
	1						1
	0						0

Fig. 8 Redundant search algorithm of a 4-bit 6-step SAR ADC using pseudo-silver-ratio weights.

$$= \begin{cases} \tau \ln 2 = 0.6931\tau & (k = 2n + 1) \\ \tau \ln 3 = 1.0986\tau & (k = 2n) \end{cases}$$

Thus the SAR ADC takes two types of settling time alternately. As  $q(1)$  is equal to  $p(1)/2$ , when  $k = 1$ , the settling time is given as follows:

$$T_{\text{settle}}(1) = \tau \ln 2 = 0.6931\tau$$

If correctable difference  $q(k)$  is less than 1 LSB, we can regard  $q(k)$  as 0.5 LSB. Then when  $k = (M-1)$ , the settling time is as follows:

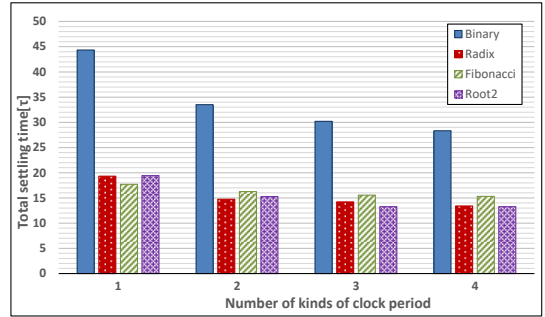


Fig. 9 Comparison of total settling time for each method in 3 types of clock periods.

$$T_{\text{settle}}(M-1) = \tau \ln 2^2 = 2 * 0.6931\tau = 1.3862\tau$$

Similarly, when  $k = M$ , the settling time is as follows:

$$T_{\text{settle}}(M) = \tau \ln 3 = 1.0986\tau$$

These results indicate that the SAR ADC using pseudo-silver-ratio needs only 3 types of settling time. Besides, the settling time at  $(M-1)$ -step which is  $1.3862\tau$ , is realized by doubling of  $0.6931\tau$ . Therefore, if the ADC has a clock period doubling circuit, only two types of clock period to realize incomplete settling is needed. As the incomplete settling time depends on the clock period, this method realized with only two types of clock period has superiority for simplification of circuit.

### D. Comparison of total settling time

We calculate total settling time of the DAC by using (11) and compare each method. Here we examine the radix method, random method, Fibonacci method, and pseudo-silver-ratio method. We substitute the random method for the round robin algorithm because the round robin algorithm needs to examine a huge number of combinations for reference voltage weight. The random method tries 10,000 times and selects combination realizing the shortest settling time.

We also investigate how much total settling time depends on the number of clock periods. For example, if the ADC can use only one clock period, the total settling time is equal to the longest span of settling time multiplied by the number of steps of the SAR ADC used. We calculate the case using 1~4 types of clock period.

Fig. 9 shows calculation results in case of 8-bit SAR ADCs. We see from this result that the pseudo-silver-ratio method realizes the fastest settling in case of using 3 types of clock period. In an 8-bit SAR ADC using 3 types of clock period, the pseudo-silver-ratio method can reduce settling time by 56.2% from the binary method and by 5.0% from the random method.

We obtain almost the same results in 4, 6, and 10-bit cases. Practically, since the settling time is realized by using only two types of clock period, this method is useful for reduction of the settling time. Besides, we have to note that any method cannot realize shorter settling time than pseudo-silver-ratio method in case using 3 types of settling time. It may indicate that the pseudo-silver-ratio method is the fastest method.

### E. Advantages of using pseudo-silver-ratio method

There are two advantages of using the pseudo-silver-ratio method for SAR ADC implementation.

First, ADC needs only few types of clock period. Generally, ADC needs many types of clock periods that correspond to the settling time at each step. However the pseudo-silver-ratio method needs only two types of clock period and it helps to ease circuit design.

Second, the SAR logic circuit can be designed with ease. Table I shows input transitions of 4-bit DAC using the binary method and the pseudo-silver-ratio method. In Table I, the ADC input is 0 LSB and first reference voltage weight  $p(1) = 2^{N-1}$  in the pseudo-silver-ratio method is dealt as sum of two  $2^{N-2}$ . As shown in Table I, both methods are controlled in the same way. Therefore pseudo-silver-ratio method can be realized by changing wiring of SAR logic circuit for the binary method. In addition, the pseudo-silver-ratio method eases design of encoder. Typically, a redundant SAR ADC needs large encoder and decoder. But the pseudo-silver-ratio method can use full adder to make encoder. Because reference voltage weight  $p(k)$  values are made by putting two binary weights in order, we can encode digital code by addition as shown in Fig. 10. We see from Table I and Fig. 10 that we can realize a redundant SAR ADC using the pseudo-silver-ratio method in the same way as the binary SAR ADC by changing wiring and adding full adder for SAR logic circuit.

## VII. CONCLUSIONS

We have described two redundant SAR ADC algorithms to ensure reliability for automotive applications together with micro-controllers. The first one uses Fibonacci sequence and its property called Golden ratio for the digital error correction. Especially, several interesting properties have been clarified that contribute to solve SAR ADC design problems. The second one uses pseudo silver-ratio (square root of 2) for the SAR ADC, which leads to simple SAR logic design and fast conversion speed in case of multiple clock period usage.

We conclude this paper by remarking that here we have demonstrated redundant SAR ADC algorithms to realize

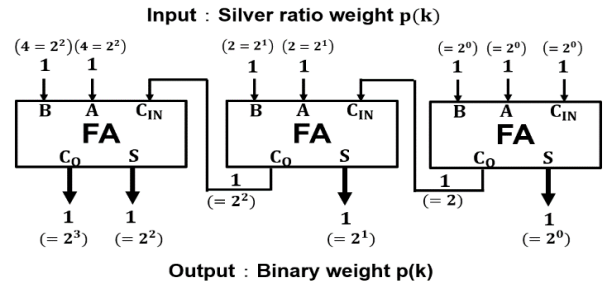


Fig. 10 4-bit encoder in case of using pseudo-silver-ratio weights.

reliable electronic systems and also shown that the benefits of the reliability lead to high-speed operation. Our methods do not require special device/process or additional large circuit / major circuit change; we have used only basic but beautiful mathematics (number theory).

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Table I. 4-bit DAC input in case of using binary weights and pseudo-silver-ratio weights.

Binary weight		Weight p(k)			
step	Vref(k)[LSB]	8	4	2	1
1	8	1	0	0	0
2	4	0	1	0	0
3	2	0	0	1	0
4	1	0	0	0	1

Silver ratio weight		Weight p(k)					
step	Vref(k)[LSB]	4	4	2	2	1	1
1	8	1	1	0	0	0	0
2	6	0	1	1	0	0	0
3	4	0	0	1	1	0	0
4	3	0	0	0	1	1	0
5	2	0	0	0	0	1	1
6	1	0	0	0	0	0	1