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S25-3 Room 3B
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Optimization and Analysis of High Reliability 30-50V Dual RESURF LDMOS

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Outline

- Research Background & Objective
- Conventional ①, ② & Proposed LDMOS
- Simulation Results
  - I_{DS}-V_{DS} Characteristics
  - Breakdown Characteristics & Locations
  - Hole Current Density & Electric Field Profiles
  - Tradeoff Between $R_{on}A$ & BV_{DS}
  - Total Power Dissipation
- Conclusion

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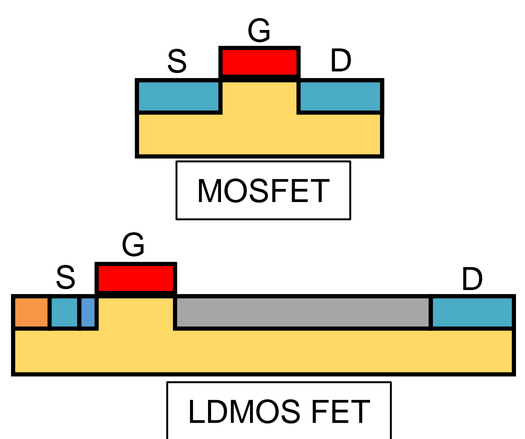
Research Background & Objective

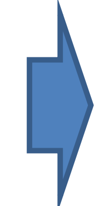
LDMOS (**L**aterally **D**iffused **MOSFETs**)

- A kind of power MOSFETs
- Used as switching devices of DC-DC converters (at less than 100V)
- Generally high on-resistance



LDMOS for 30-50V automotive applications require high reliability

Important points
- Impact ionization
- Current expansion (Due to Kirk effect)



Suppression !

Objective

Obtain high reliability LDMOS with low on-resistance

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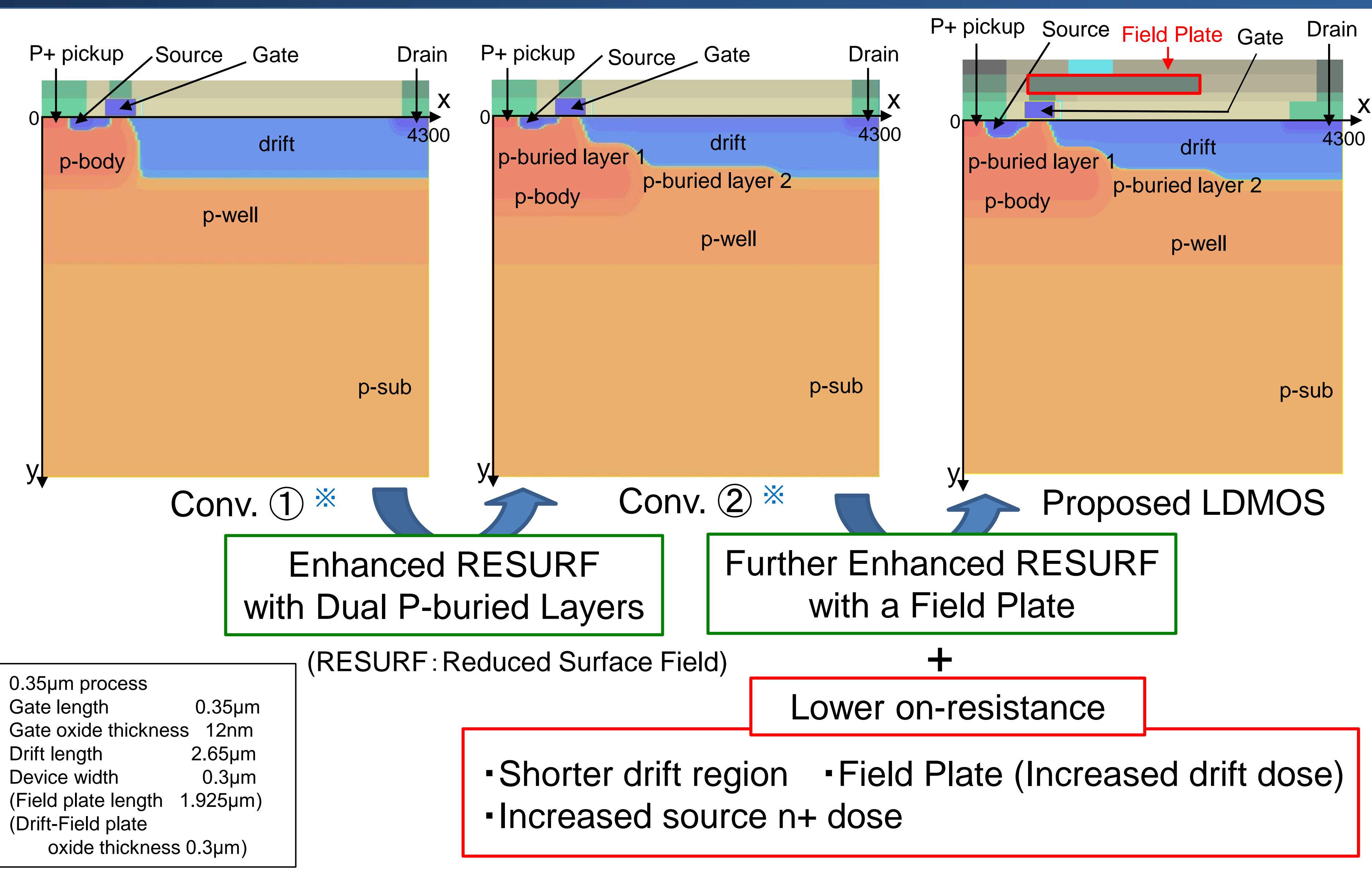
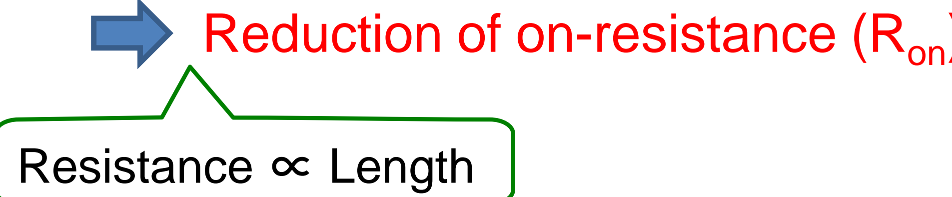
Conventional ①, ② & Proposed LDMOS



※J. Matsuda, et al., “A Proposal of High Reliability Nch-LDMOS,” IEEJ Workshop, SPC-15-148, Nagasaki (Oct. 2015).

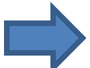
Lower On-Resistance

Ⅰ. Shorter drift region



Reduction of on-resistance (R_{on})

Ⅱ. Field Plate (FP)

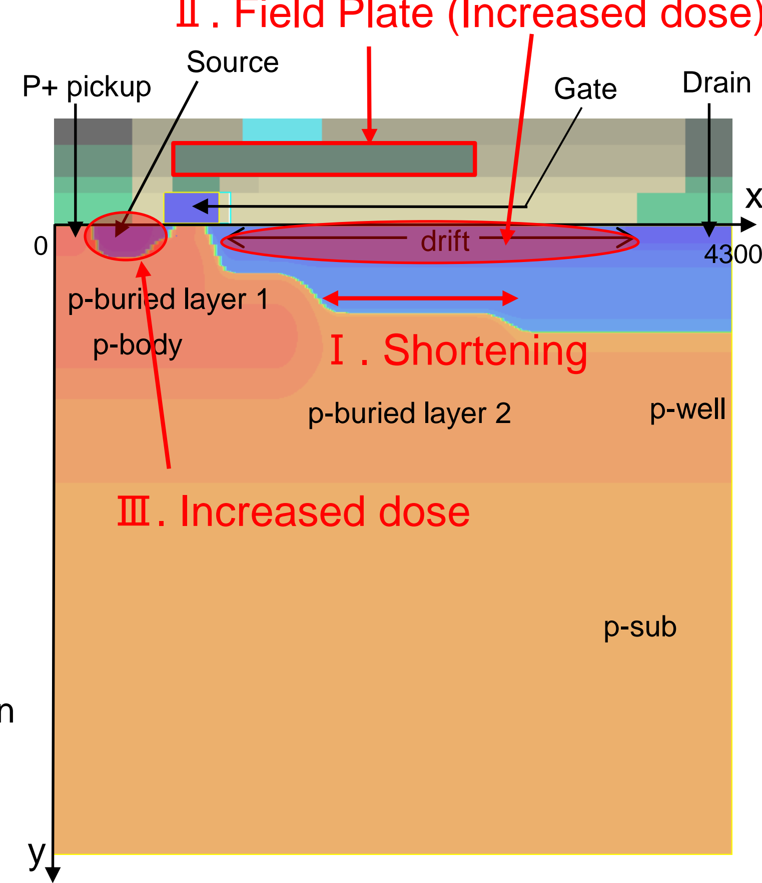


Enhancement of RESURF effect

⇒ Increased drift dose ⇒ Lower R_{on}

Ⅲ. Increased source n+ dose

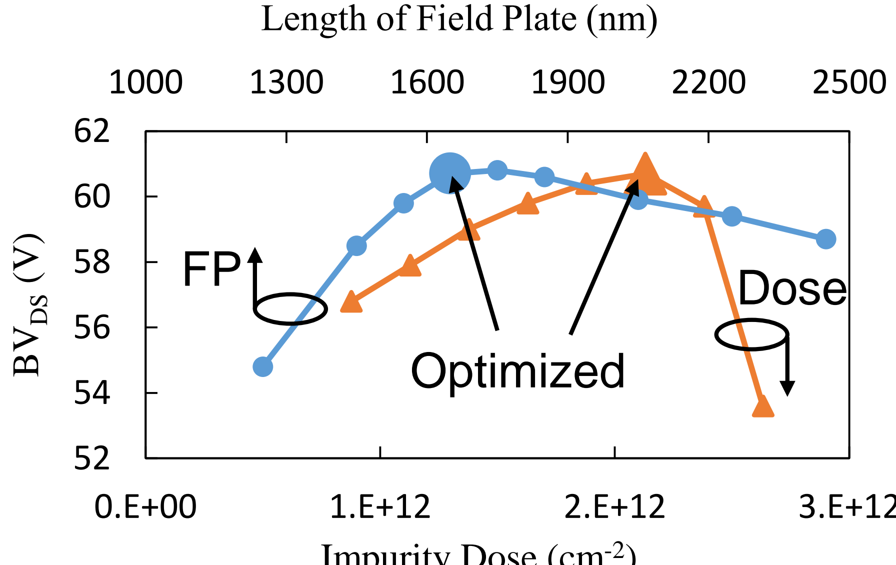
- Lower source resistance ⇒ Lower R_{on}
- Suppression of back-gate effect ⇒ increase of current drivability

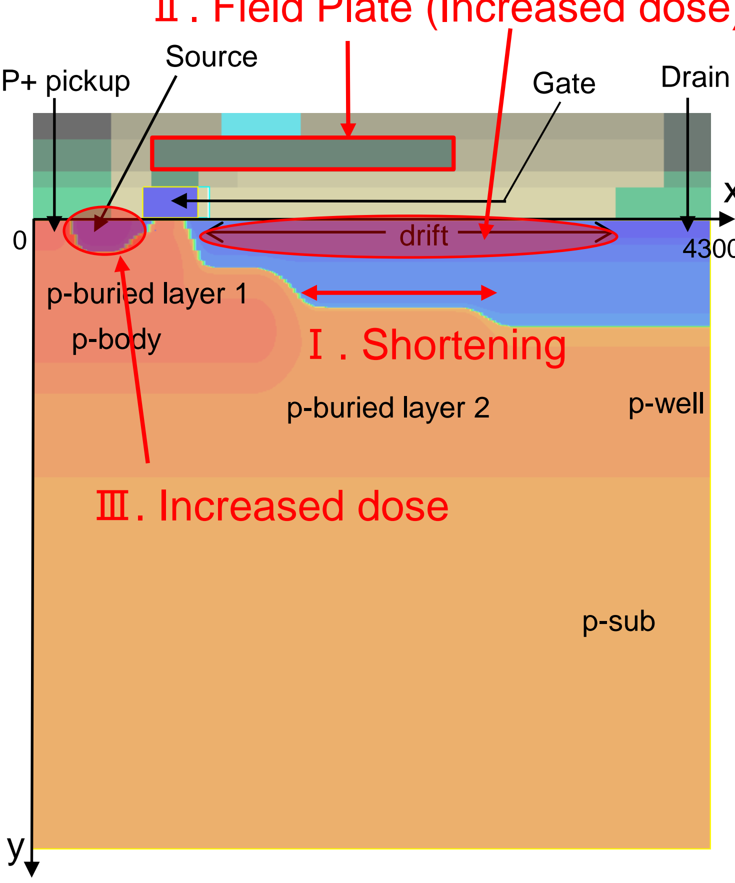


Optimization of Proposed LDMOS

Optimized drift dose & FP length
to obtain maximum BV_{DS}

Drift dose ⇒ $2.13 \times 10^{12} cm^{-2}$
FP length ⇒ 1625nm





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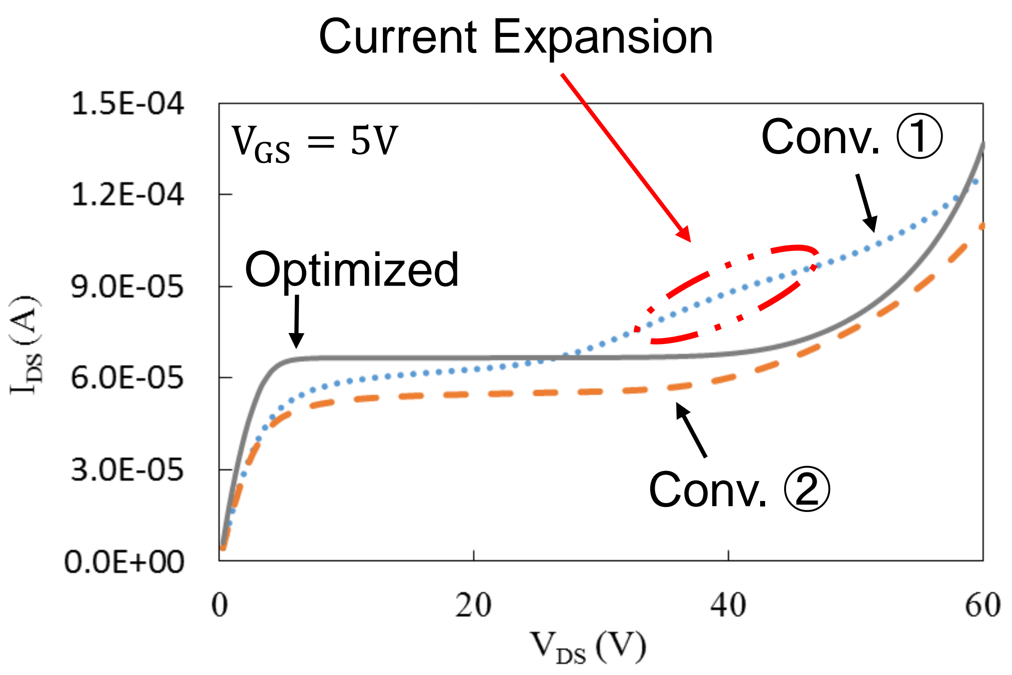
  - **Hole Current Density & Electric Field Profiles**
  - **Tradeoff Between $R_{on}A$ & BV_{DS}**
  - **Total Power Dissipation**
- Conclusion

*Simulator: 3D TCAD (Device Simulator: Advance/DESSERT)
Developed by AdvanceSoft Corporation, Japan

I_{DS}-V_{DS} Characteristics

Current Expansion



	Conv. ①	Conv. ②	Optimized
Current expansion suppression	×	○	○
Specific on-resistance $R_{on}A$ (A=width×pitch)	$68.7 m\Omega mm^2$ (A=0.3×4μm²)	$69.3 m\Omega mm^2$ (A=0.3×4μm²)	$44.8 m\Omega mm^2$ (A=0.3×3.725μm²)

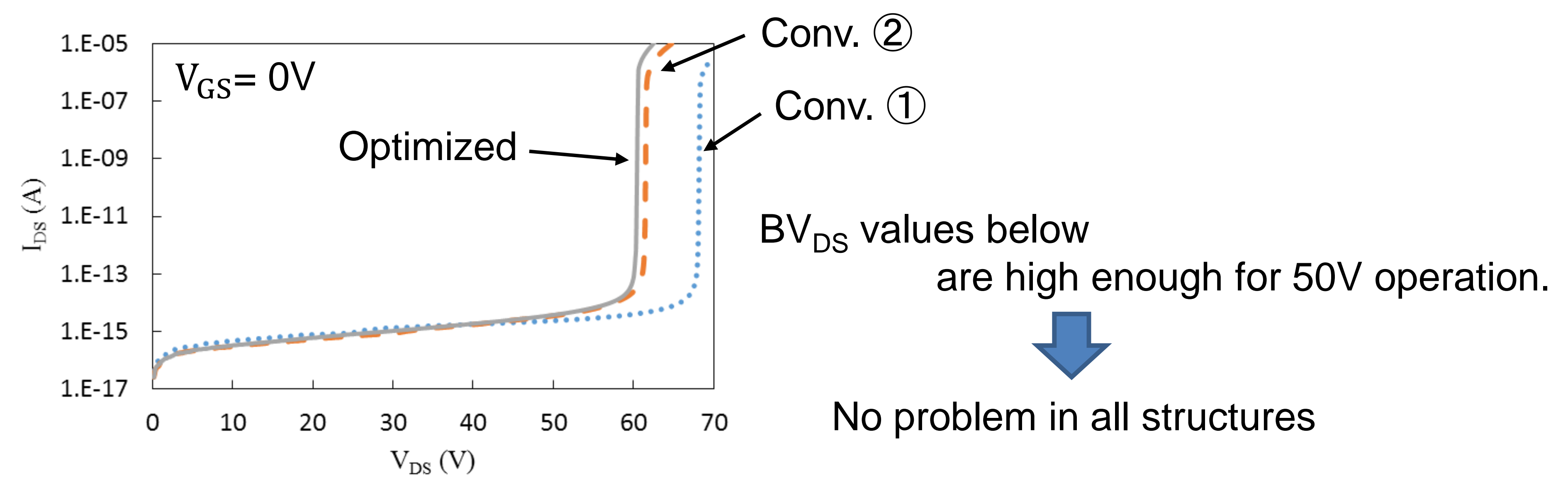
Low reliability

High reliability

High reliability

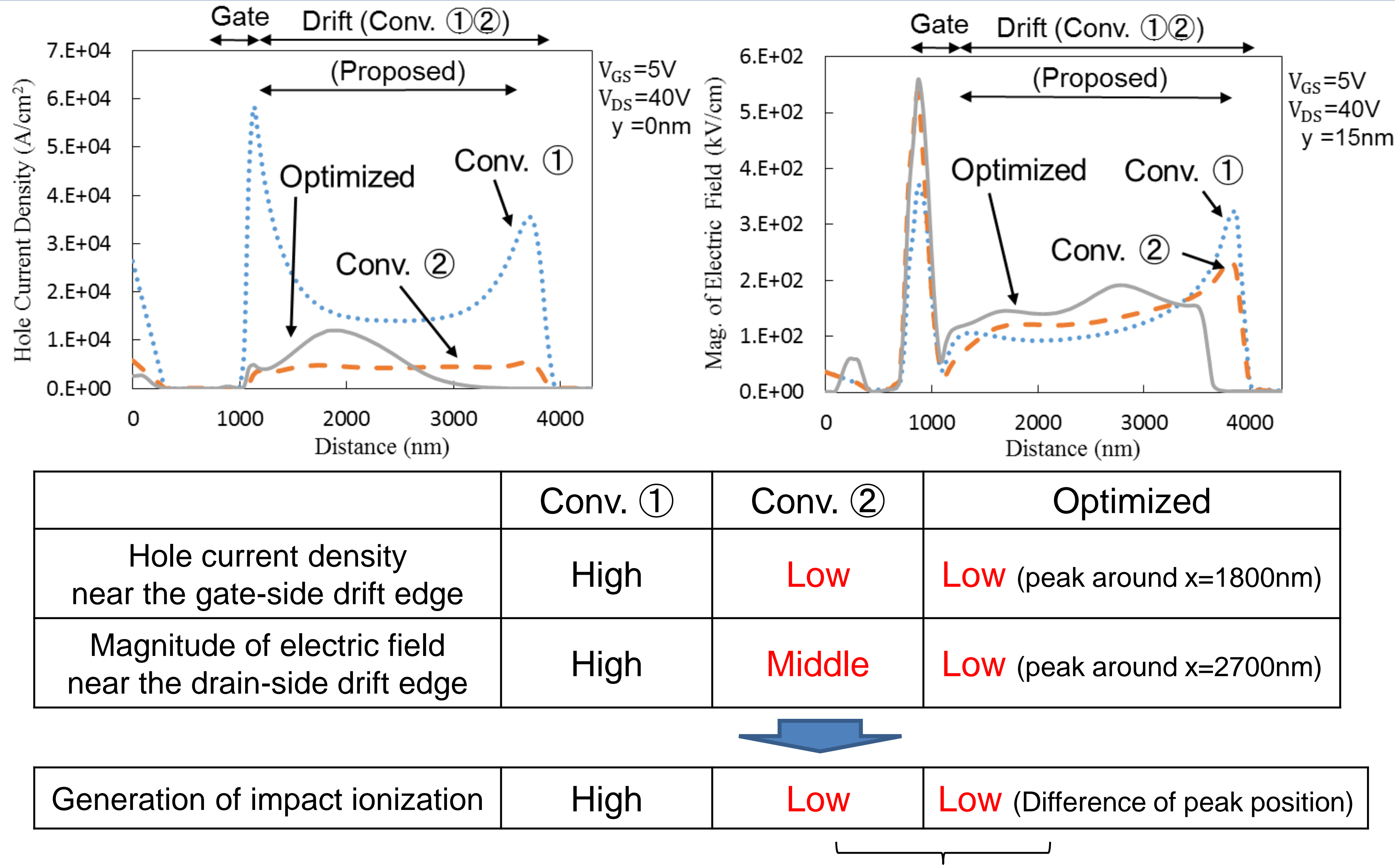
Low $R_{on}A$

Breakdown Characteristics & Locations



	Conv. ①	Conv. ②	Optimized
Breakdown Voltage	67.6V	61.0V	60.7V
Breakdown location All in the bulk Good ESD performance !	S G Drift D	S G Drift D	S G Drift D

Hole Current Density & Electric Field Profiles

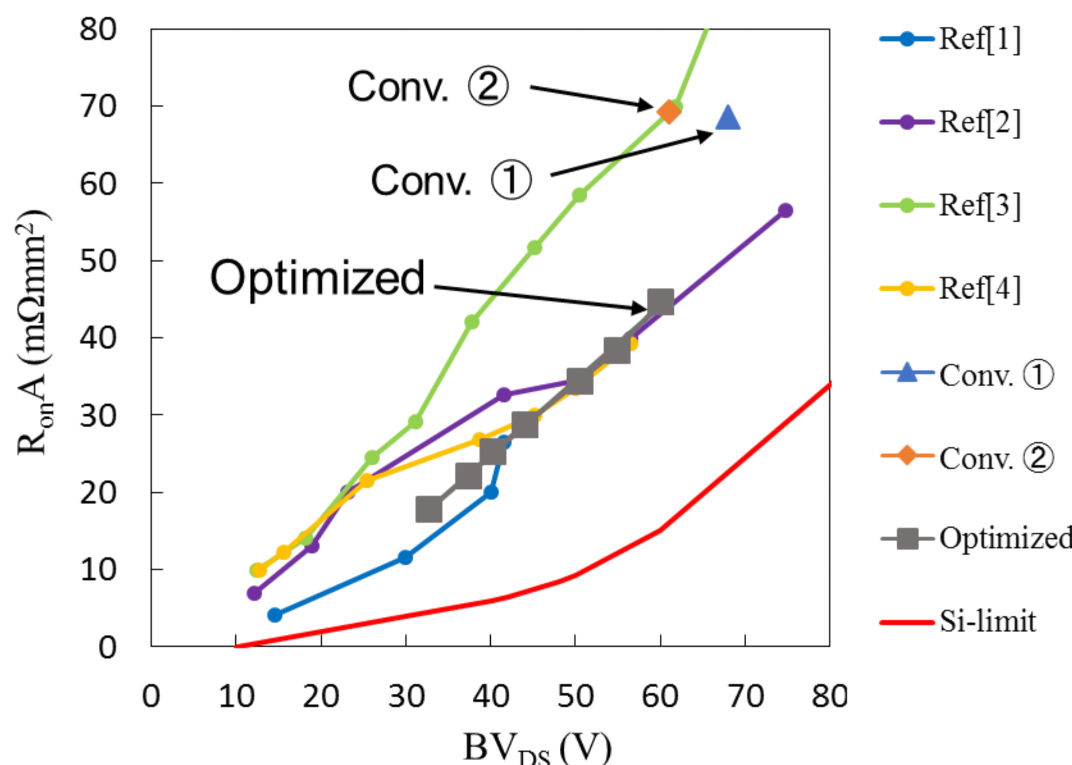


	Conv. ①	Conv. ②	Optimized
Hole current density near the gate-side drift edge	High	Low	Low (peak around x=1800nm)
Magnitude of electric field near the drain-side drift edge	High	Middle	Low (peak around x=2700nm)

Generation of impact ionization	High	Low	Low (Difference of peak position)

※Thanks to dual RESURF

Tradeoff Between $R_{on}A$ & BV_{DS}



The optimized LDMOS has good $R_{on}A$ and BV_{DS} characteristics

Ref[1]:S.Pendharkar "7 to 30V state-of-art power device implementation in 0.25μm LBC7 BiCMOS-DMOS process technology" Proc. Of ISPSD, p419-422, 2004. （Texas Instruments（USA））

Ref[2]:R.Zhu, "Implementation of high-side, "high-voltage RESURF LDMOS in a sub-half micron smart power technology" ,ISPSD, p403-406, 2001.（Motorola（USA））

Ref[3.4]:Choul-Joo Ko, et al., "Implementation of Fully Isolated Low Vgs nLDMOS with Low Specific On-resistance," ISPSD, pp. 24-27 (2011).（Dongbu Hitek（Korea））

Switching Loss

t=0[s]

R_G 500kΩ

R_D 5MΩ

5V

LDMOS

40V

Circuit for switching loss analysis

V_{GS}

5V

Gate charge

t[s]

I_{GS}

t_1

t[s]

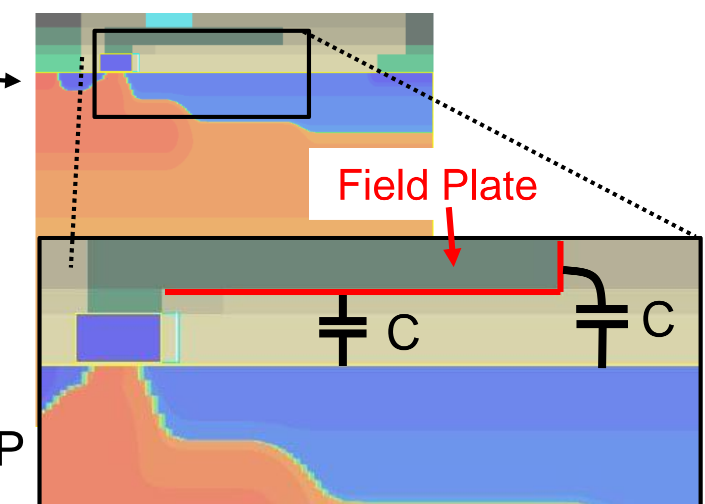
Transient wave

$$Q_g = \int_0^{t_1} I_{GS}\, dt$$

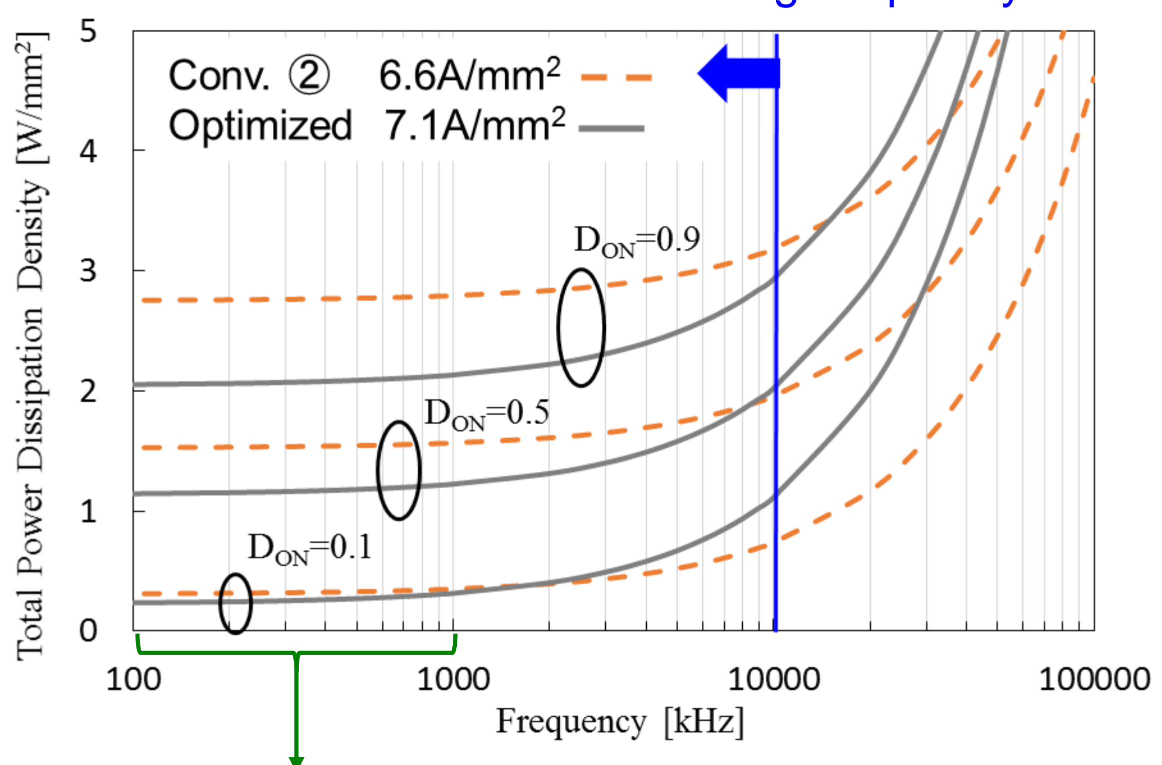
	Conv. ②	Optimized
$R_{on}A$ (mΩmm²)	69.3	44.8
Q_g/A (nC/mm²)	1.49	3.13
FOM (=R_{on}×Q_g) (mΩnC)	104	141

（Figure of Merit）

※ Larger capacitance caused by FP



Total Power Dissipation



Practical switching frequency range of DC-DC converters

- Total power dissipation = Gate driving loss + Switching loss + Conduction loss

Conv. ② > Optimized LDMOS

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Conclusion

We have obtained the optimized 30-50V LDMOS with
(1) High reliability, (2) State-of-the-art $R_{on}A$-BV_{DS} characteristics,
(3) Low power dissipation density in the practical switching frequency range.

Items	Conv. ①	Conv. ②	Optimized	
Current expansion suppression	×	○	○	⇒(1)
$R_{on}A$ (mΩmm²)	68.7	69.3	44.8	⇒(2)
BV_{DS} (V)	68	61	60	⇒(2)
Breakdown location	Bulk	Bulk	Bulk	⇒(1)
Hole current density near the gate-side drift edge	High	Low	Low	⇒(1)
Magnitude of electric field near the drain-side drift edge	High	Middle	Low	⇒(1)
FOM(=R_{on}×Q_g) (mΩnC)		104	141	
Total power dissipation density (In practical switching frequency range of DC-DC converters)		High	Low	⇒(3)

Acknowledgement

We would like to express sincere thanks to AdvanceSoft Corporation for lending us 3D TCAD simulator.

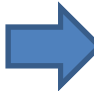
The 3D TCAD developed by AdvanceSoft Corporation was assisted by A-STEP program of Japan Science and Technology Agency, National Research and Development Agency.

Appendix

3D TCAD simulator

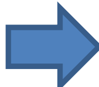
3D TCAD Simulator ・・・ Advance/DESSERT（β ver.） AdvanceSoft Corporation

・Using models close to the actual structure

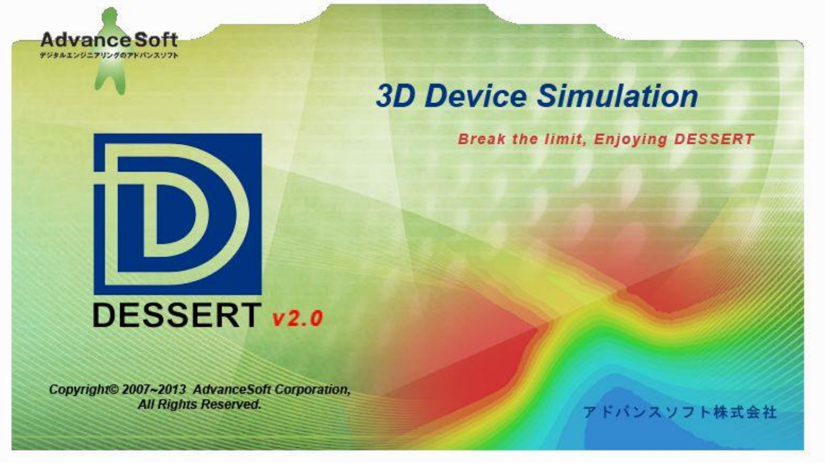


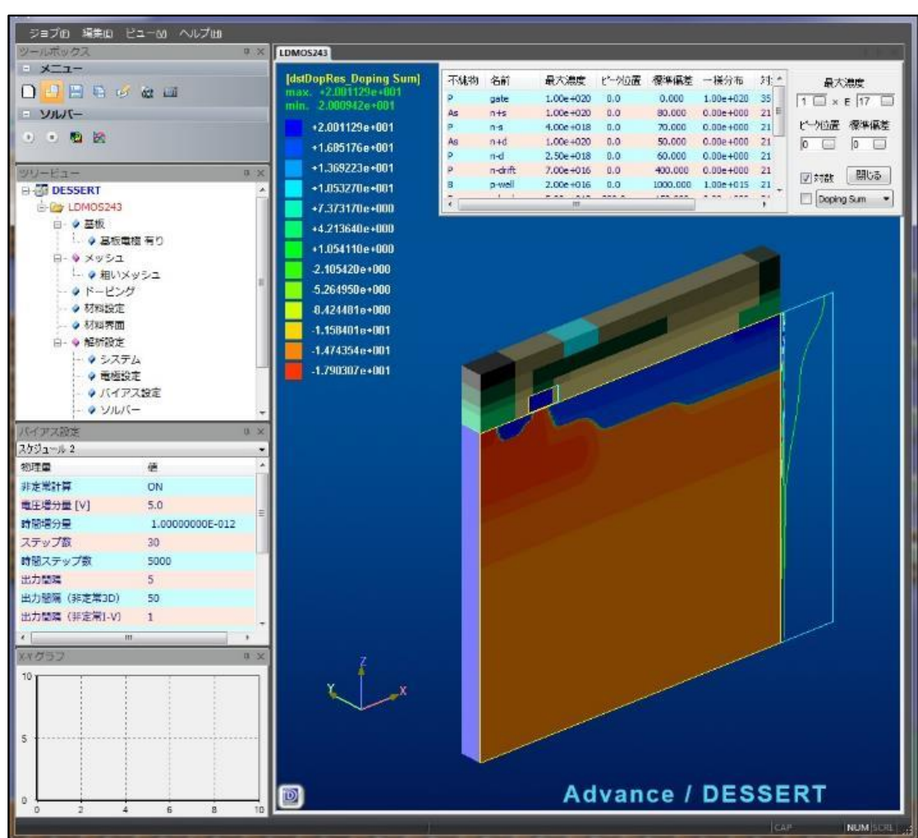
High precision

・No need to make the actual structure



Development in a short time

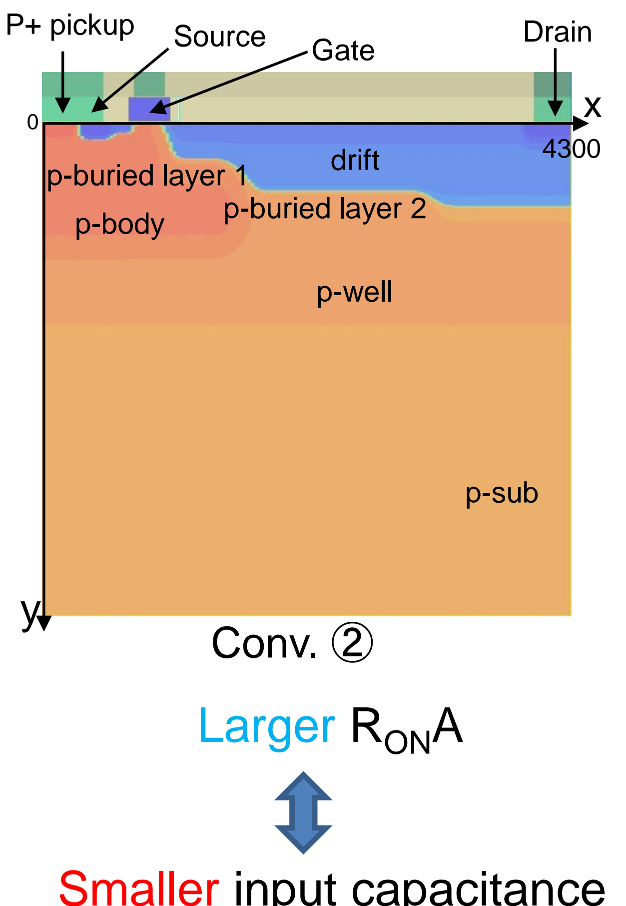




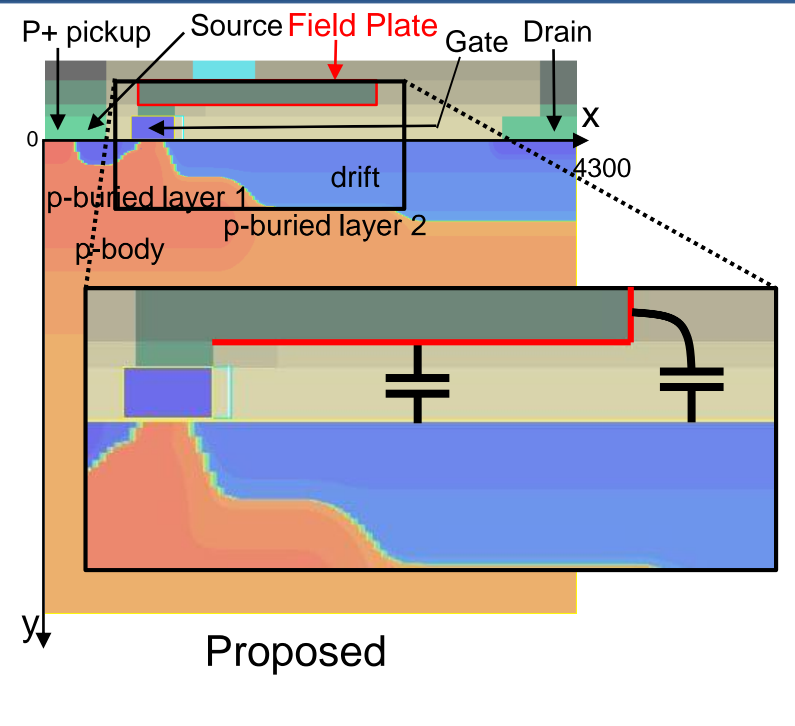
Simulator screen

App.

Structure Analysis



Conv. ②



Proposed

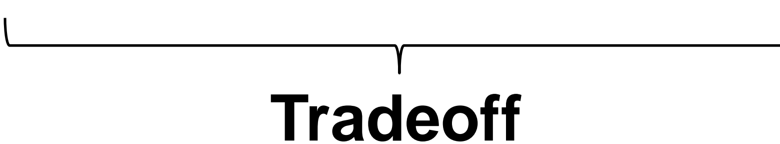
Larger $R_{ON}A$

Smaller input capacitance

Smaller $R_{ON}A$

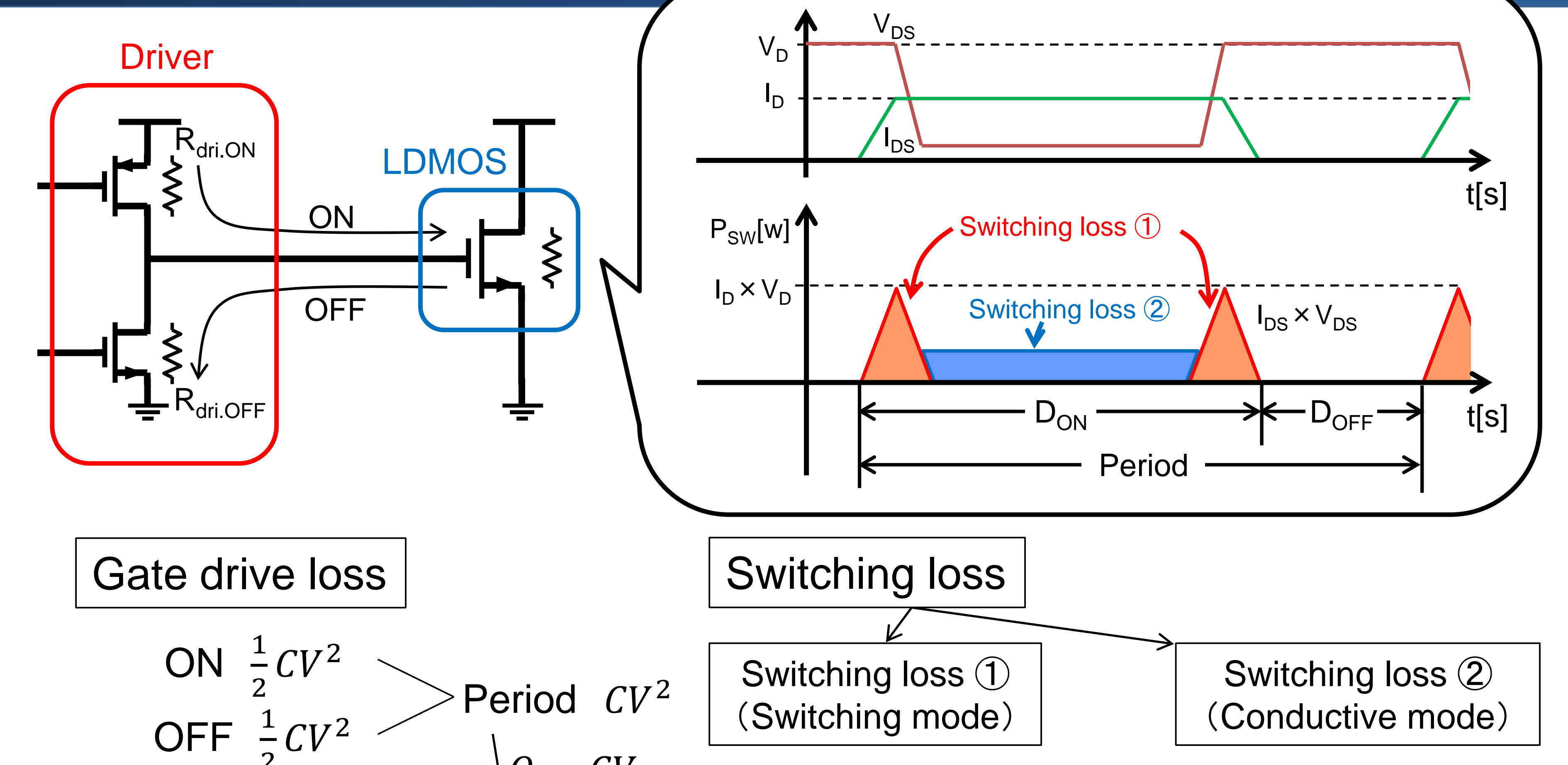
Lager input capacitance

because of Field Plate (Miller capacitance)



Tradeoff

Detail of Dissipation



Area of triangle

ON-time

Total power dissipation [w]

$$= f \times Q_g V_{GS} + f \times 2 \int_{turn_ON} i_{ds} v_{ds} dt + D_{ON} \times I_{DS} V_{DS}$$

Frequency dependence

Duty ratio dependence

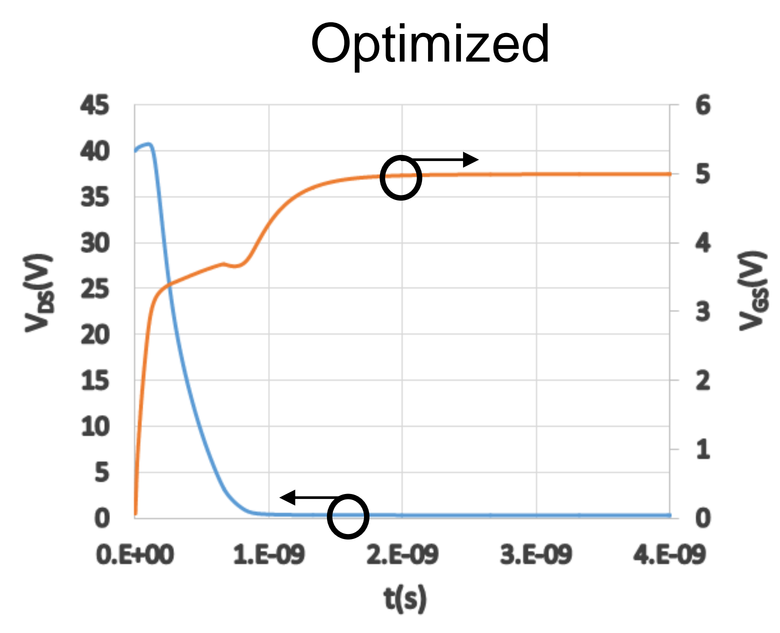
App. Transient Characteristics during Turn-on

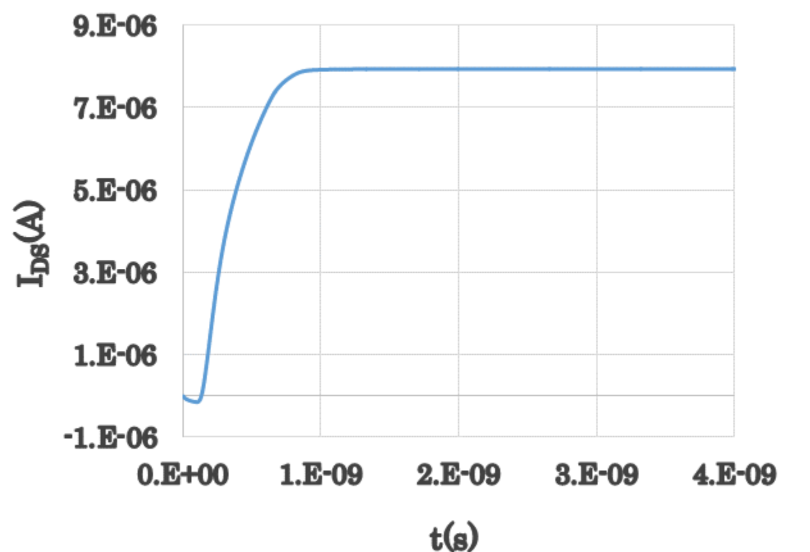
Conv. ②

45 40 35 30 25 20 15 10 5 0
V_{DS}(V)
6 5 4 3 2 1 0
V_{GS}(V)
0.E+00 1.E-09 2.E-09 3.E-09 4.E-09
t(s)

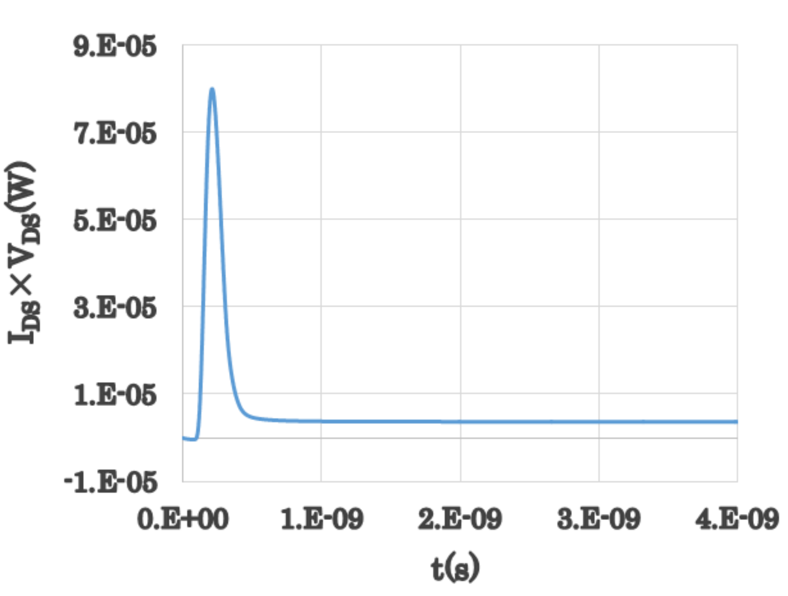
9.E-06 7.E-06 5.E-06 3.E-06 1.E-06 -1.E-06
I_{DS}(A)
0.E+00 1.E-09 2.E-09 3.E-09 4.E-09
t(s)

Optimized

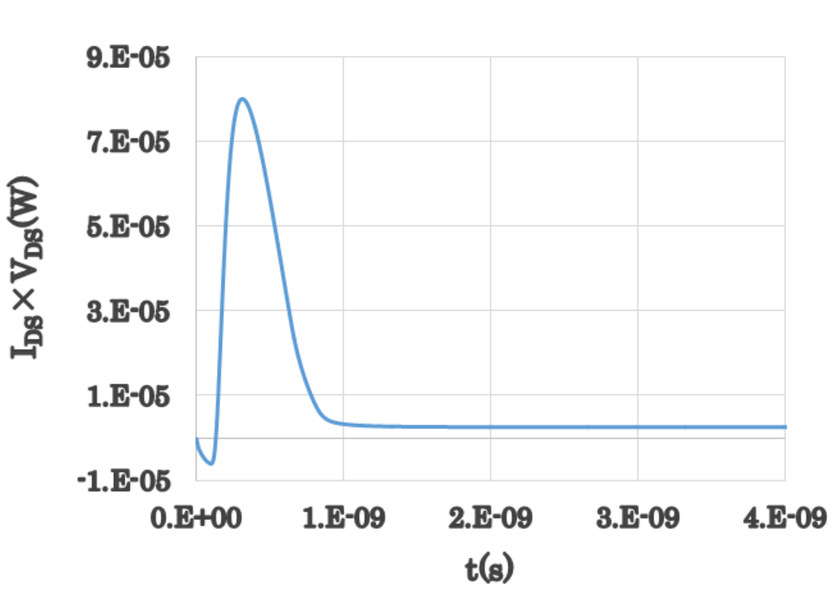




Power dissipation during Turn-on

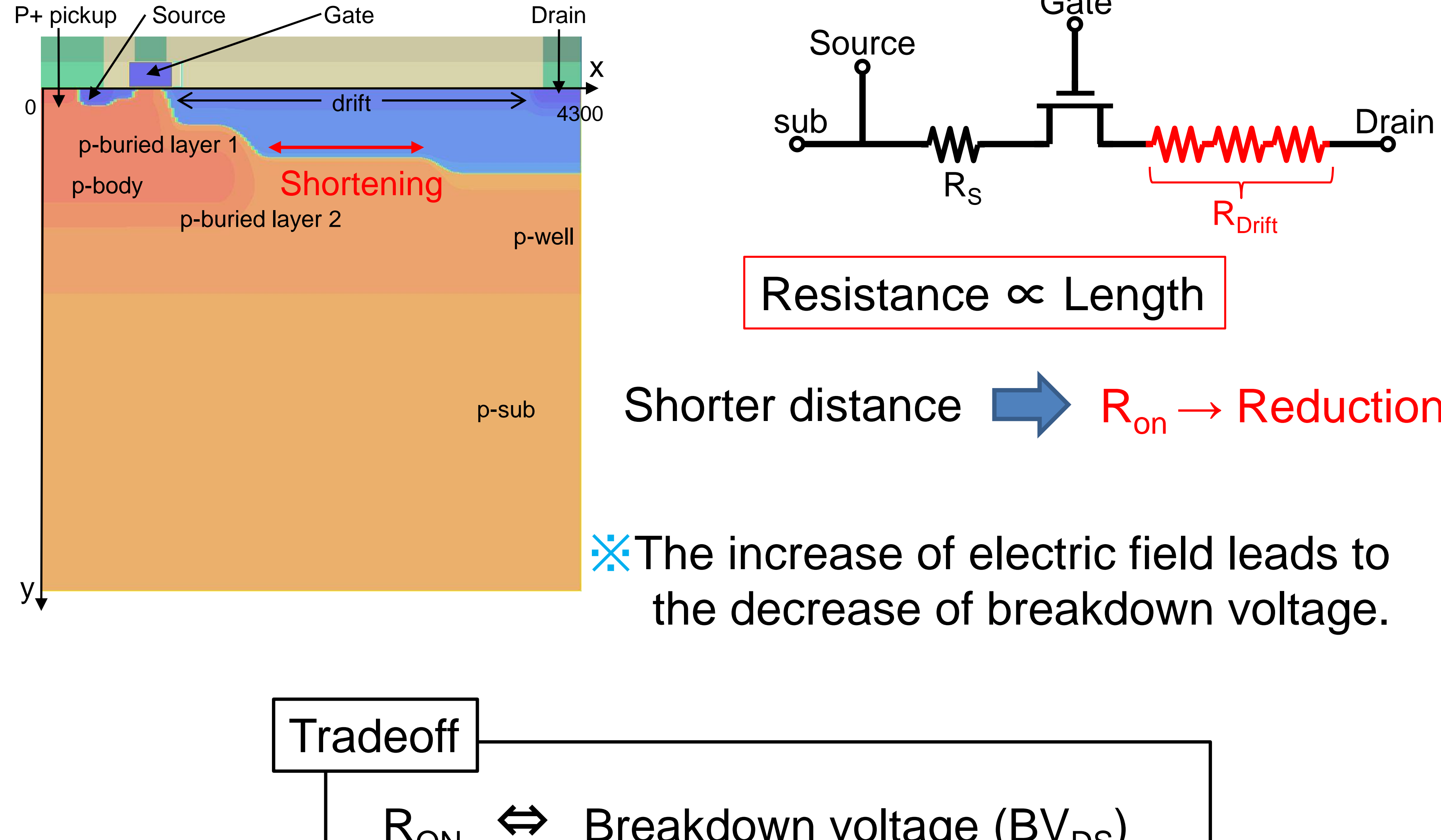


Optimized



App.

Shorter Drift Region

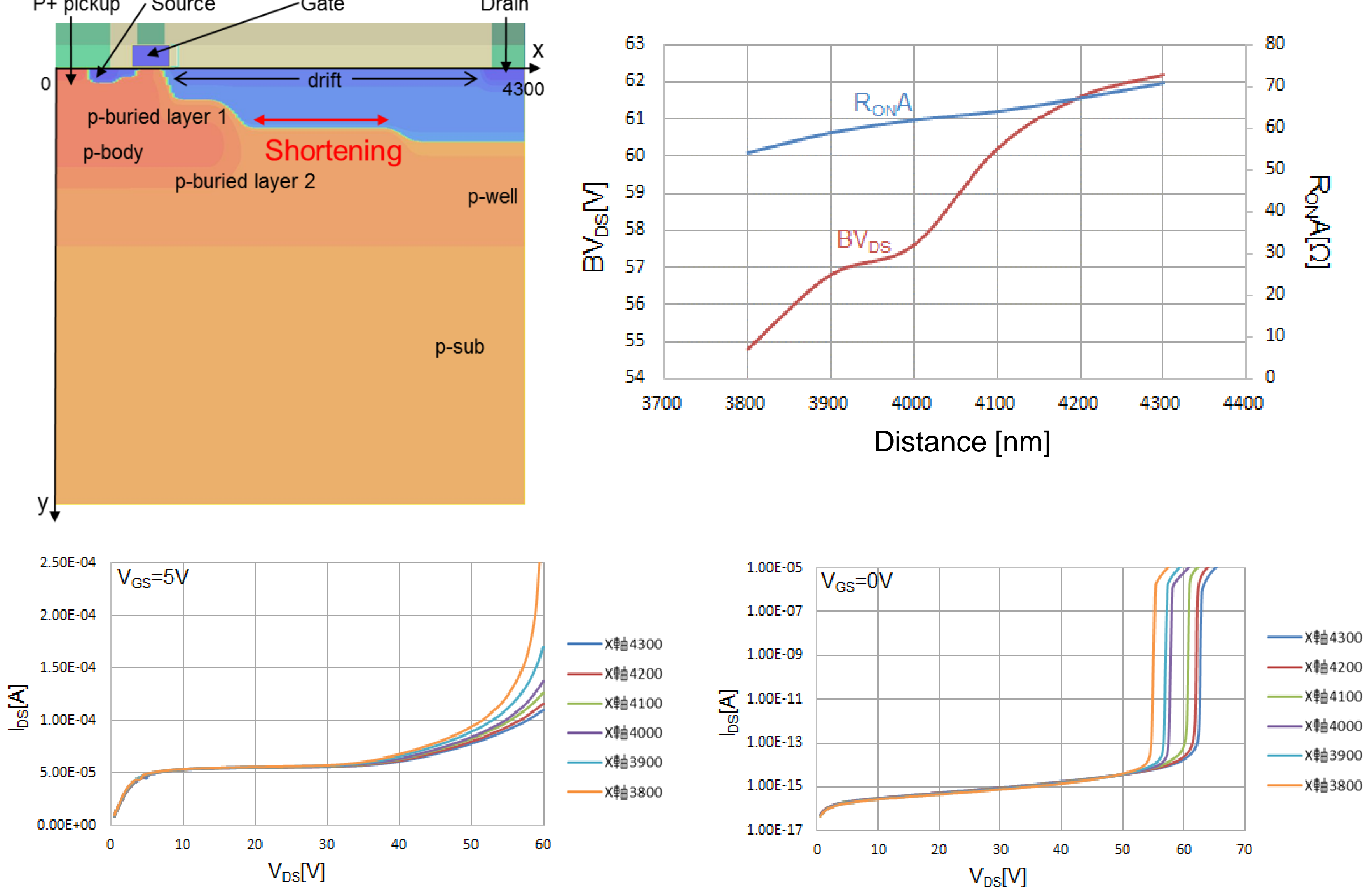


Tradeoff

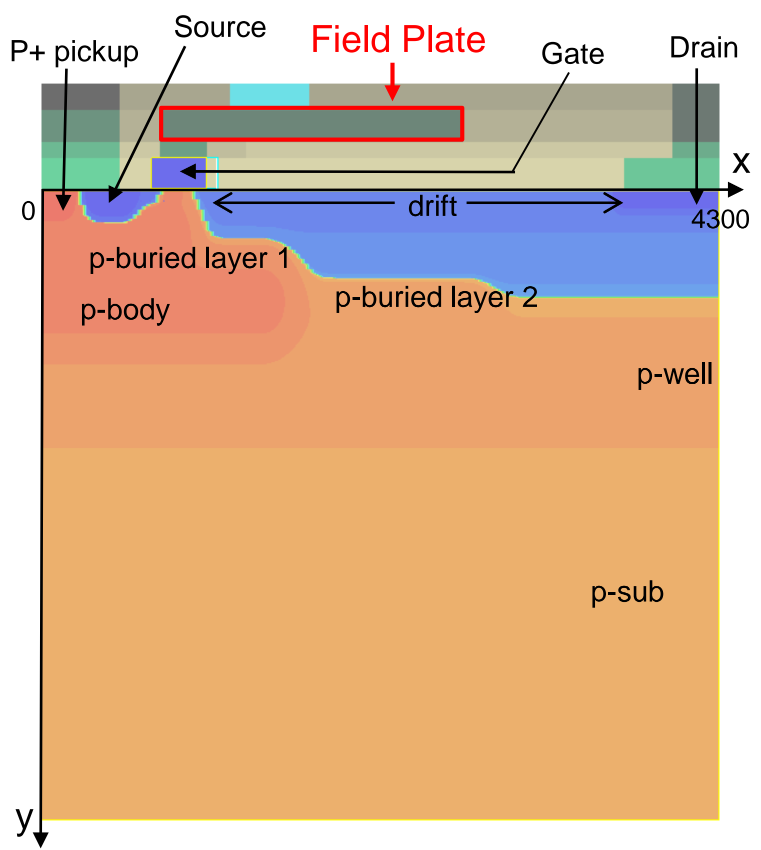
R_{ON} ⇔ Breakdown voltage (BV_{DS})

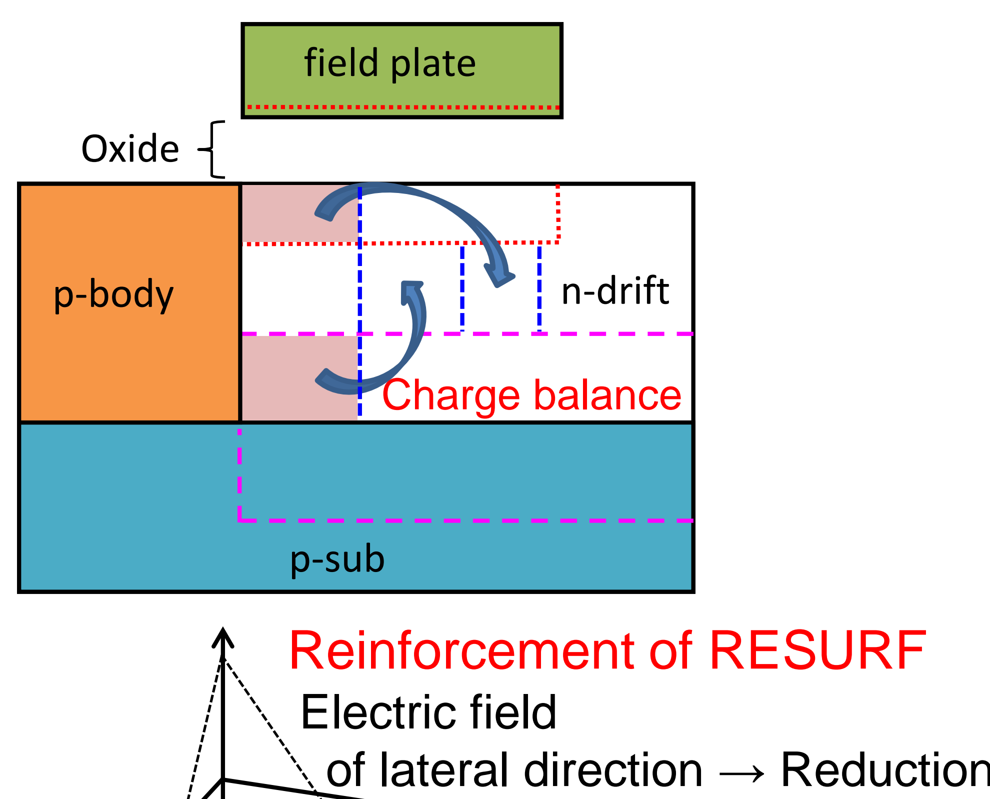
App.

Shorter Drift Region



Field Plate (FP)





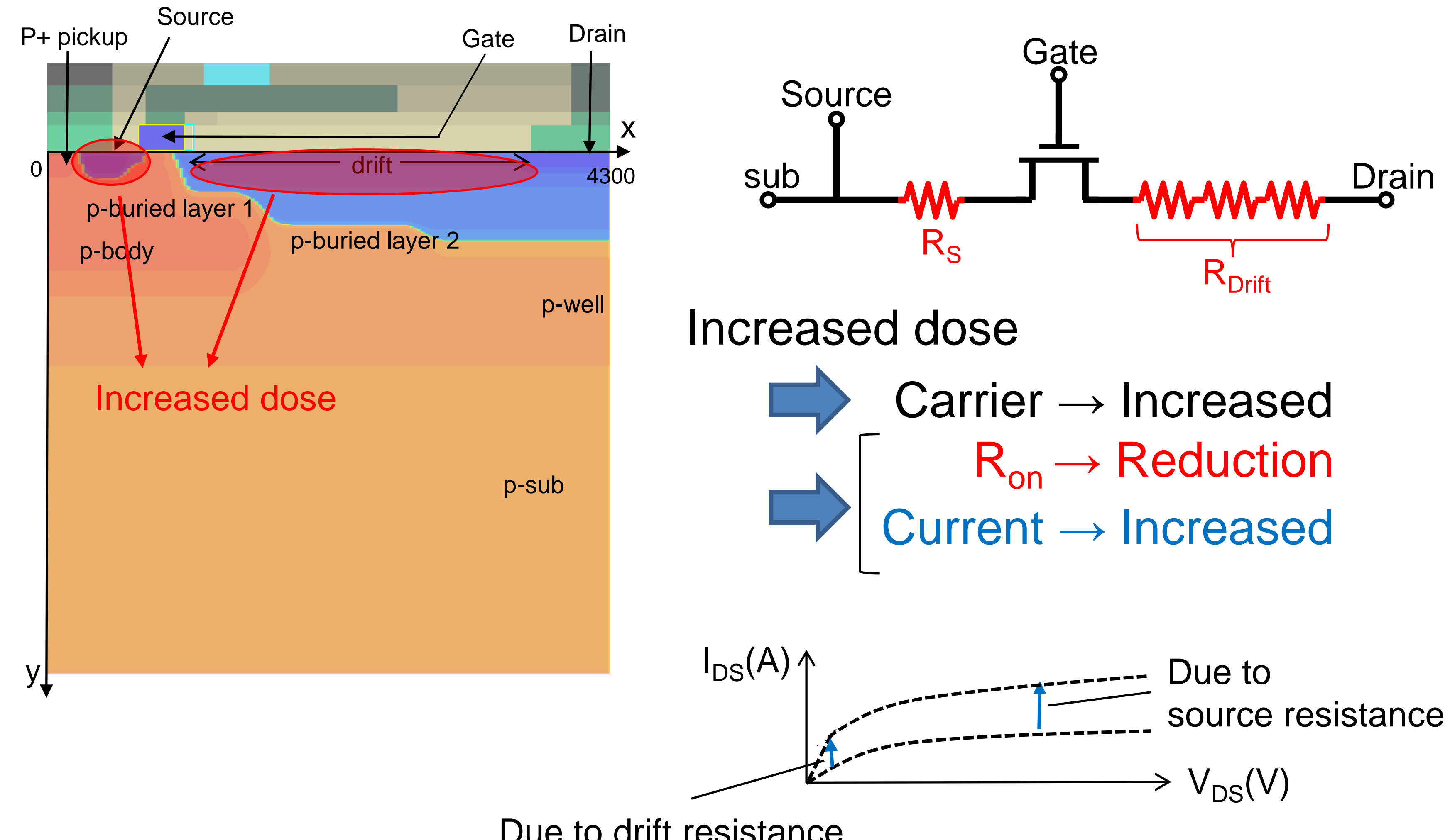
※ The increase of the parasitic capacitance due to the FP enhances RESURF effect, and the input capacitance as well.

Tradeoff

RESURF ⇔ Input capacitance

App.

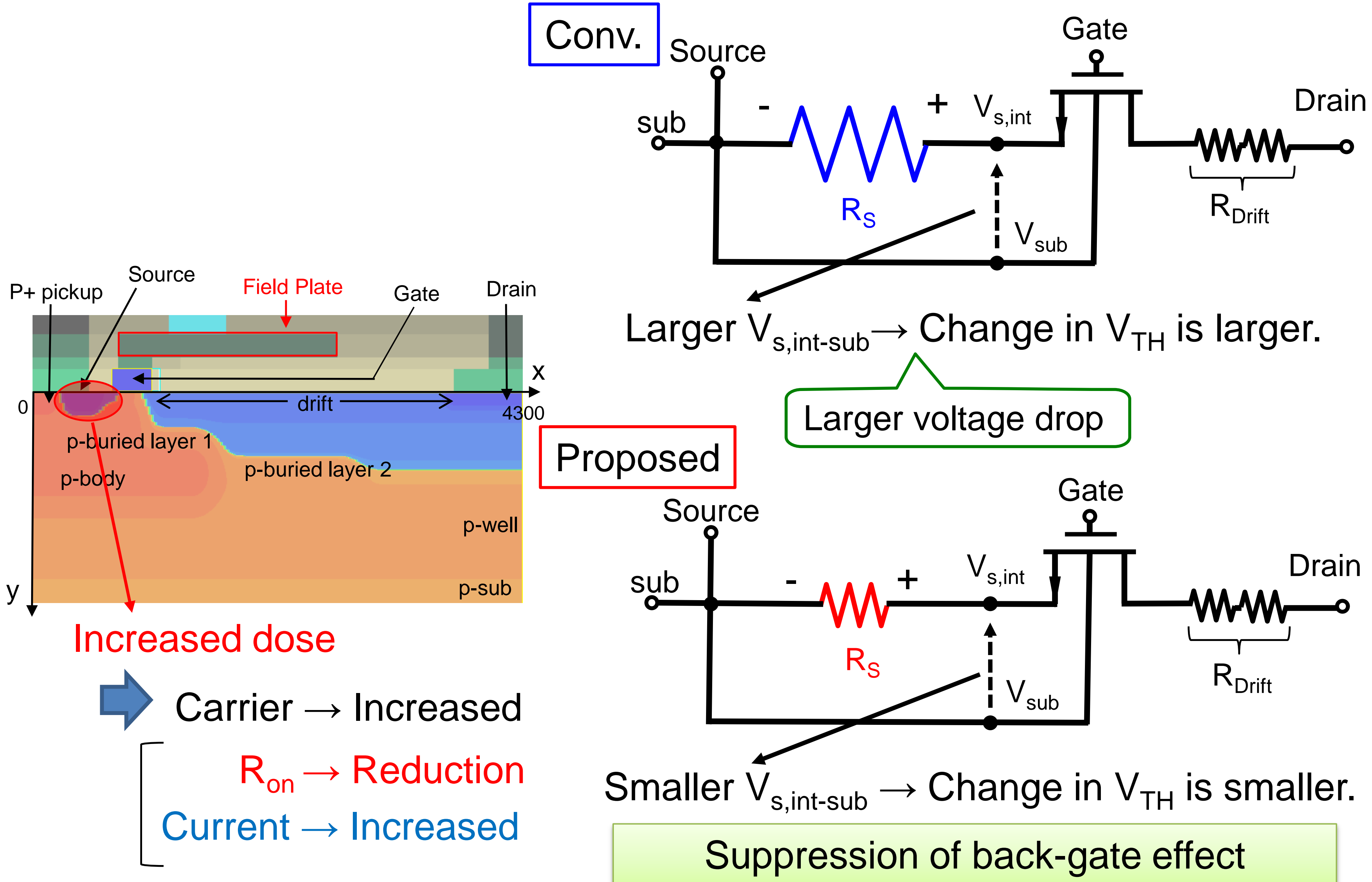
Increased Source & Drift Dose



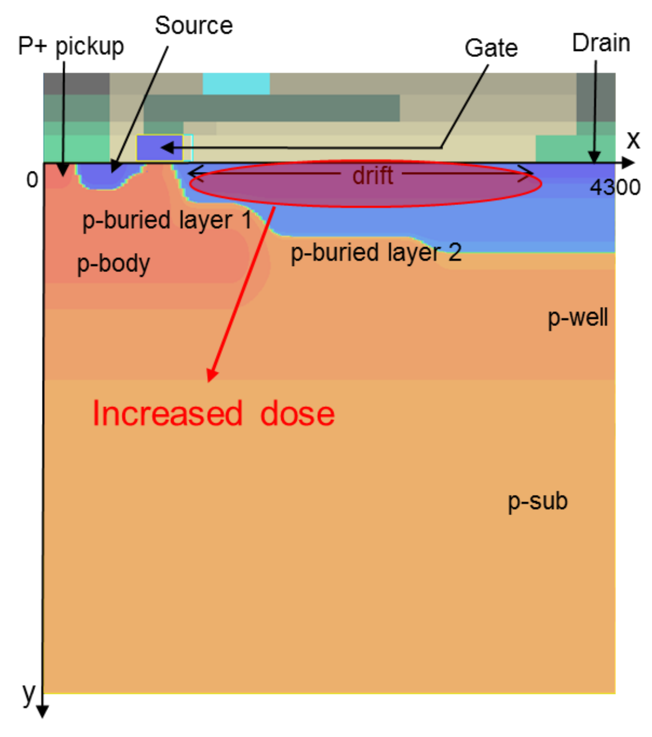
※ Suppression of back-gate effect

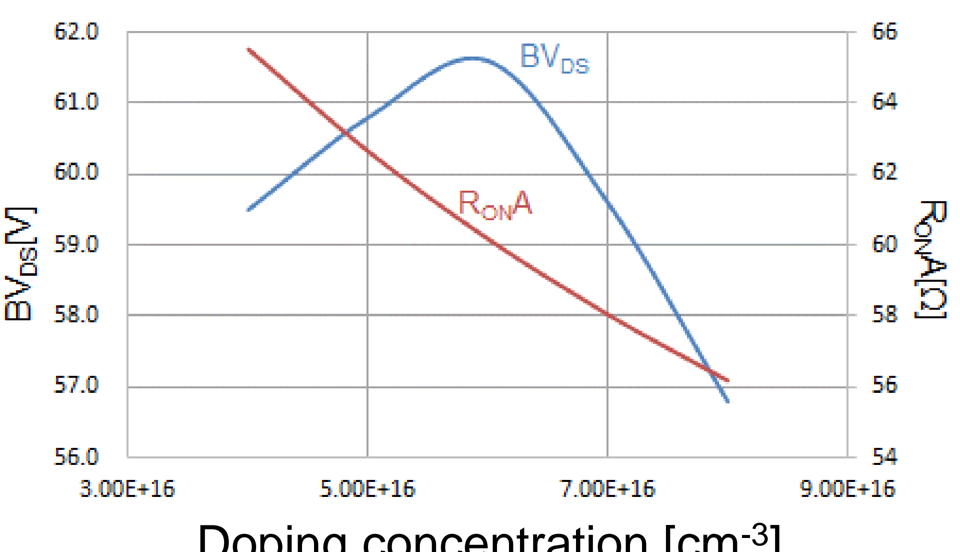
App.

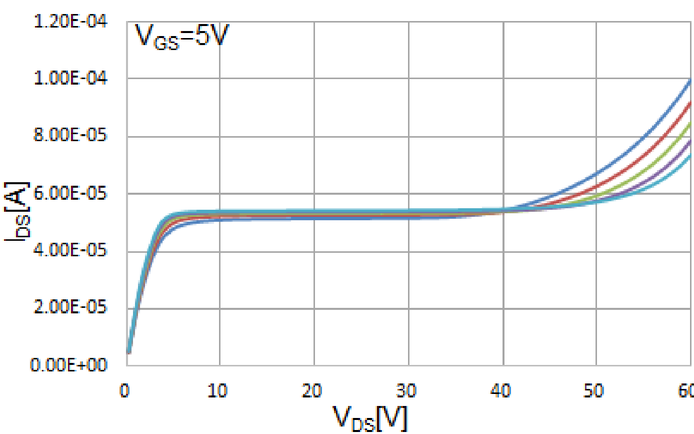
Increased Source Dose

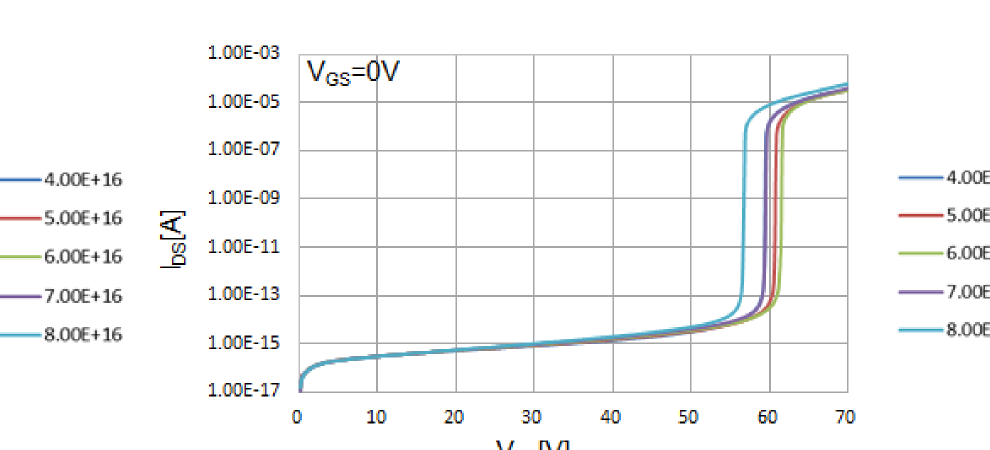


Increased Drift Dose





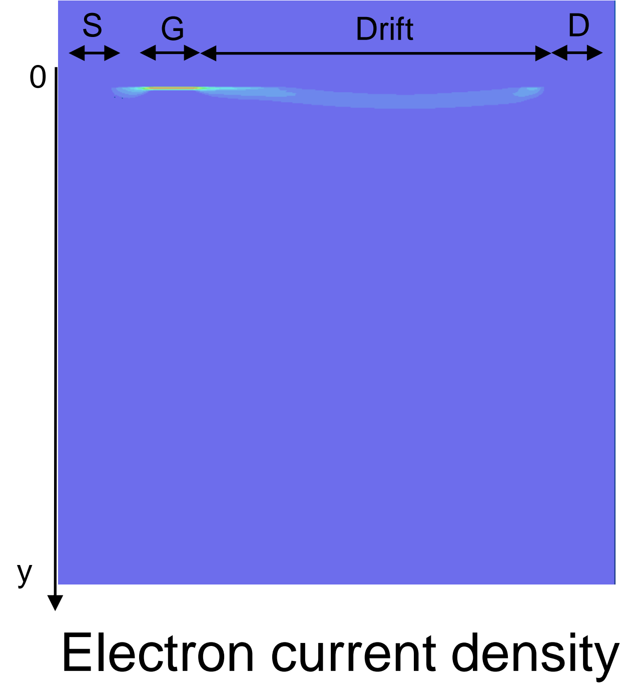




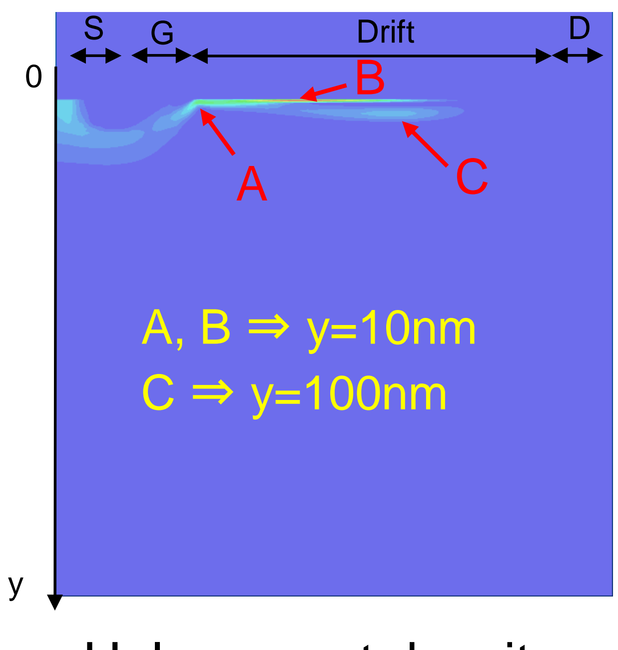
App.

Current Density Profiles of Optimized LDMOS

V_{DS}=40V, V_{GS}=5V



Electron current density

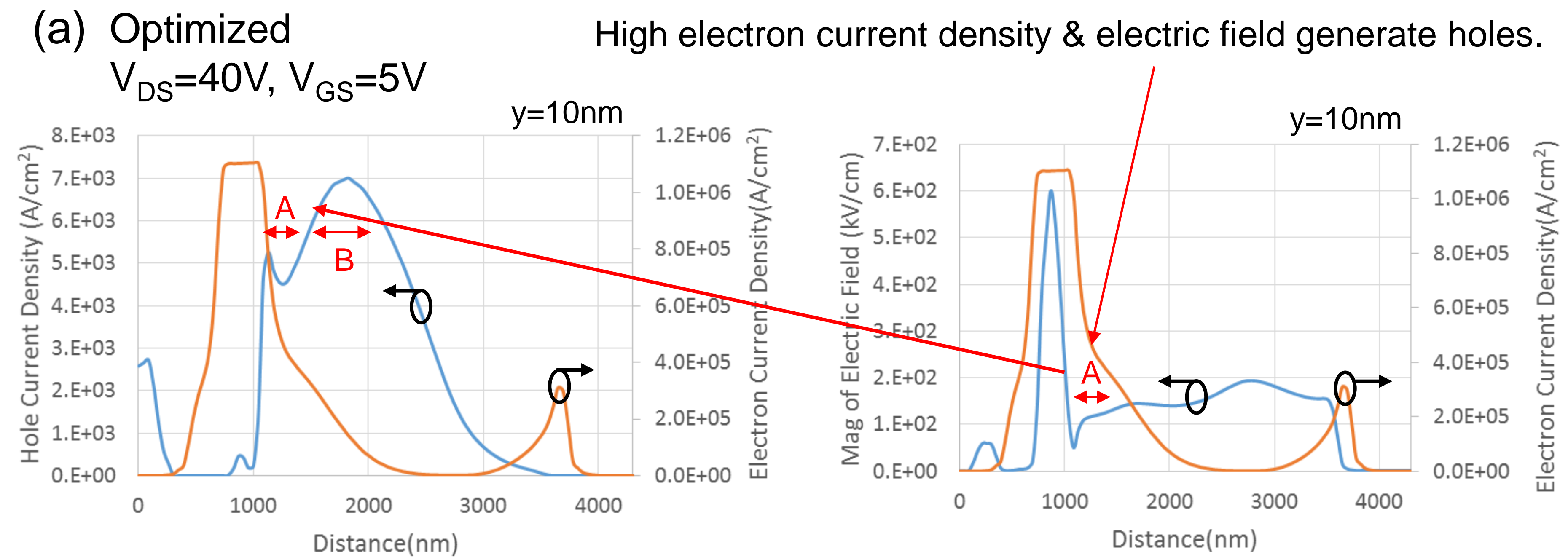


Hole current density

The electron current flows in a deep drift region.

The high hole current density occurs in surface "A" and "B", and deep "C" regions.

App. Hole/Electron Current Density & Electric Field Profiles



The hot carriers generated in the "A" region would degrade MOSFET characteristics.

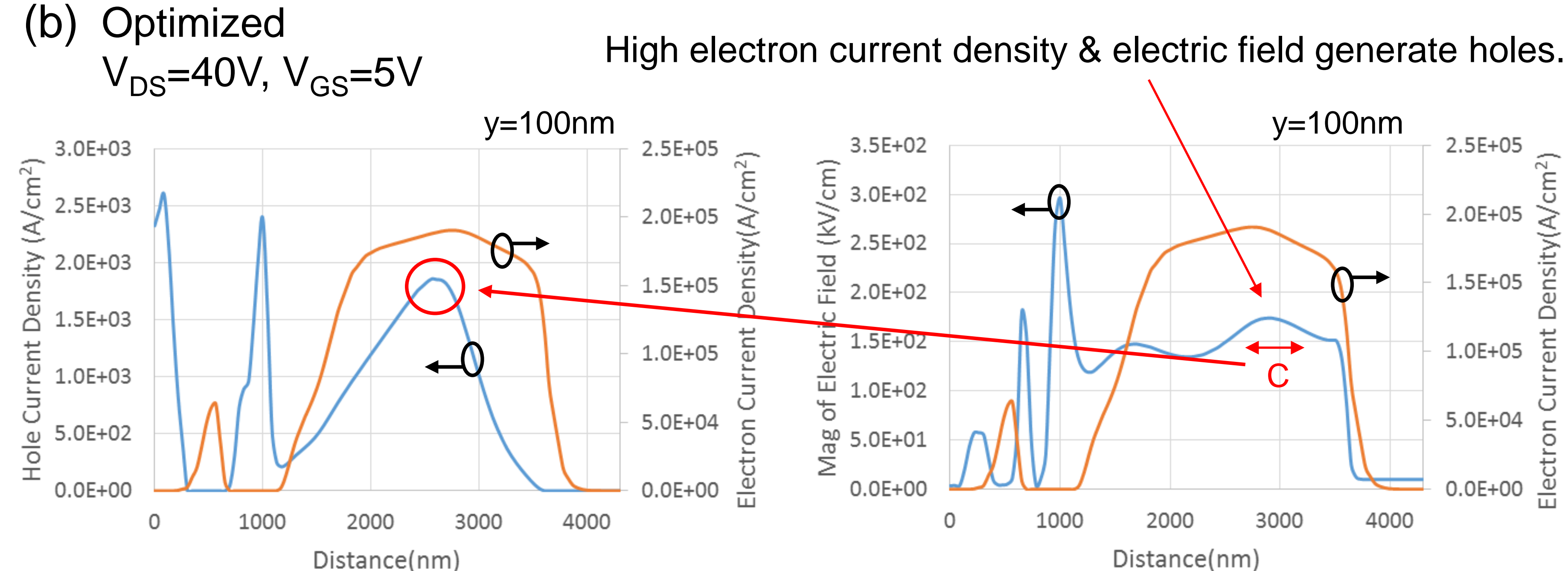
The holes in the shallow "B" region mainly comes from the deep "C" region.

Hole current by impact ionization
$\propto$(electron current) × (electric field) × exp(-A/electric field)

App.

Hole/Electron Current Density & Electric Field Profiles

(b) Optimized
V_{DS}=40V, V_{GS}=5V



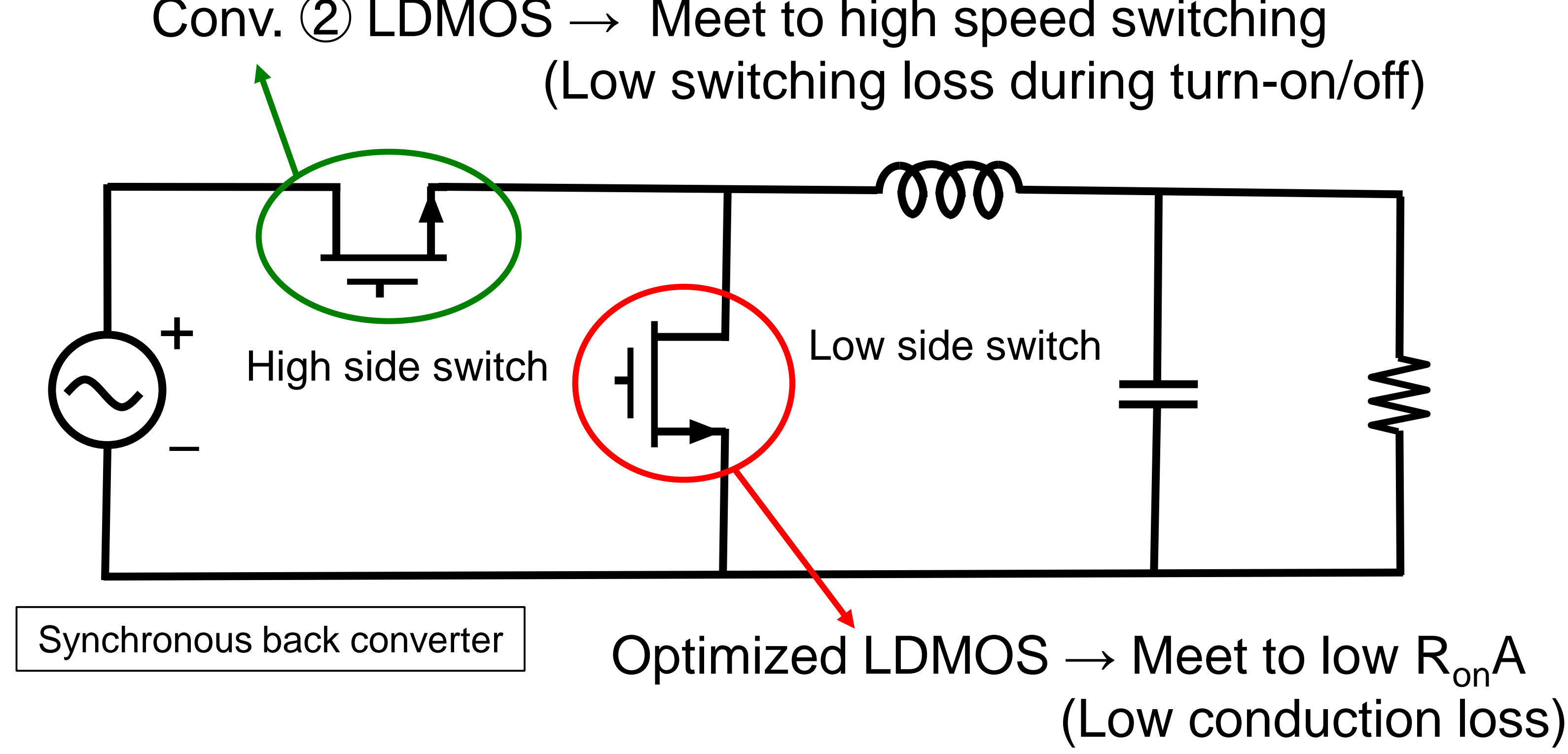
Enhanced impact ionization occurs in the “C” region.

A part of the holes in the deep “C” region flows to the surface “B” region.

Hole current by impact ionization
∝(electron current)×(electric field)×exp(-A/electric field)

App.

Example of Conv. ② & Optimized LDMOS



	$R_{on}A$ [mΩmm²]	Q_g/A [nC/mm²]	Dissipation
Conv. ②	69.3	1.49	Low (Switching frequency > 10MHz)
Optimized	44.8	3.13	Low (Switching frequency < 10MHz)

App.

Q1. 耐圧などはシミュレーションでどれほどの精度があるのか。

A1. We used a device simulator, DESSERT. This simulator can analyze device characteristics with high precision using latest and proven physical models. So, simulation results can be basically accurate.

Q2. 実際に作ったらどうか。

A2. The LDMOS can be made based on a conventional 0.35μm CMOS process. So, the fabrication of the LDMOS would not be complicated.

Q3.製造のときにフィールドプレートや層のズレがあると思うが、耐圧とかは下がらないのか。

A3. If the amount of misalignment for the field plate and p-buried layers is less than ±10%, the value of the breakdown voltage remains almost constant.

Ｑ＆Ａ 発表日:2016/10/27

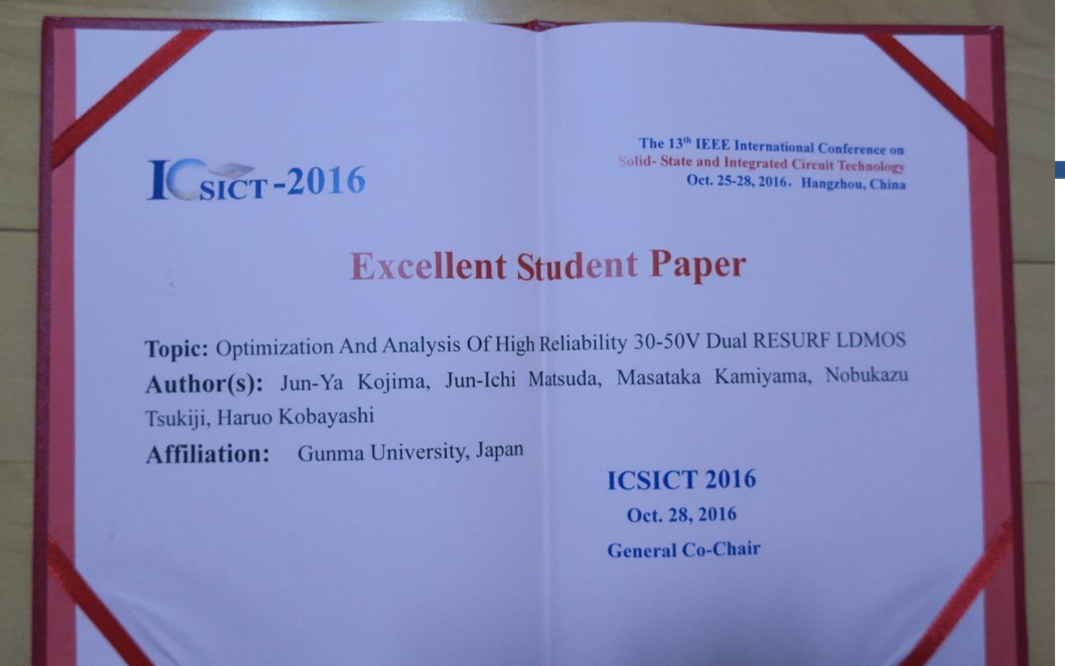
Q1: p.11の下の画像は実測なのか？

A1: 実測ではない。シミュレーションのみの結果である。

Q2: p.11に”good ESD performance“とあるが、なぜか？

A2: バルクでブレークダウンが発生しており、ゲートでは発生していないから。

(上のように答えましたが、質問者は何度も質問し、その質問を私は正確に聞き取ることができませんでした。発表後、築地さんに尋ねたところ、質問者はBVDSのことをD-S間ではなくG-S間と勘違いしていたそうです。)


ICSICT-2016
The 13th IEEE International Conference on
Solid- State and Integrated Circuit Technology
Oct. 25-28, 2016. Hangzhou, China
Excellent Student Paper
Topic: Optimization And Analysis Of High Reliability 30-50V Dual RESURF LDMOS
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