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Catalunya, Spain

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15:00-15:30

Conference Room: Goya

Successive Approximation Time-to-Digital Converter with Vernier-level Resolution

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Kobayashi Laboratory

群馬大学 GUNMA UNIVERSITY

Contents

- Research Objective
- TDC Application to LSI Testing Technology
- 4 Types of TDCs Developed at Gunma Univ.
  - ✓ Flash-type TDC
  - ✓ Gray code based TDC
  - ✓ SAR-typeTDC
  - ✓ Delta-Sigma TDC
- Discussions and Conclusion

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Research Objective

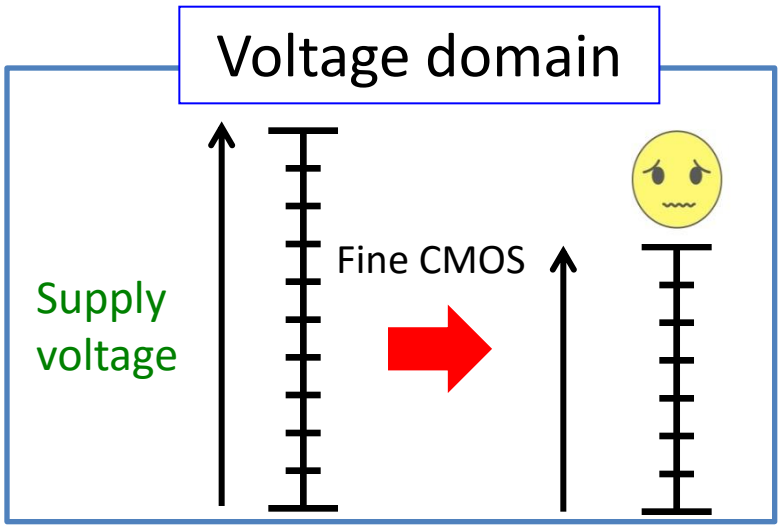
- Compare 4 types of Time-to-Digital Converters (TDCs) developed at the presenter's lab for LSI testing technology.

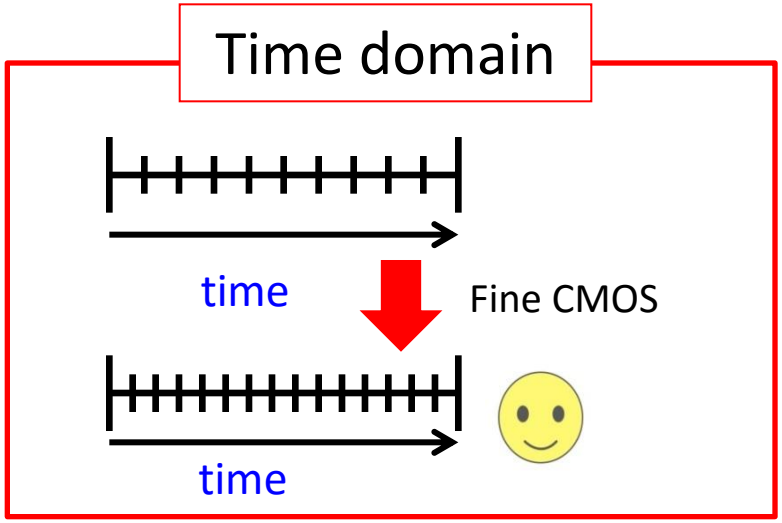
- Especially present details of the SAR TDC architecture and its calibration method.

Research Background

Advanced CMOS VLSI

- Low power-supply voltages
- Fast switching speeds





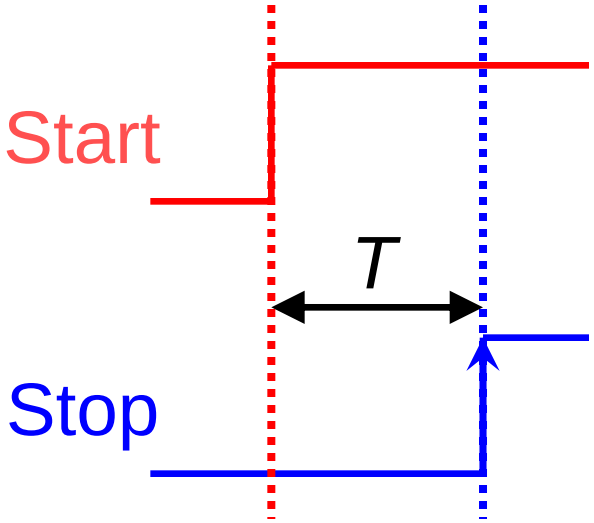
A Time-to-Digital Converter (TDC) provides a digital output proportional to the time between two clock transitions.

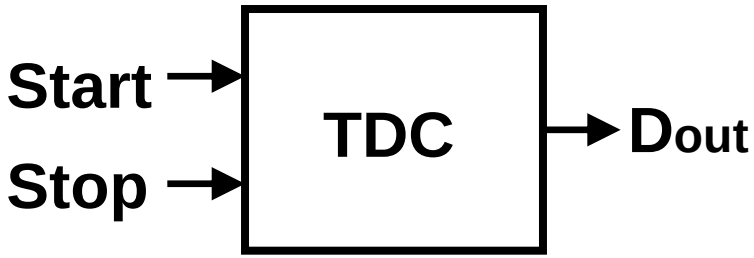
The TDC is a key component in time-domain analog circuits,

（e.g. Sensor Interfaces, All-Digital PLLs, ADCs, .. ）

Time to Digital Converter（TDC）

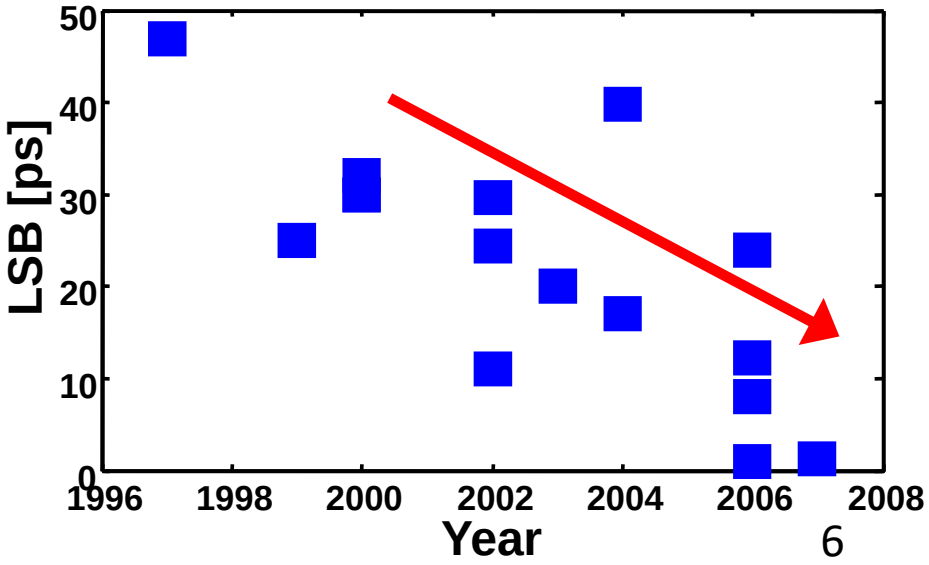
- time interval → Measurement → Digital value





- Key component of Time-domain analog circuit
- Higher resolution can be obtained with scaled CMOS

Higher resolution with CMOS scaling



Time Domain Analog Circuit Features

- Voltage domain:

  Signal range : Up to power supply voltage

  Time domain:

  Signal range : Time continues indefinitely

  ⇒ Large dynamic range

- Time domain analog circuit :

  Binary amplitude（Vss, Vdd)

  ⇒ Can consists of digital circuit

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ATE System and TDC

- "Timing" is very important in ATE systems
- Many High-performance TDCs are used there.

Such as

for Clock timing, jitter measurements

[1] K. Yamamoto,at. el. (Advantest Corp.),
"Multi Strobe Circuit for 2.133 GHz Memory Test System,"
IEEE International Test Conference, Paper 6.1 (2006).

Analog/Mixed-Signal BIST, BOST

- TDC can be used for BIST , BOST
- BIST, DFT

Chip design time maybe longer	Long time-to-market
Chip may be larger	Costly
Difficult to assure its reliability	Should be simple

- BOST

Design/implementation after tape out Attractive

- I have a feeling

Japanese companies prefer BOST,

US companies prefer BIST.

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4 Types of TDCs

	Clocks Under Test	Measurement Time	Time Resolution	Circuit	FPGA
Flash-type	Single event ○	Short ○	Coarse ✕	Large ✕	Digital ○
Gray code based	Single event ○	Short ○	Coarse ✕	Small ○	Digital ○
SAR-type	Repetitive clock △	Middle △	Middle △	Small ○	Digital ○
Delta-Sigma type	Repetitive clock △	Long ✕	Fine ○	Small ○	Small Analog △

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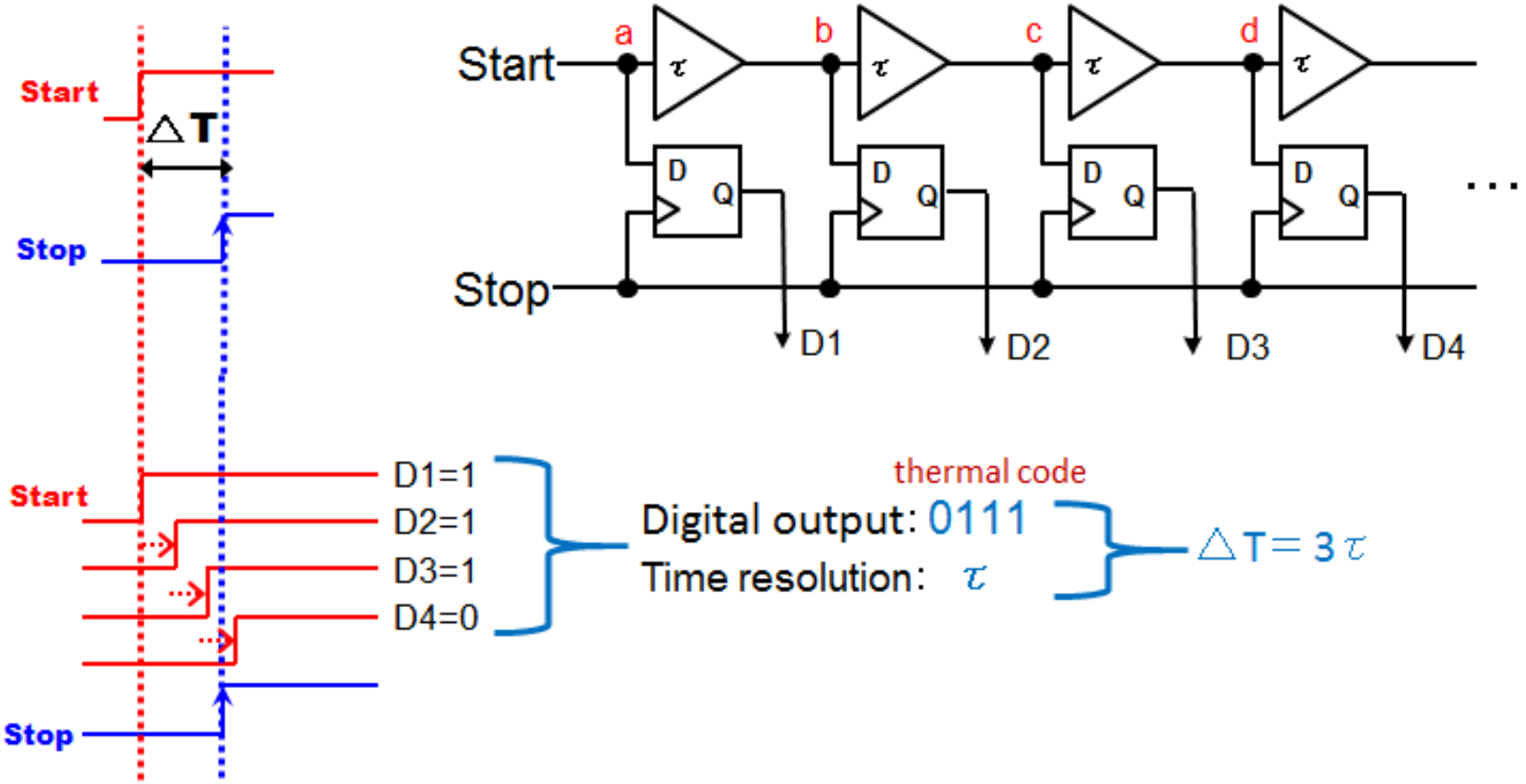
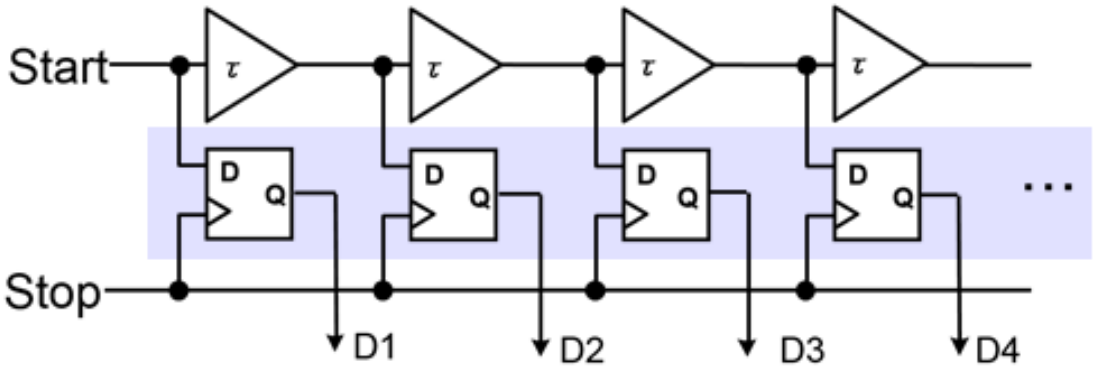
Flash-type TDC



Flash-type TDC Evaluation

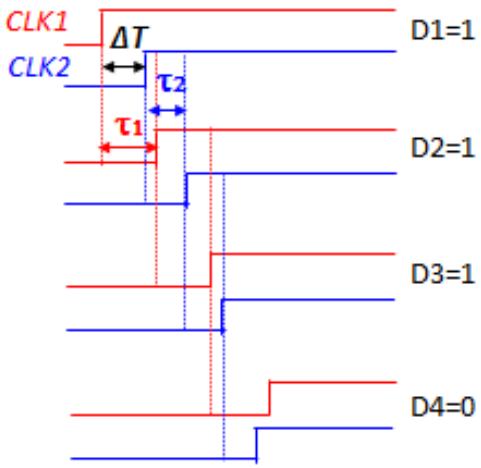


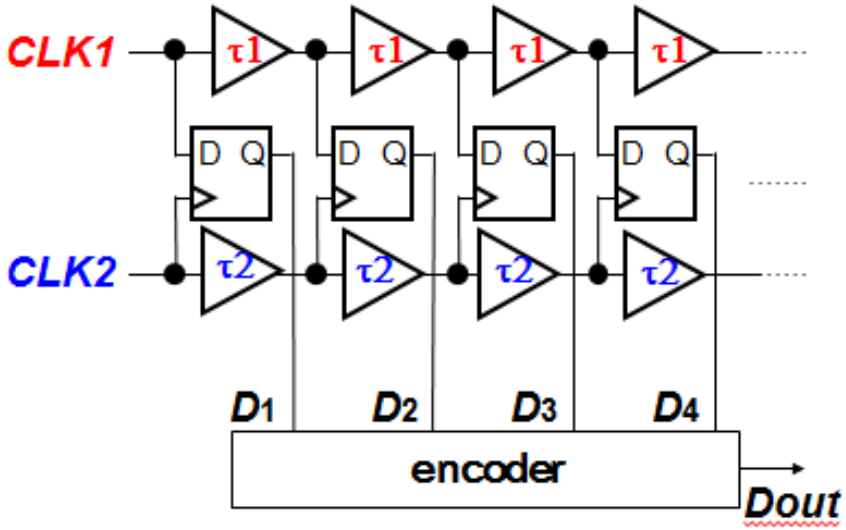
# of buffers : $2^n - 1$ (10bit→1023)

# of DFFs: $2^n - 1$ (10bit→1023) → Large circuit → Large power

Time resolution: buffer gate delay τ → Too coarse

Vernier-type TDC





Delay: $\tau_1 > \tau_2$

Time resolution : $\tau_1 - \tau_2$

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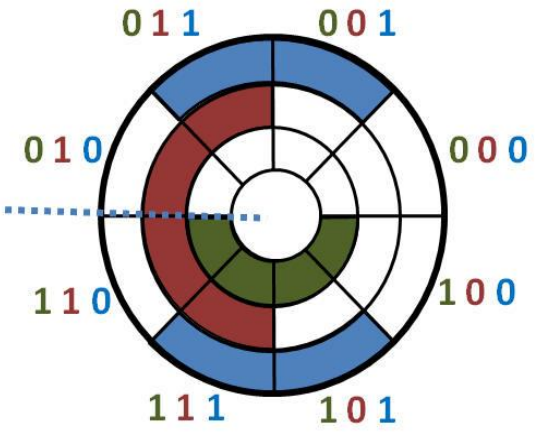
Concept of Gray code

Gray code is a binary numeral system
where two successive values differ in only one bit.

4-bit Gray code vs. 4-bit Natural Binary Code

Decimal numbers	Natural Binary Code	4-bit Gray Code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

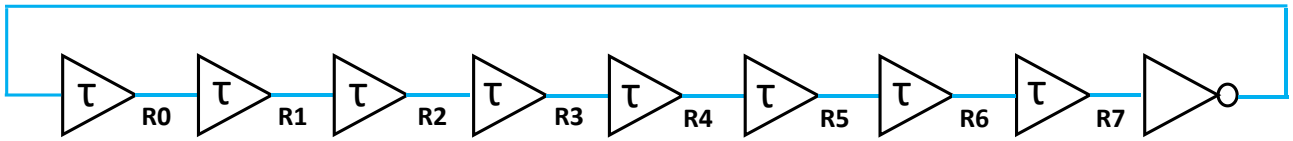


Frank Gray and A. L. Johnsrud in television booth. Behind the glass panels at sides and top are the photo-electric cells.

Gray code was invented by Frank Gray at Bell Lab in 1947

How to utilize Gray code in TDC

In a ring oscillator, between any two adjacent states, only one output changes at a time.



8-stage Ring Oscillator Output								4-bit Gray Code			
R0	R1	R2	R3	R4	R5	R6	R7	G3	G2	G1	G0
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	1	1
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	1	1	0
1	1	1	1	1	0	0	0	0	1	1	1
1	1	1	1	1	1	0	0	0	1	0	1
1	1	1	1	1	1	1	0	0	1	0	0
1	1	1	1	1	1	1	1	1	1	0	0
0	1	1	1	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	0
0	0	0	0	1	1	1	1	1	0	1	0
0	0	0	0	0	1	1	1	1	0	1	1
0	0	0	0	0	0	1	1	1	0	0	1
0	0	0	0	0	0	0	1	1	0	0	0

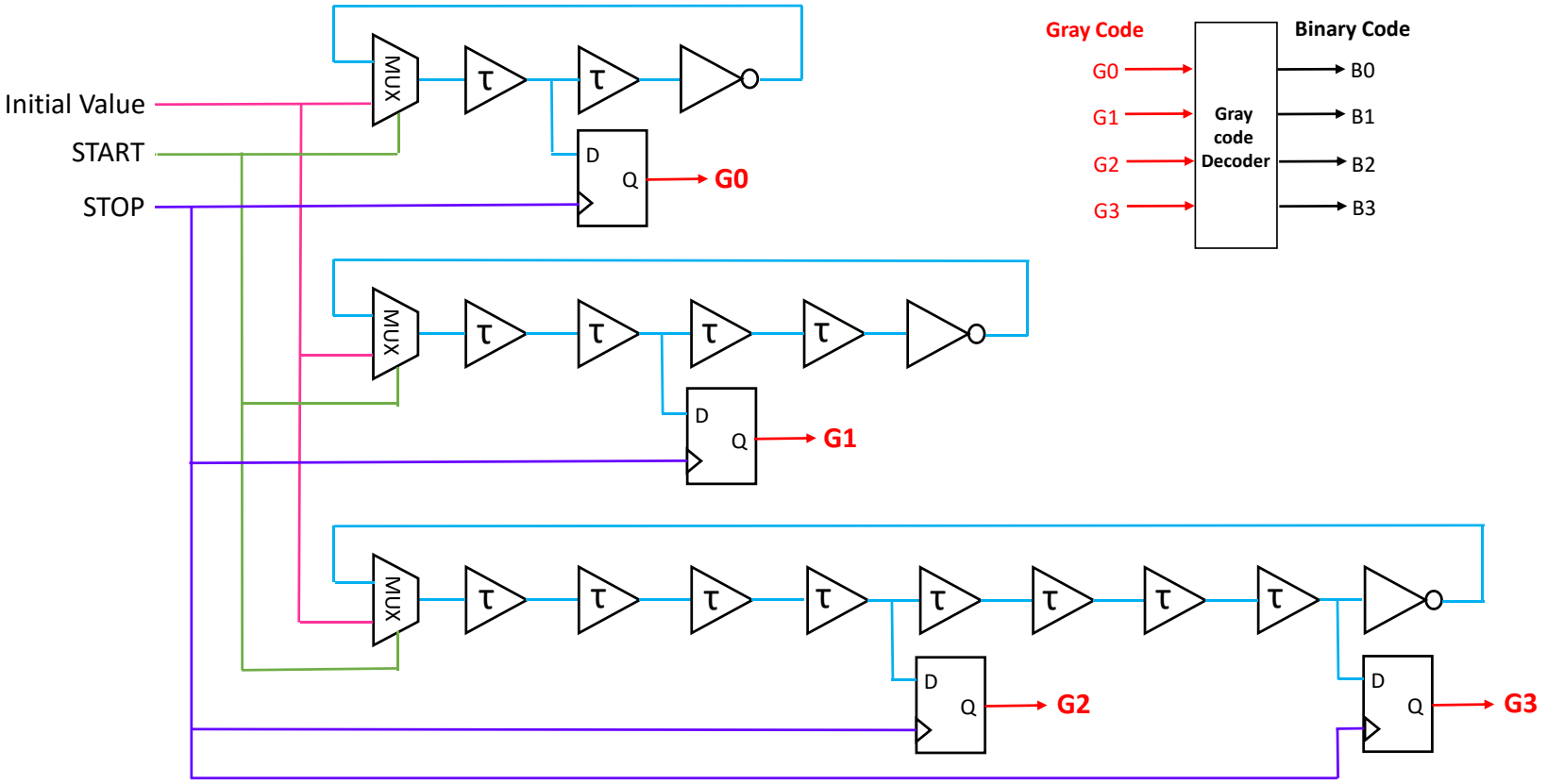
For any given Gray code, each bit can be generated by a certain ring oscillator.

Proposed 4-bit Gray code TDC

A large Flash TDC

Convert

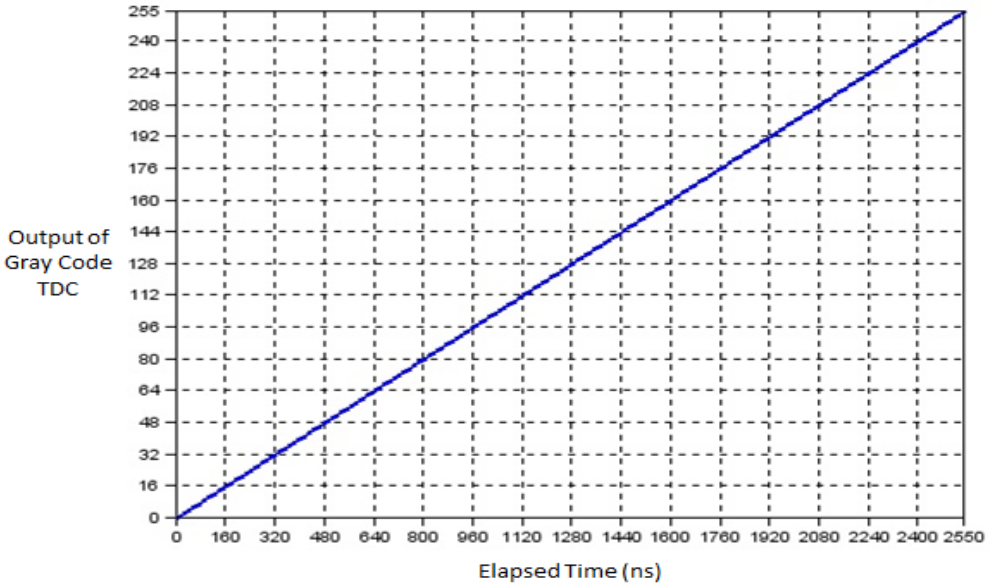
A set of smaller Flash TDCs performed in parallel



Proposed Gray code TDC architecture in 4-bit case

FPGA measurement results of 8-bit Gray code TDC

FPGA implementation of
Gray code TDC



Gray code TDC works with good linearity as expected

[1] C. Li, H. Kobayashi, "A Gray Code Based Time-to-Digital Converter Architecture and its FPGA Implementation", IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), Sendai, Japan (Aug. 26-28, 2015).

Flash TDC vs. Gray code TDC

	Number of delay cells	Number of DFFs	Maximum stage of RO
Gray code TDC	$2^n - 2$	n	2^{n-1}
Flash-type TDC	2^n	2^n	2^n

For large measurement range, the number of flip-flops in Gray code TDC decreases rapidly ($n \ll 2^n$)

Reduction of circuit complexity!!

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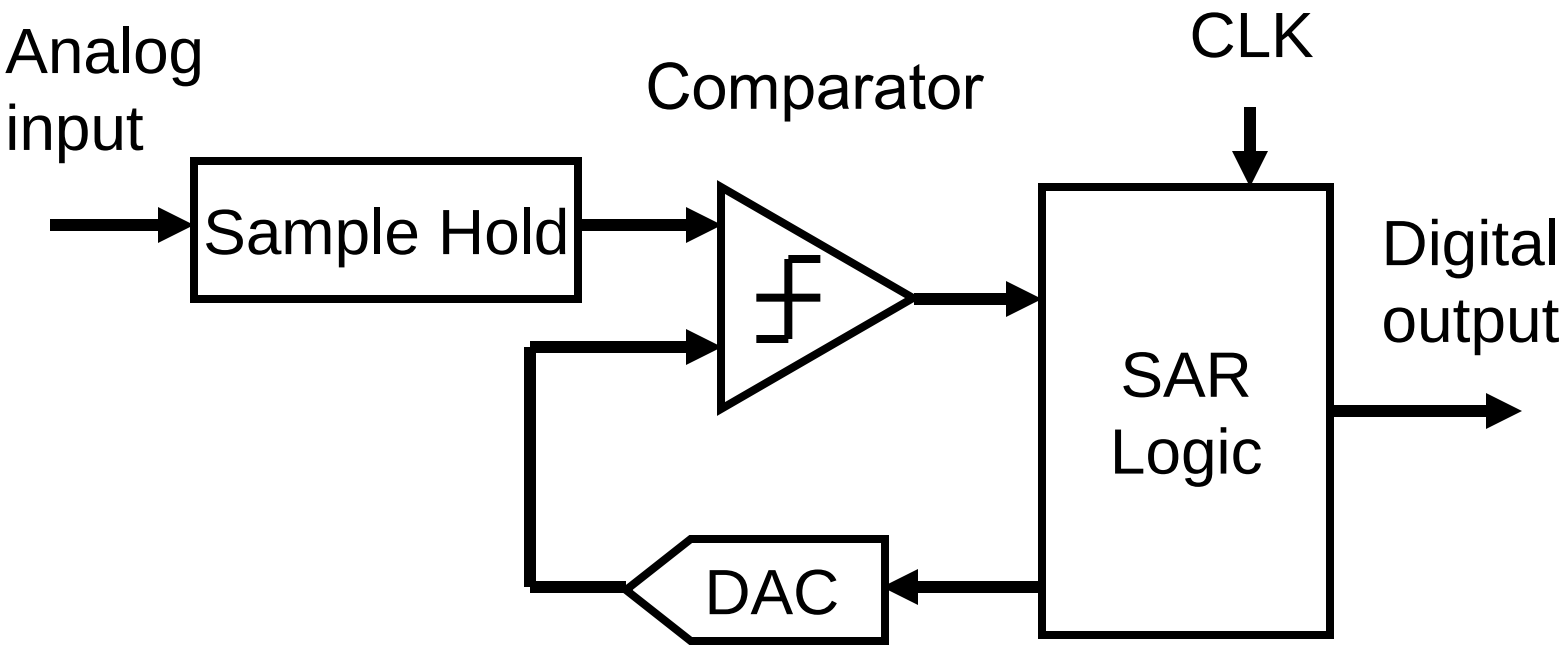
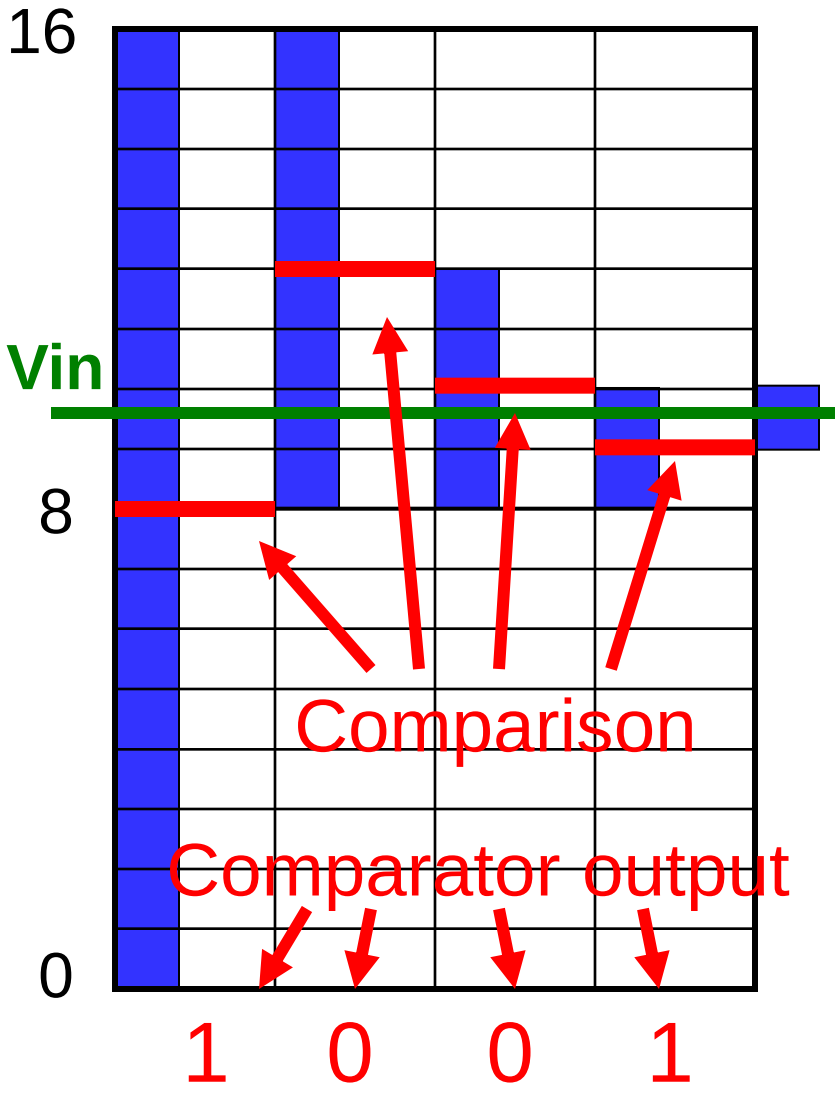
SAR ADC Block

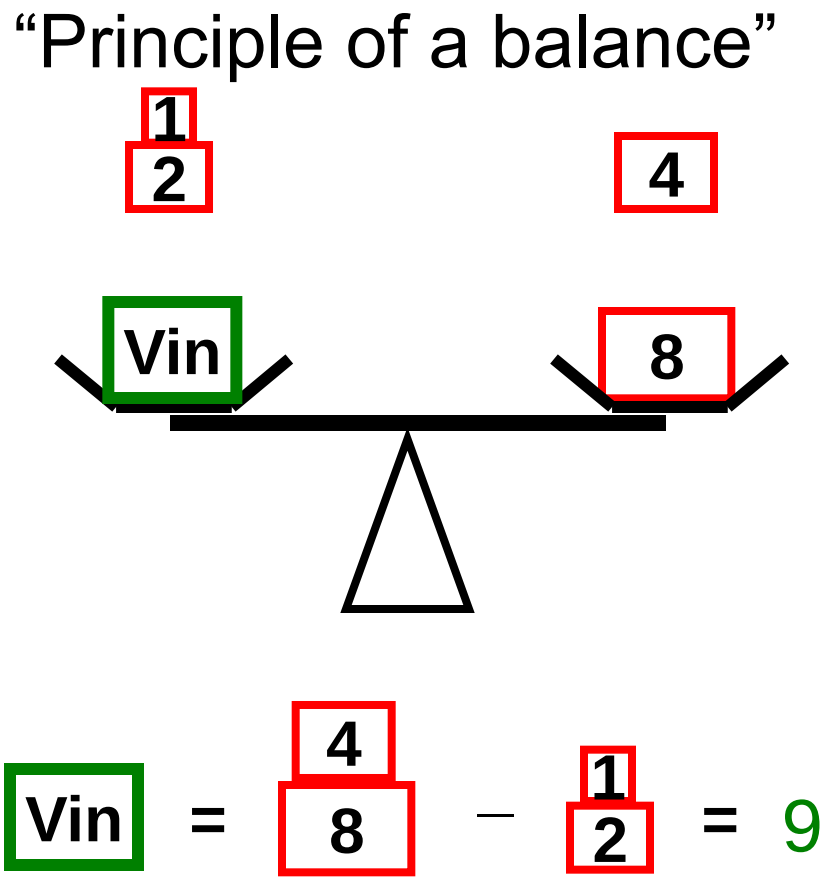


SAR ADC is digital centric.

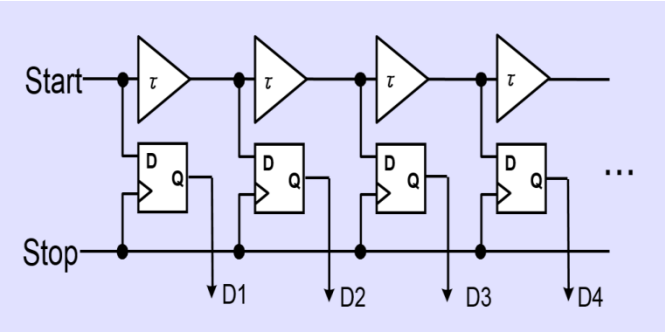
→ Suitable for fine CMOS implementation.

SAR ADC Operation

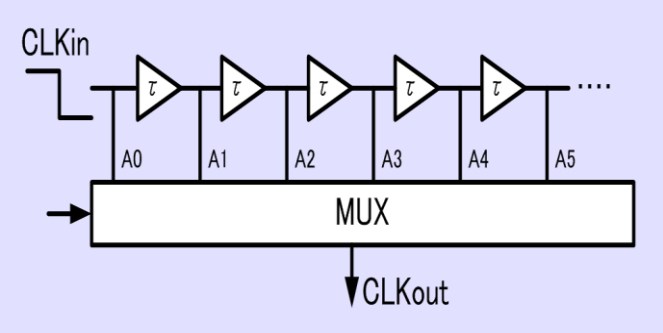




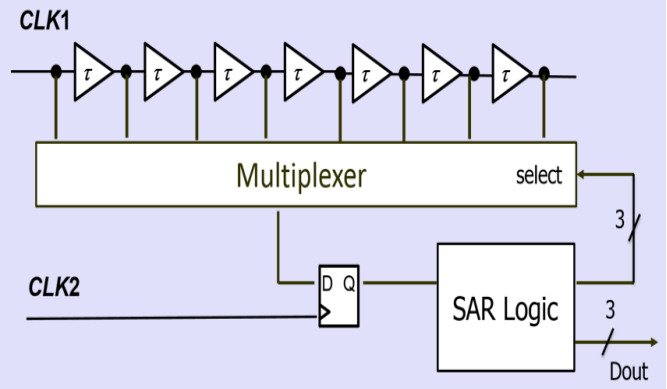
SAR TDC Configuration



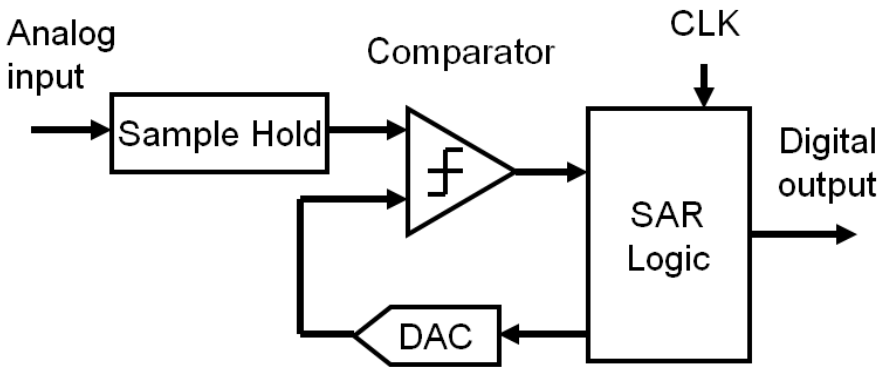
# of DFFs reduction

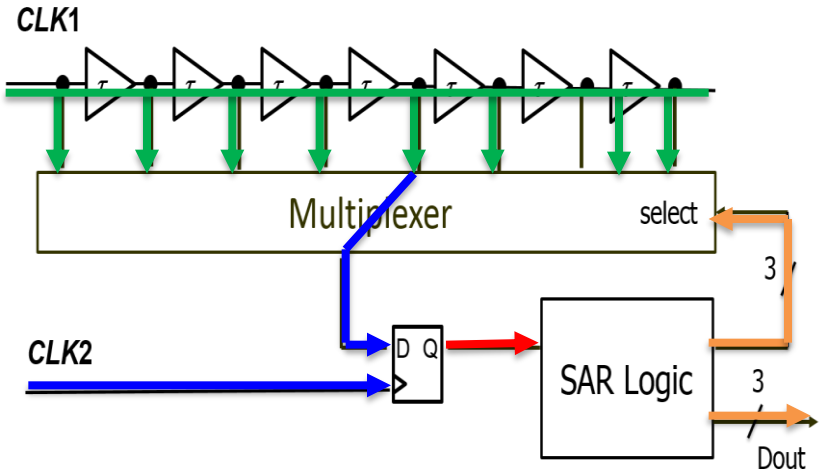


SAR Operation



SAR ADC versus SAR TDC

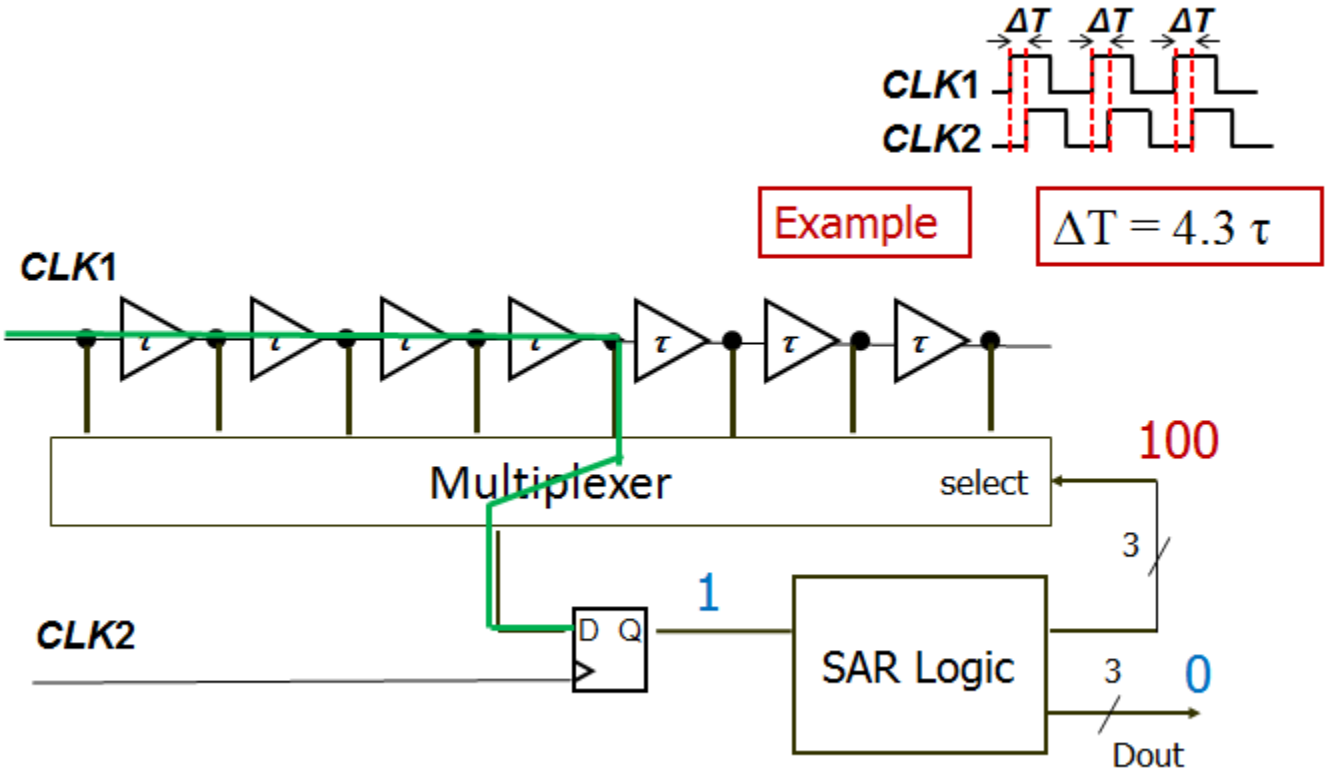




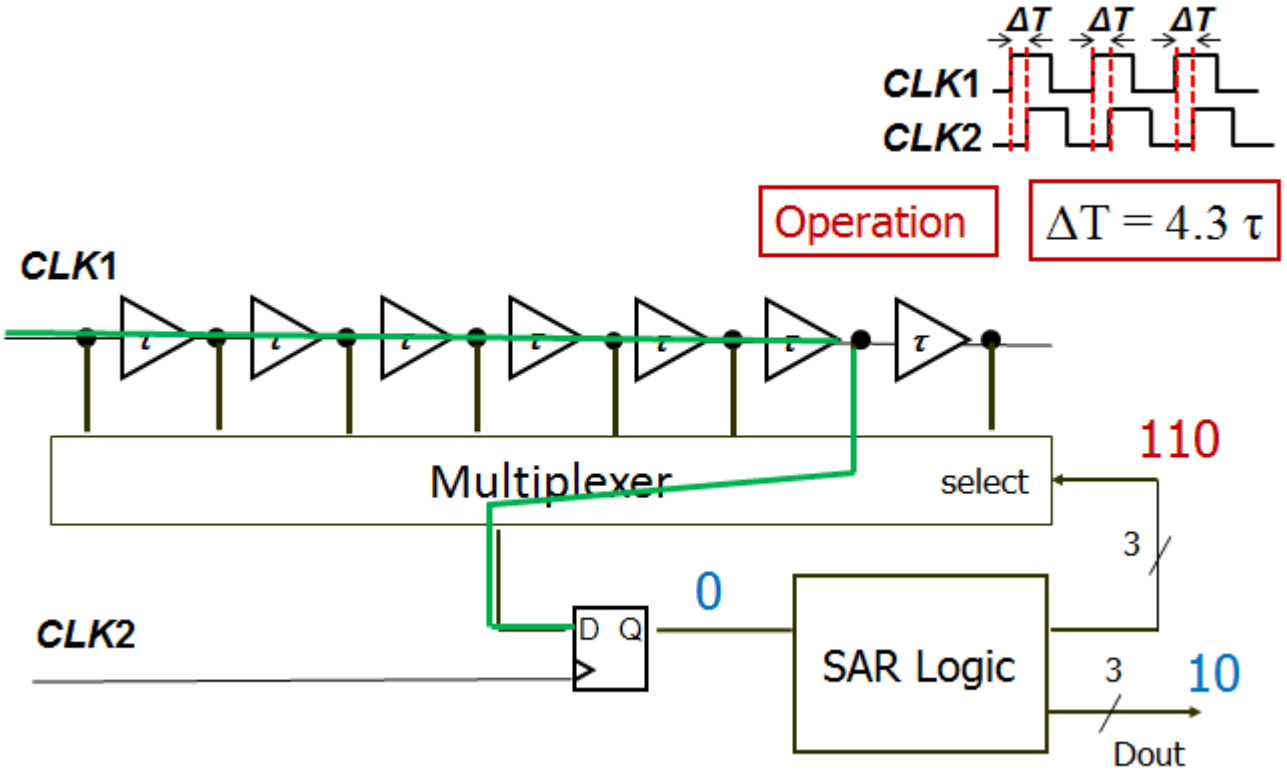
SAR ADC
- Comparator
- DAC

SAR TDC
- DFF
- Delay chain, MUX

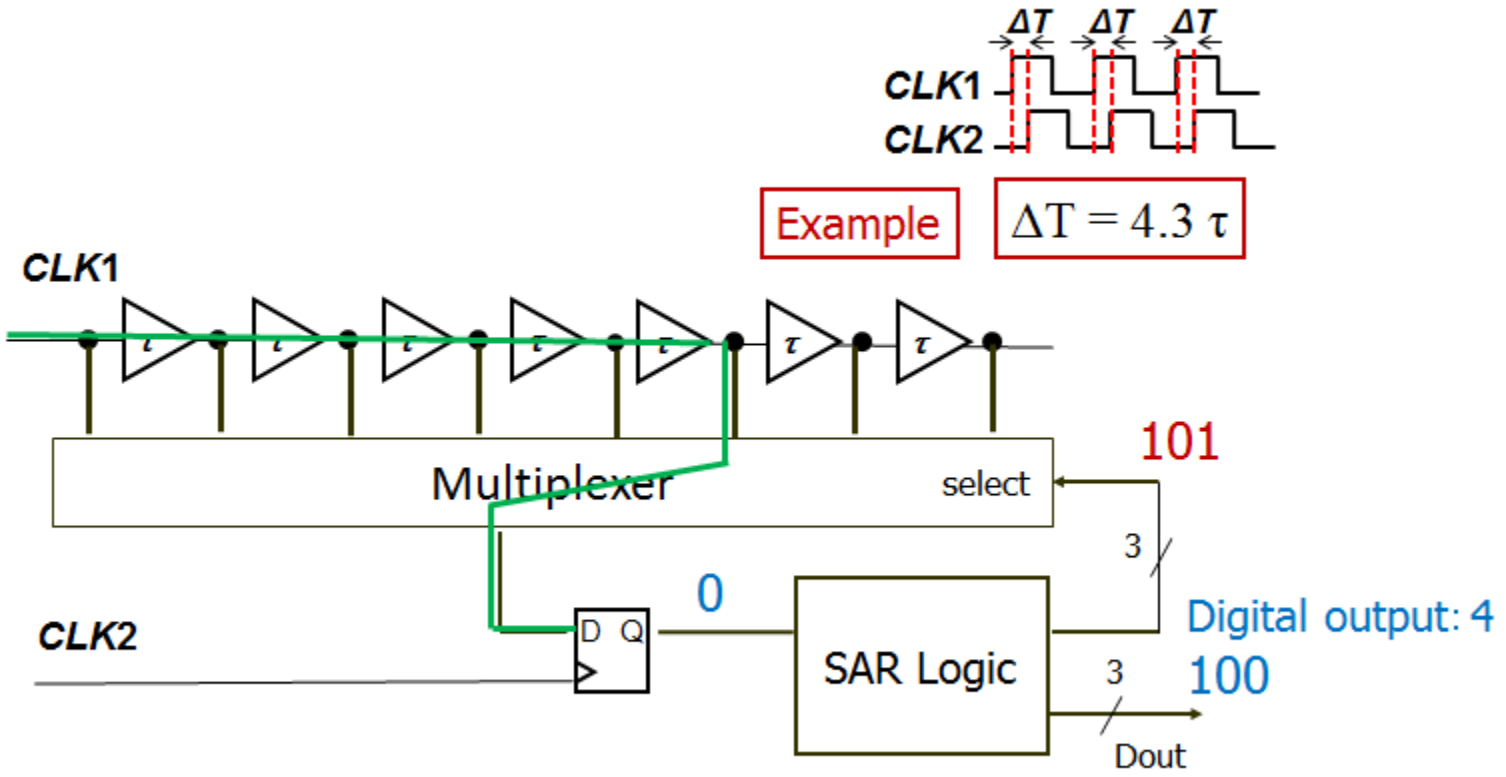
SAR TDC Operation Step 1



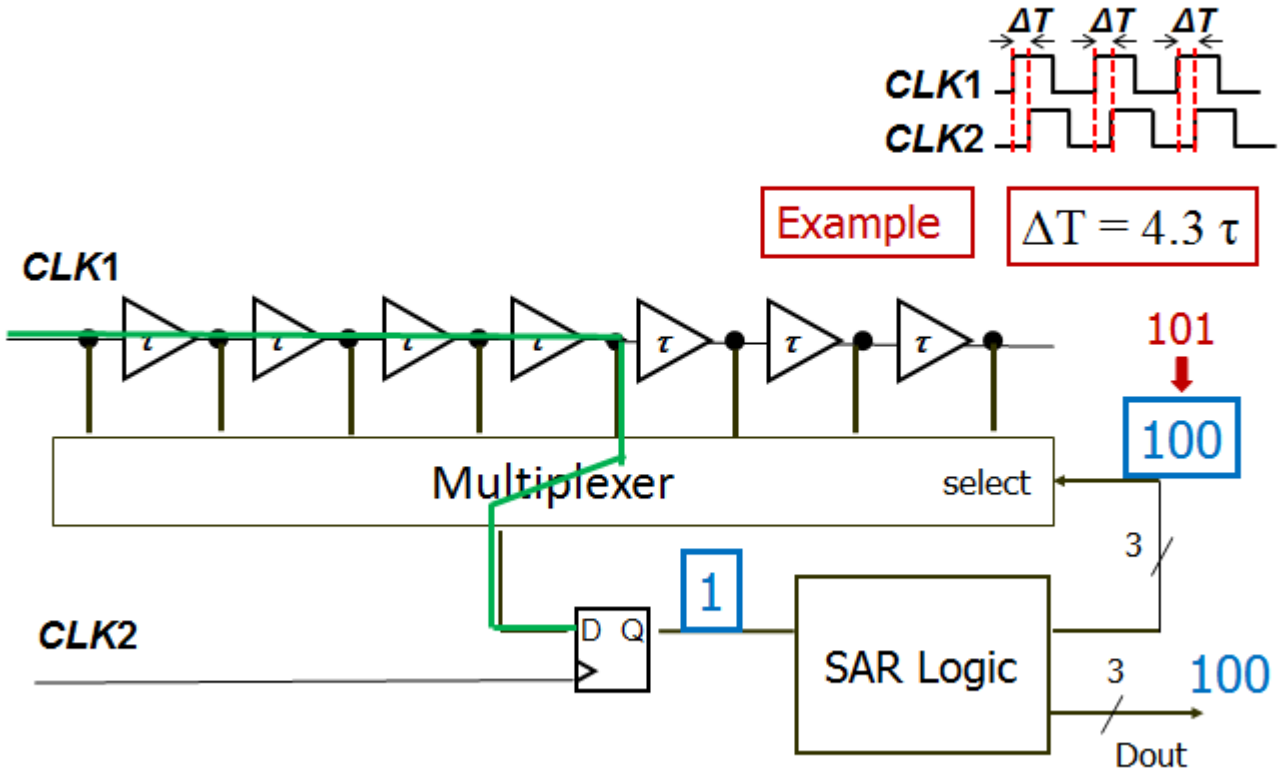
SAR TDC Operation Step 2



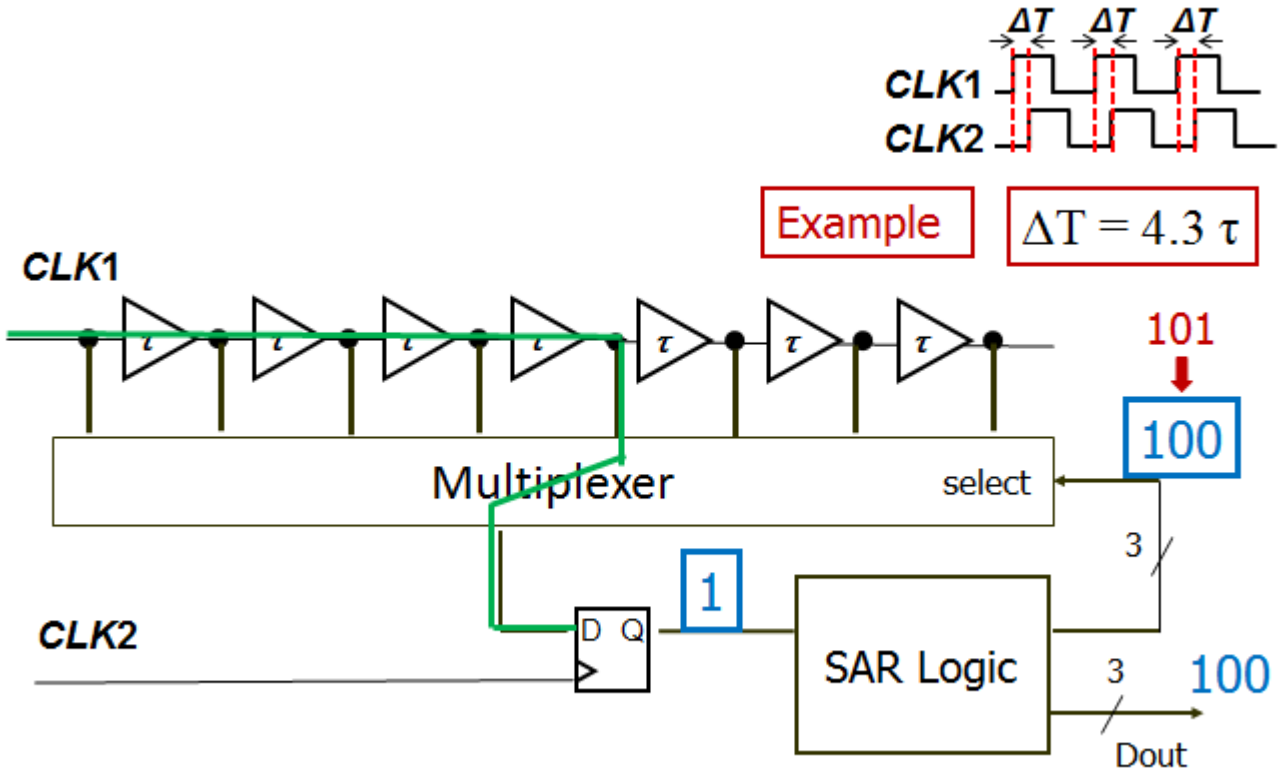
SAR TDC Operation Step 3



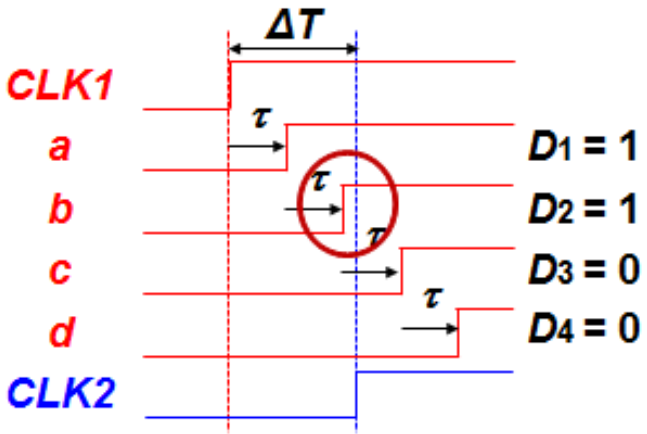
SAR TDC Operation Step 4



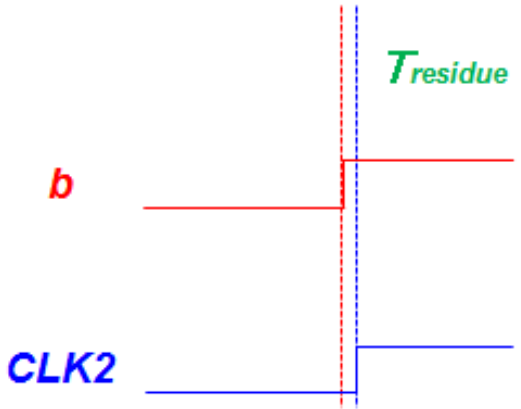
SAR TDC Operation Step 4 Steady State



Residue Time Usage



SAR TDC Operation Result

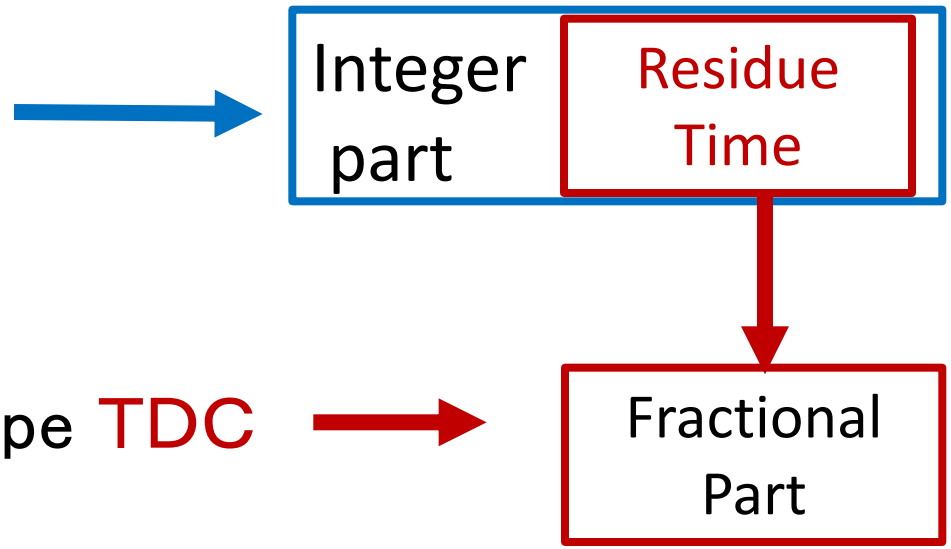


Residue time $T_{residue}$
Sub-TDC with fine time resolution

Fine time resolution

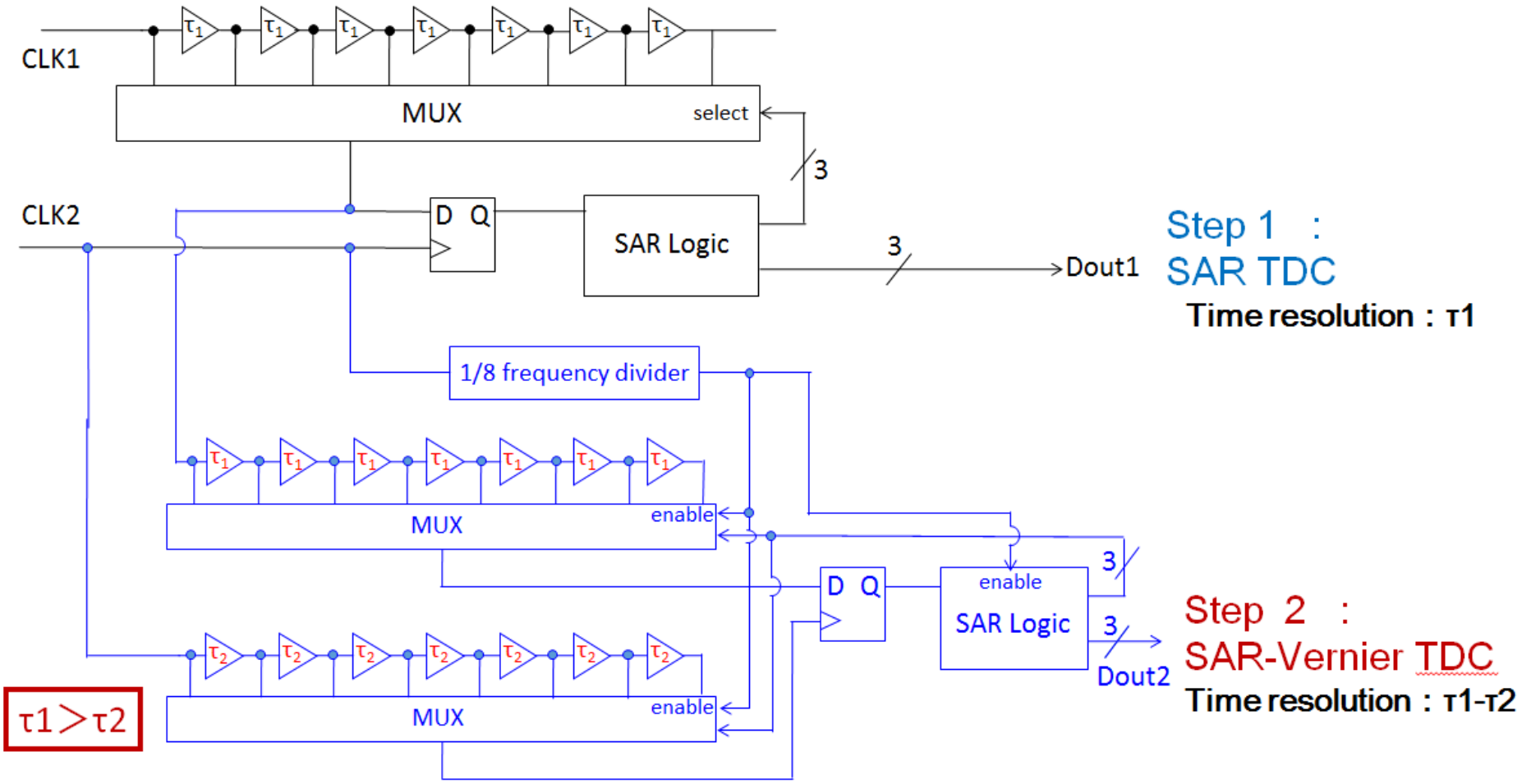
with 2-Step SAR＋Vernier-Type TDC

Step１：SAR TDC

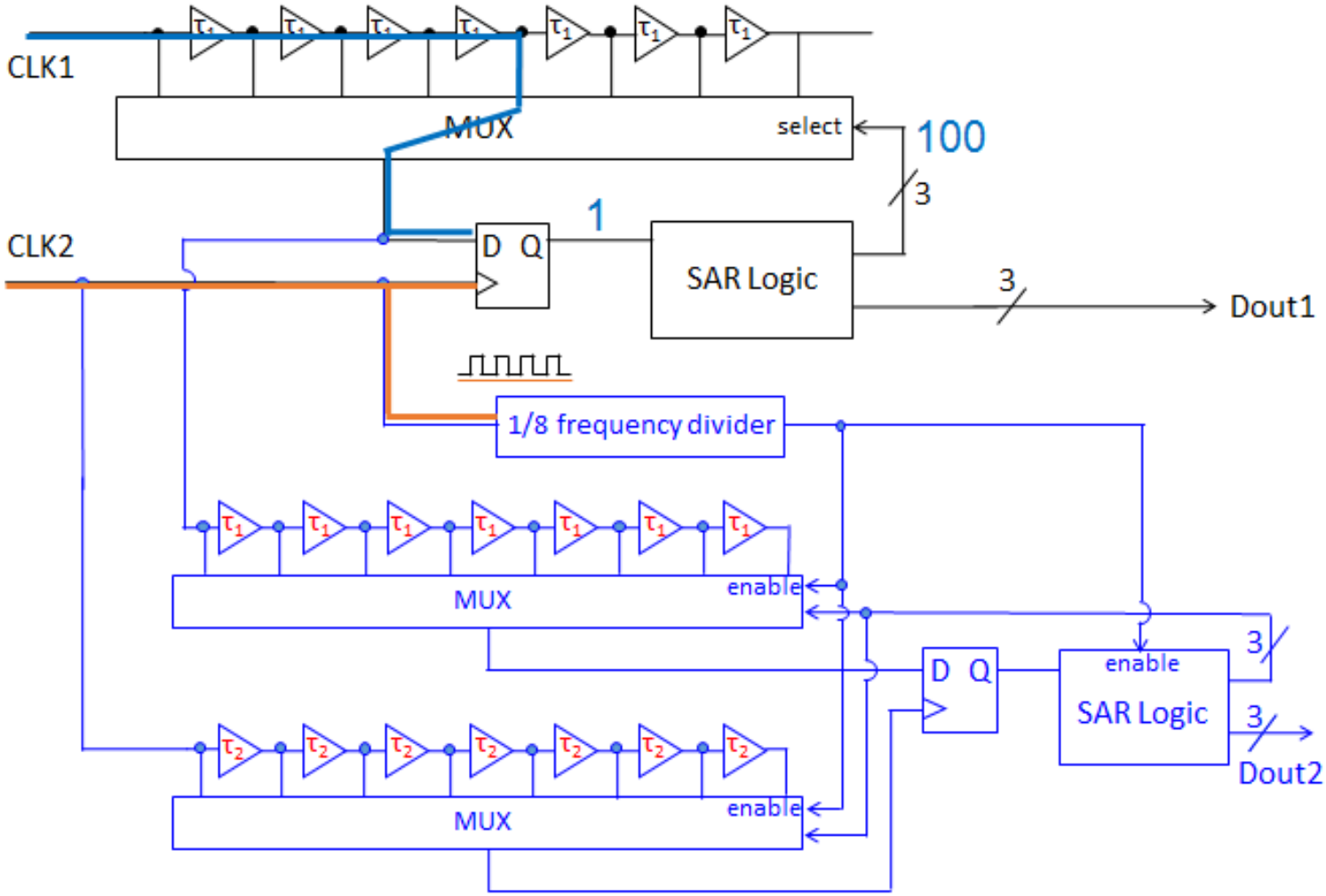


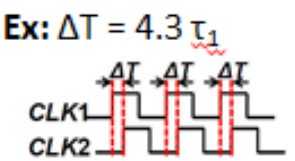
Step２：SAR +Vernier−type TDC

3bit SAR + 3bit SAR-Vernier TDC Configuration

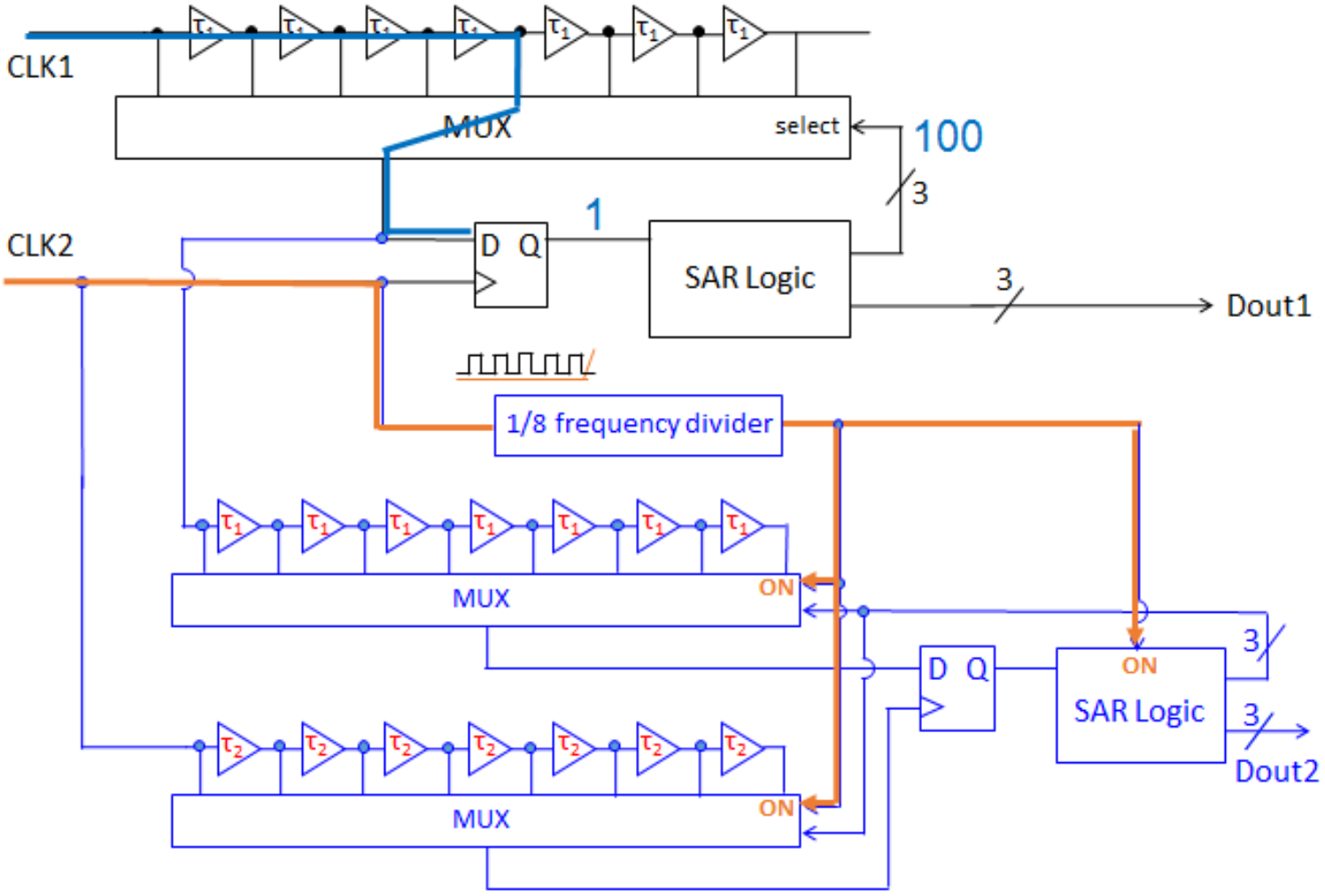


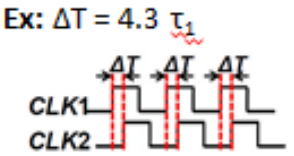
3bit SAR + 3bit SAR-Vernier TDC Operation ①



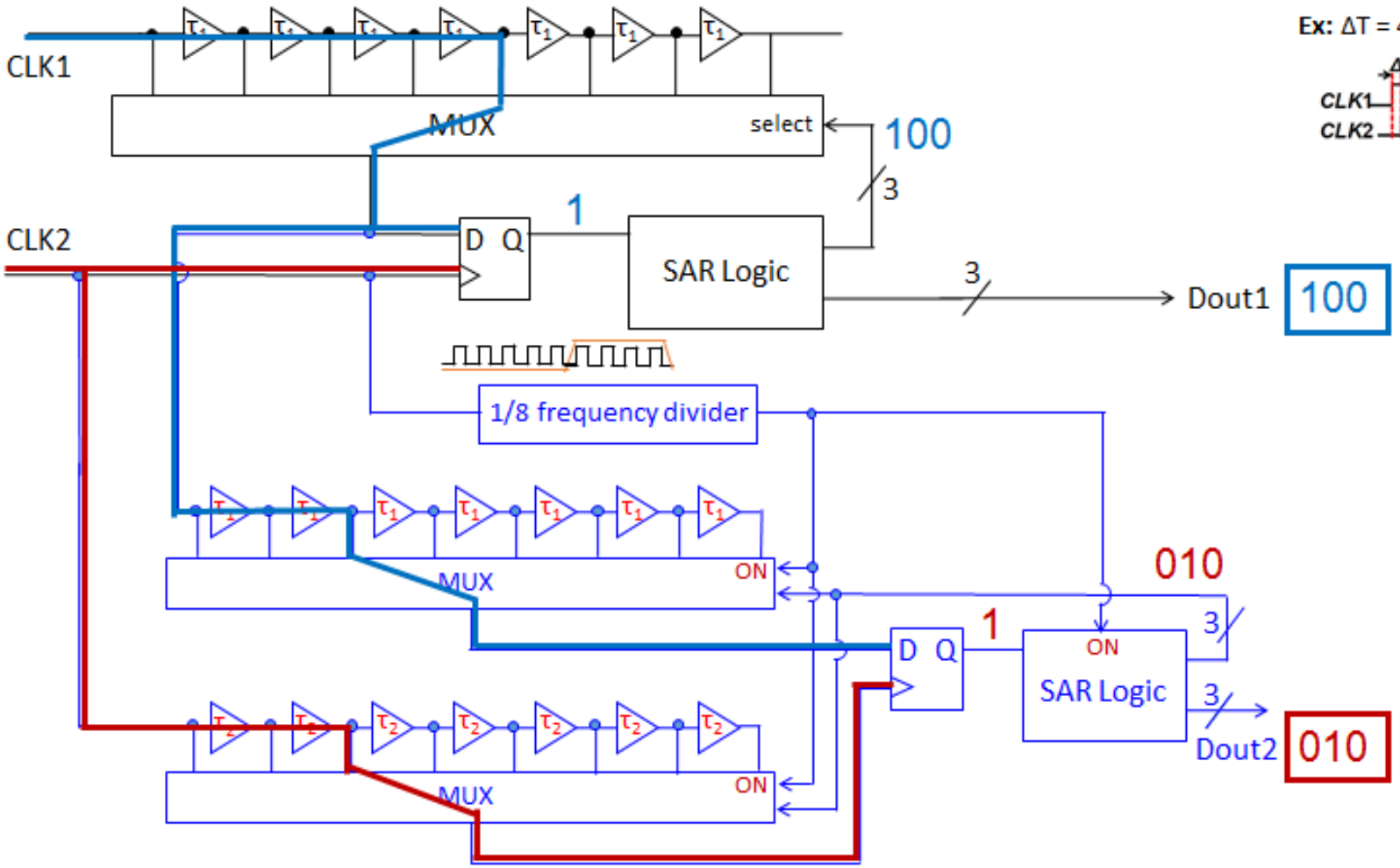


3bit SAR + 3bit SAR-Vernier TDC Operation ②

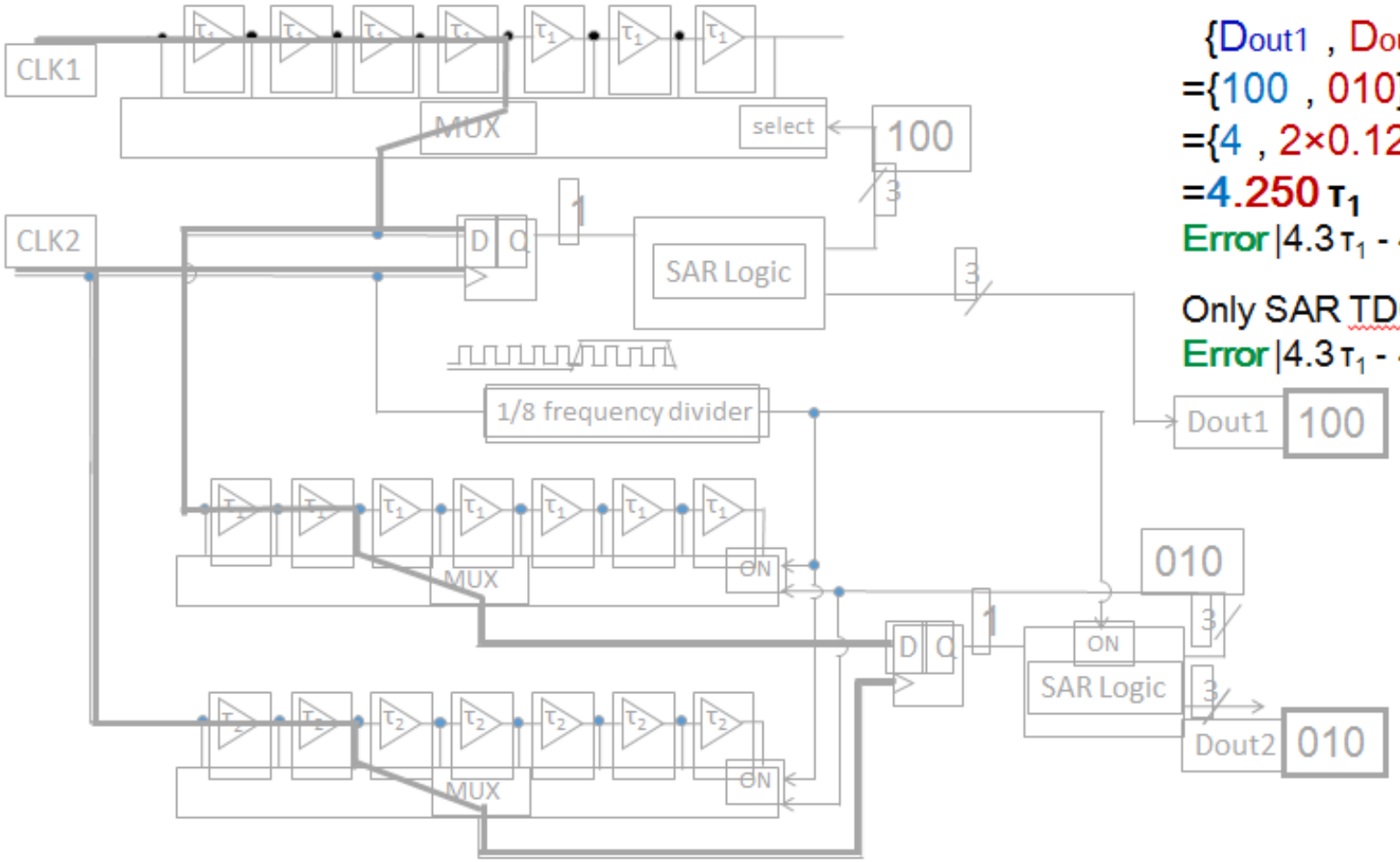




3bit SAR + 3bit SAR-Vernier TDC Operation ③



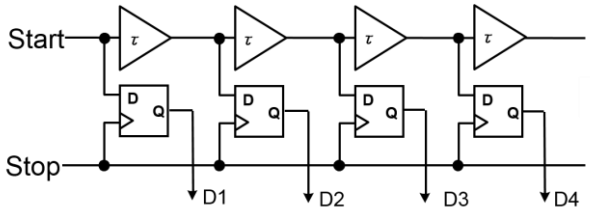
3bit SAR + 3bit SAR-Vernier TDC Output

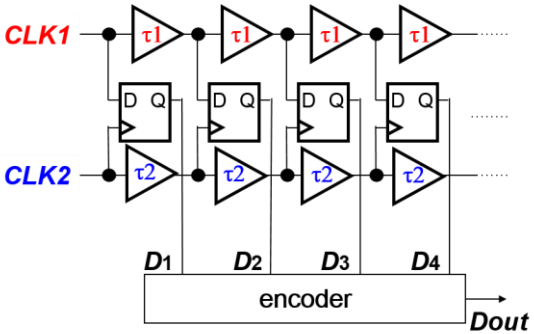


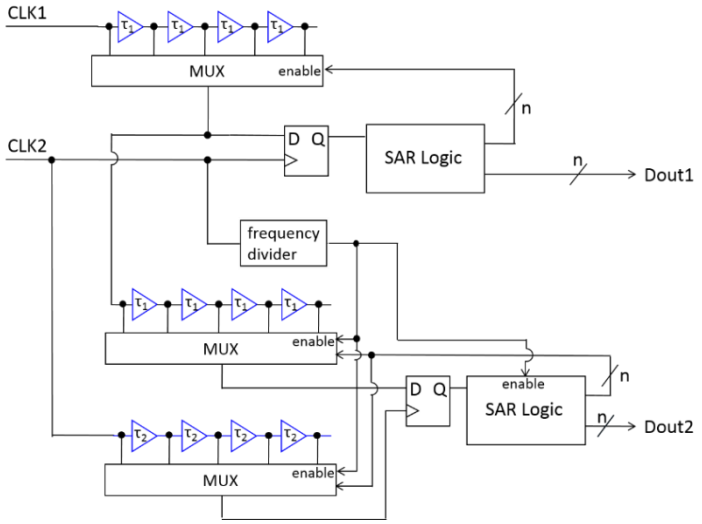
{Dout1 , Dout2}
$=\{100 , 010\}_2$
$=\{4 , 2\times0.125\}_{10}$
$=4.250\,\tau_1$
Error $|4.3\,\tau_1 - 4.250\,\tau_1| = 0.05\,\tau_1$

Only SAR TDC:
Error $|4.3\,\tau_1 - 4\,\tau_1| = 0.3\,\tau_1$

Flash TDC vs. Vernier TDC vs. SAR + SAR-Vernier







10bit design case			5bit+5bit
# of buffers:	1023	2046	93
# of DFFs:	1023	1023	14
Time resolution:	τ1	τ1-τ2	τ1-τ2
Measurement time:	One shot	One shot	10 times

Xilinx ISE 14.1 RTL Simulation Verification

CLK1, CLK2 periods: 33MHz

Buffer delays: $\tau_1 = 3.788ns$

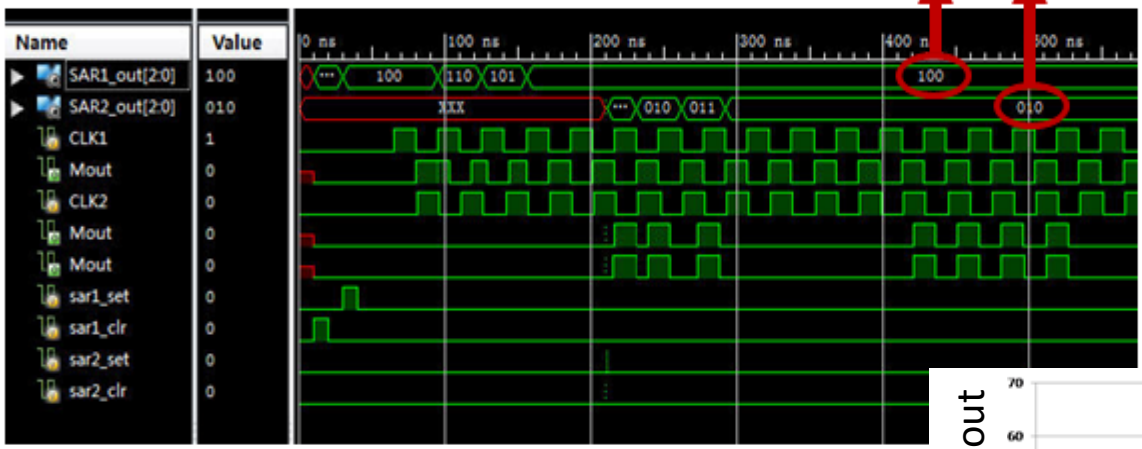
$\tau_2 = 3.314ns$

Time resolution: $\tau_1 - \tau_2 = 1/8\tau_1 = 0.474ns$

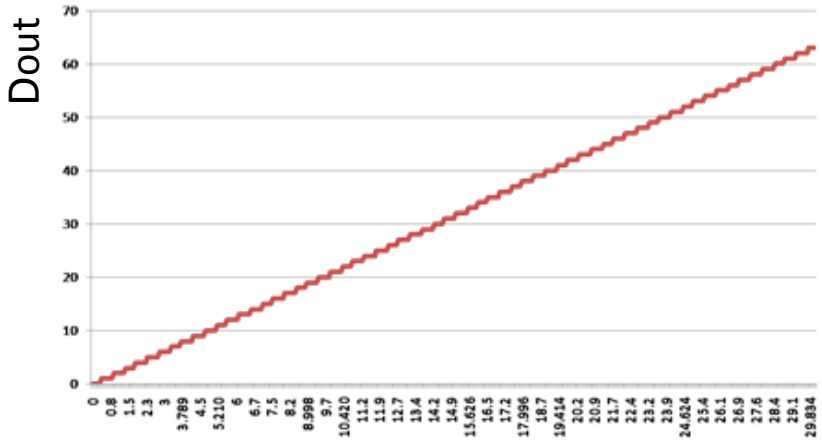
Input timing difference: $\triangle T = 4.3\tau_1 = \mathbf{16.286ns}$

Digital output:

$\{Dout1, Dout2\} = \{100, 010\}_2 = 4.250\tau_1 = \mathbf{16.099ns}$



Verilog HDL 3bit SAR + 3bit SAR-Vernier TDC



Input time difference ΔT [ns]

Random Variation among Delay Cells

- Delay τ variation

  Relative variation

  ➡ TDC nonlinearity

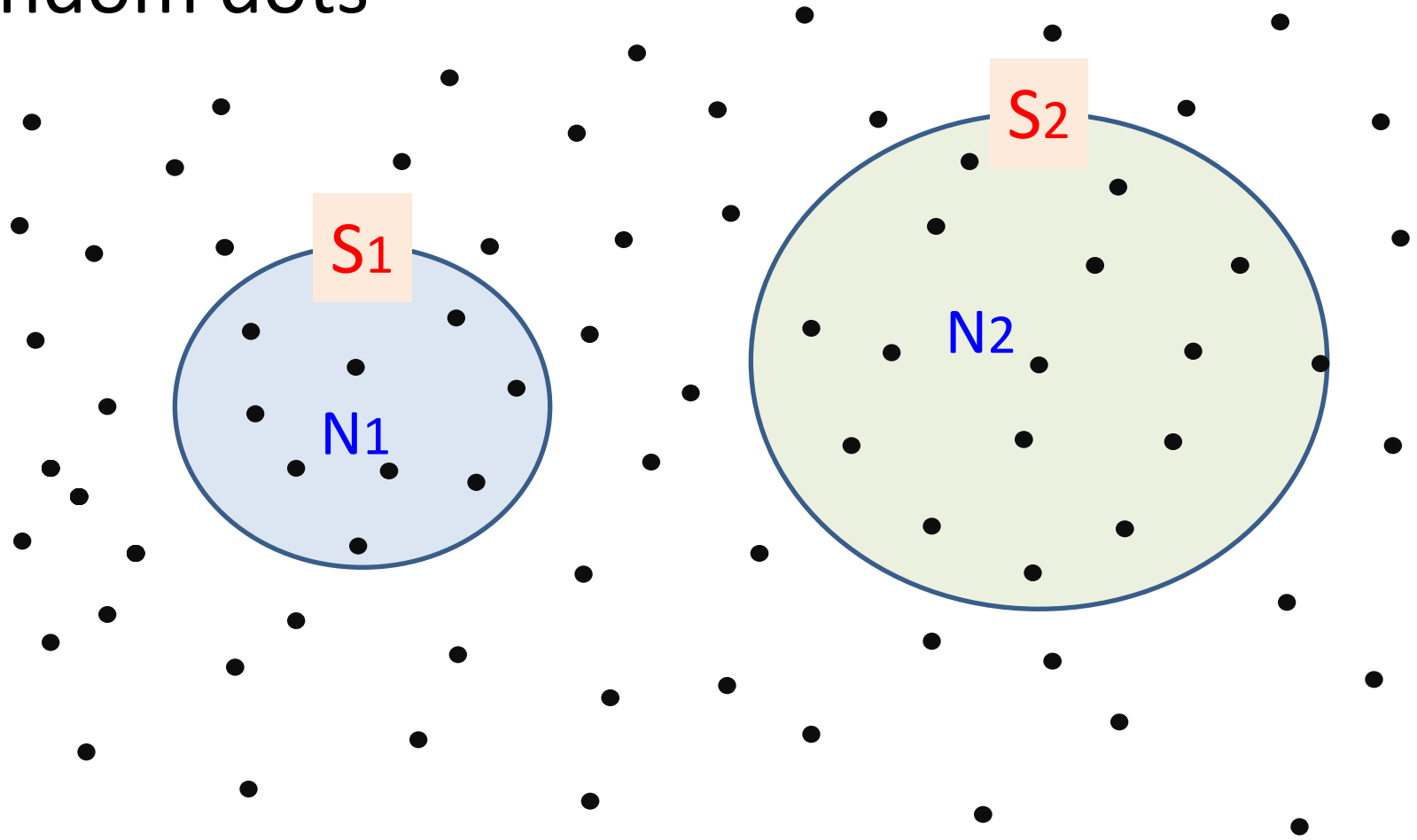
  Absolute（average value) variation

  ➡ TDC input range & time resolution

- Focus on relative variation here.

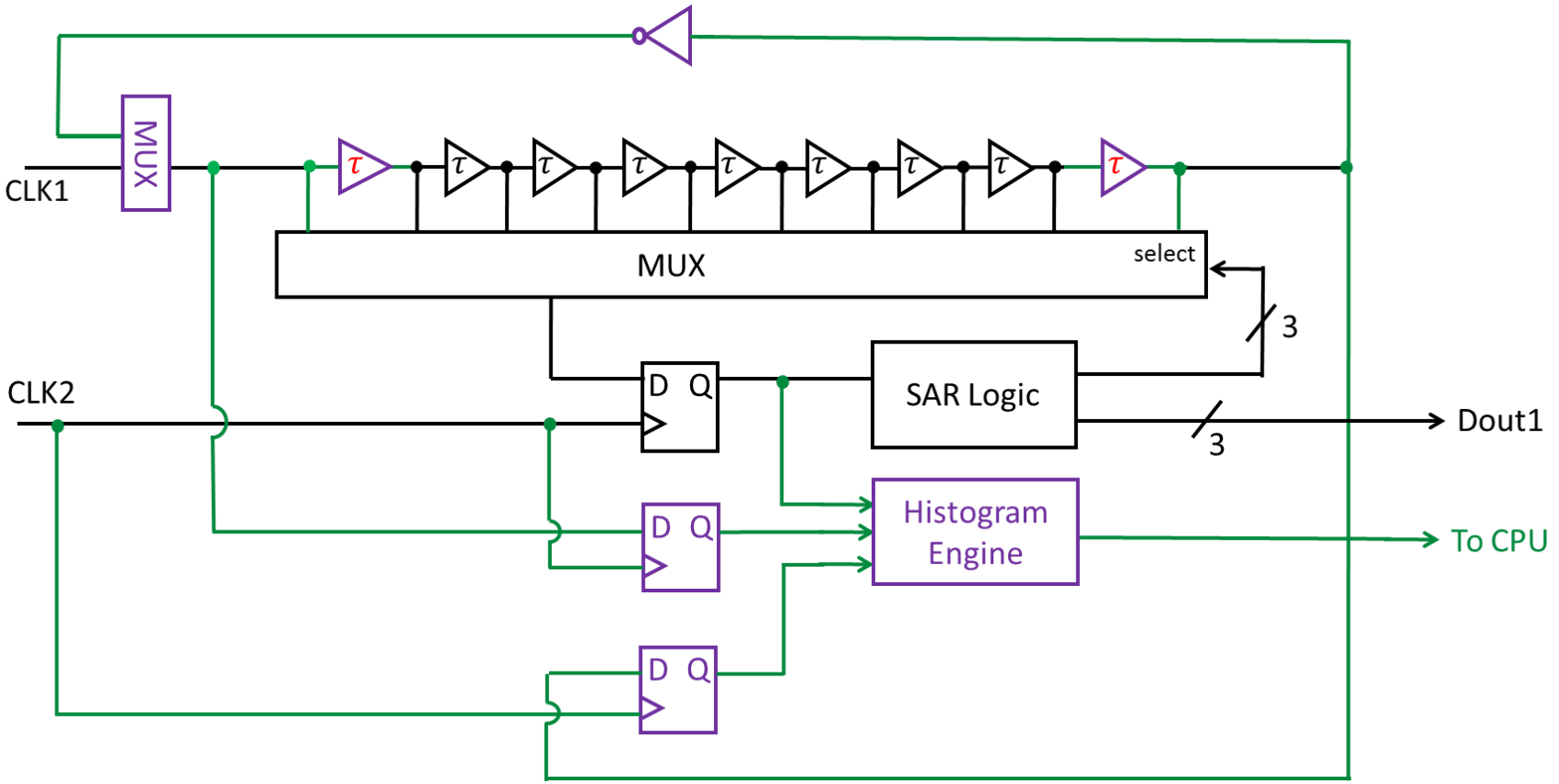
Measurement with Histogram

Random dots



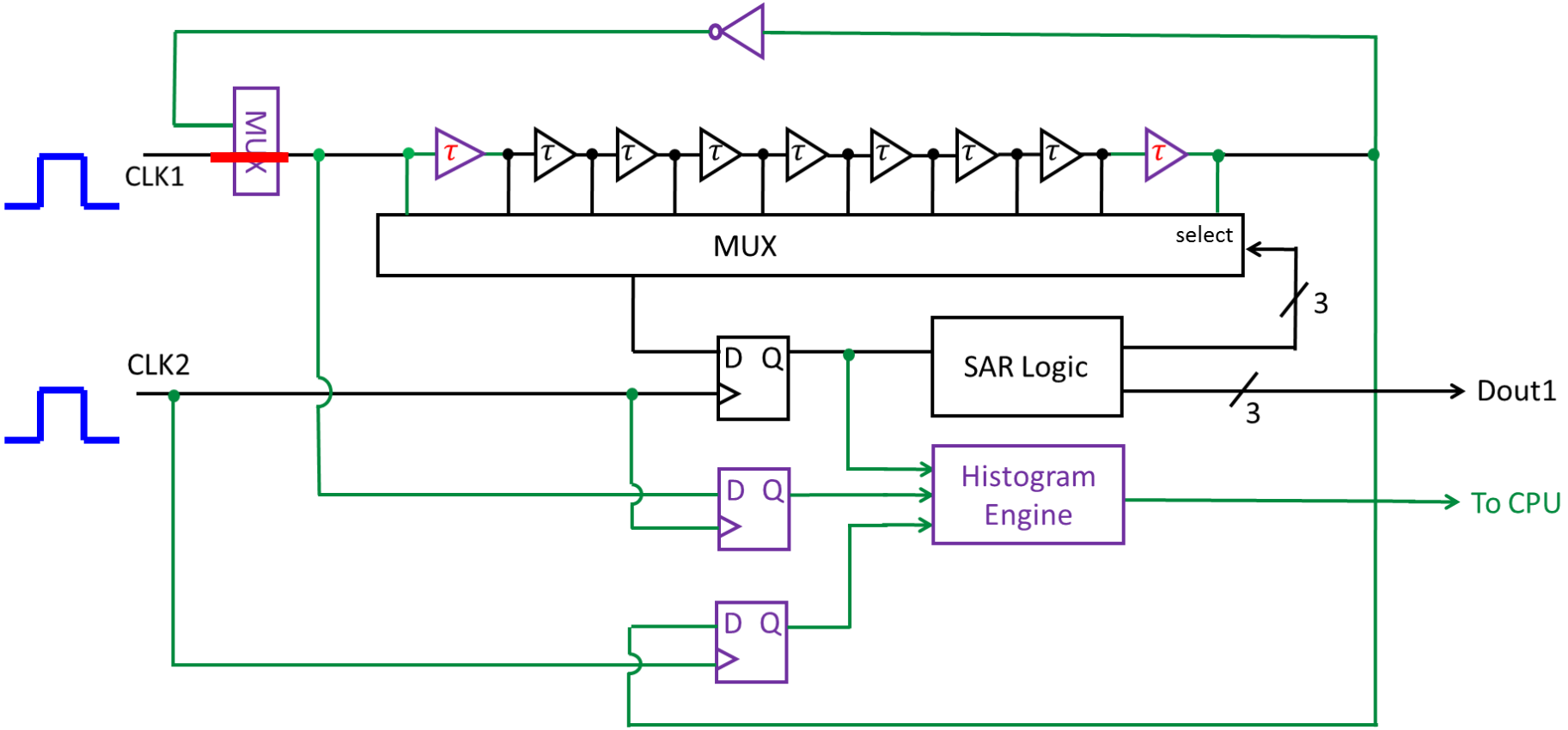
# of dots ratio $\frac{N1}{N2}$ ⇒ Area ratio $\frac{S1}{S2}$

SAR TDC with Self-Calibration

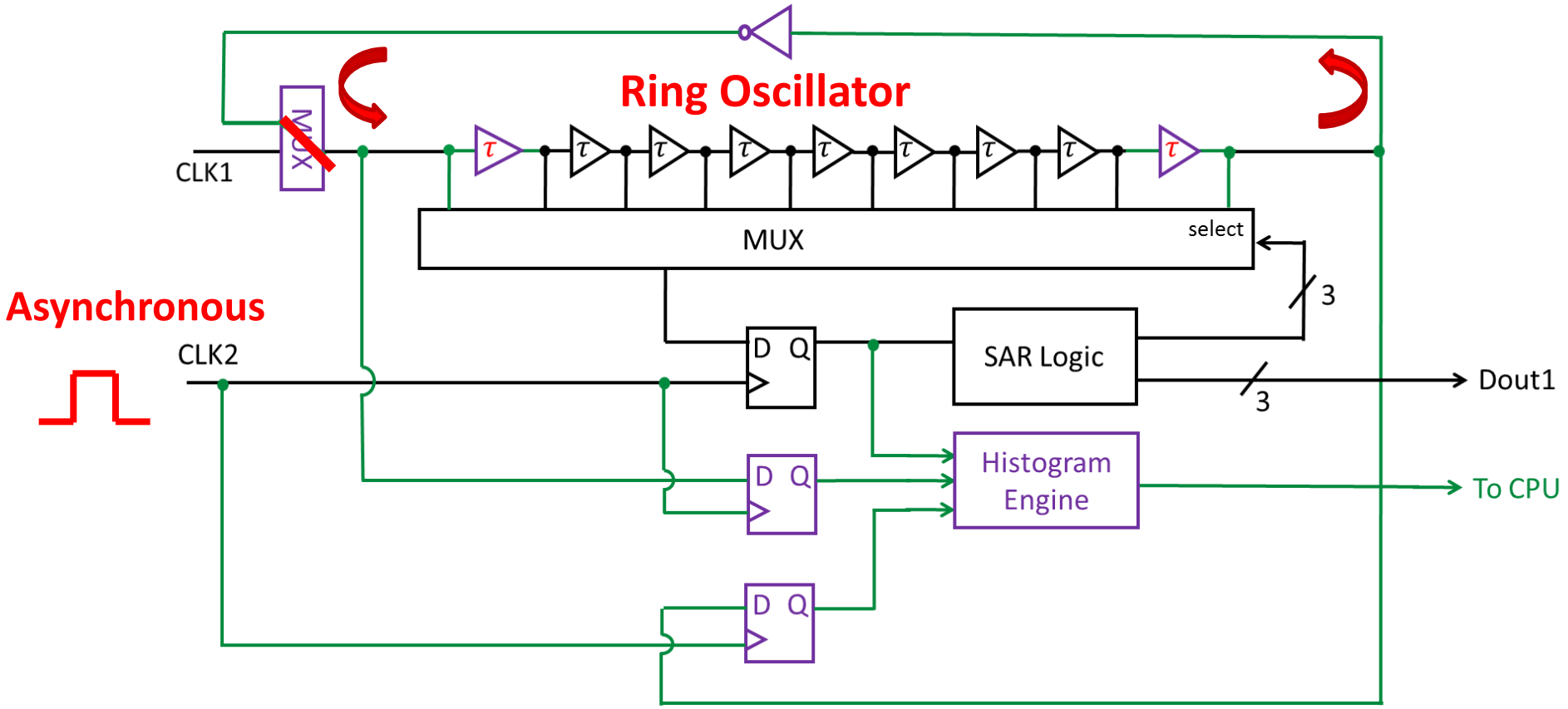


Addition of calibration circuit, interconnection

Normal Operation Mode

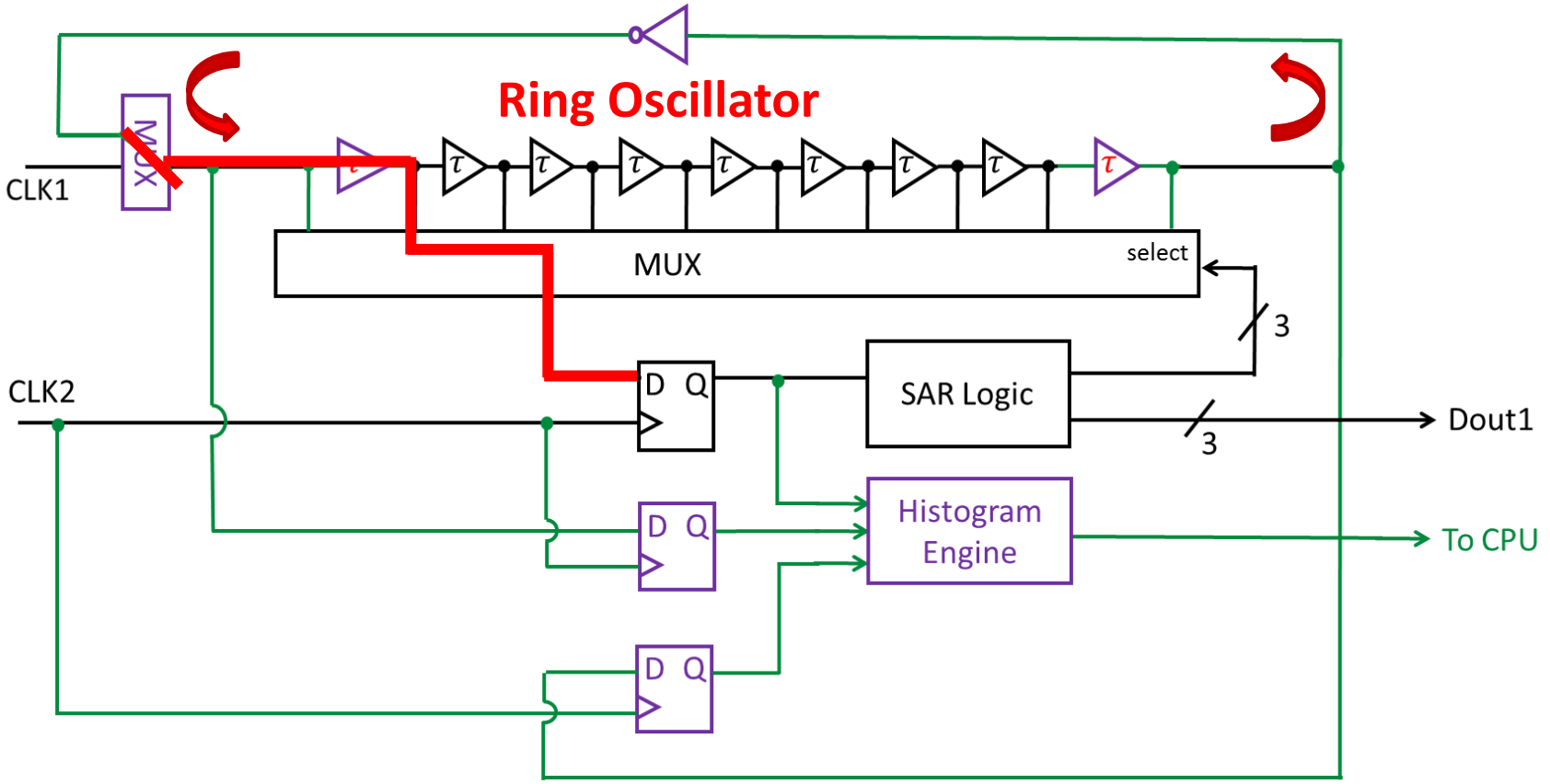


Calibration Mode

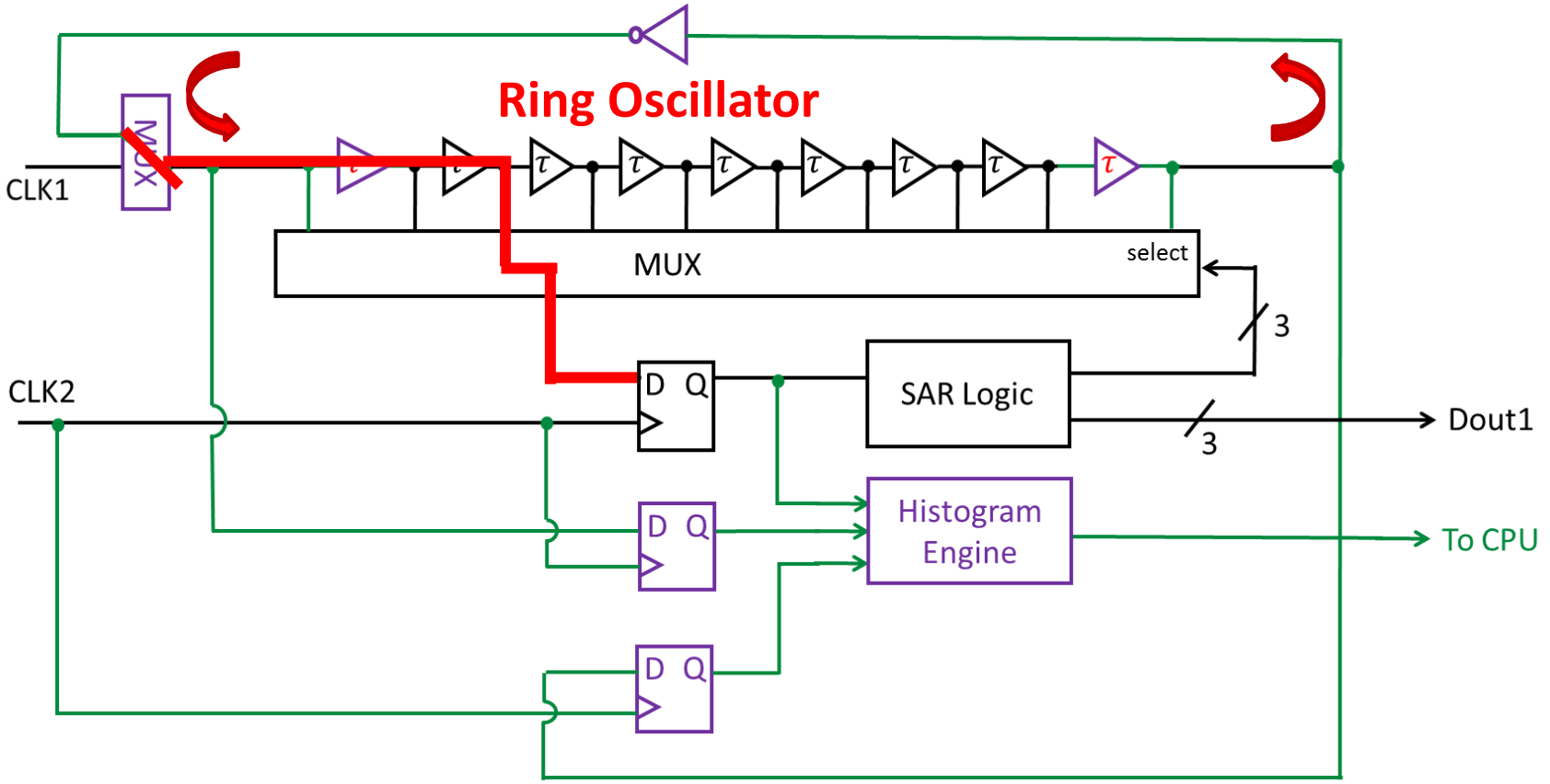


CLK1, CLK2 are NOT correlated. ⟺ Random dots

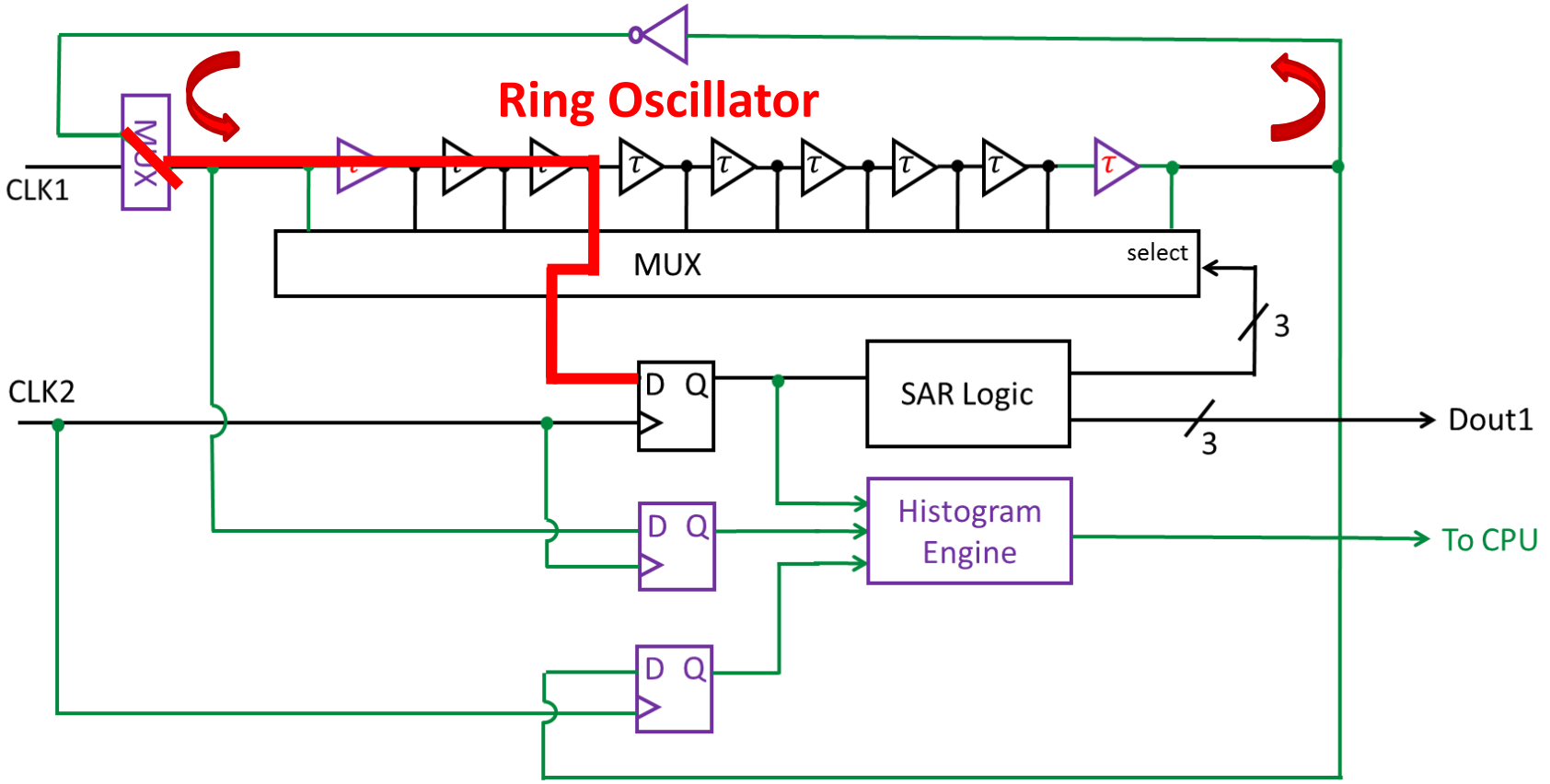
Calibration Mode (1)



Calibration Mode (2)



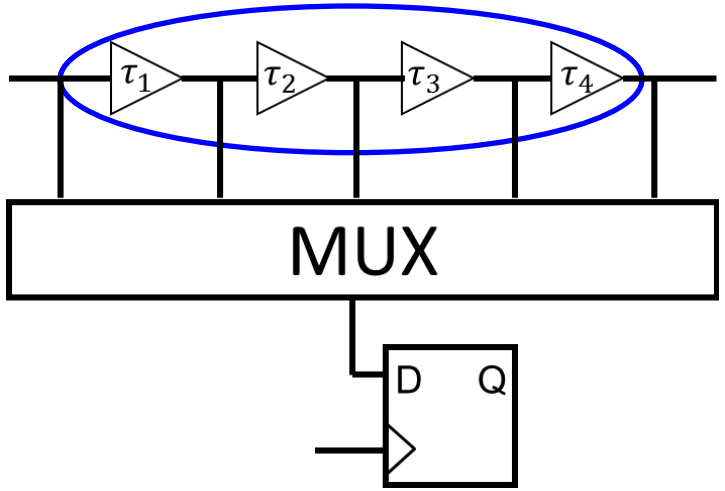
Calibration Mode (3)

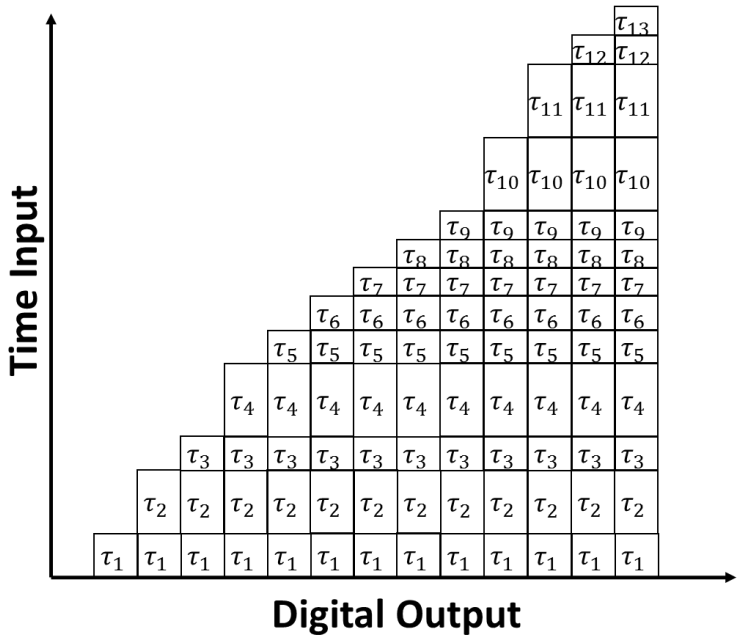


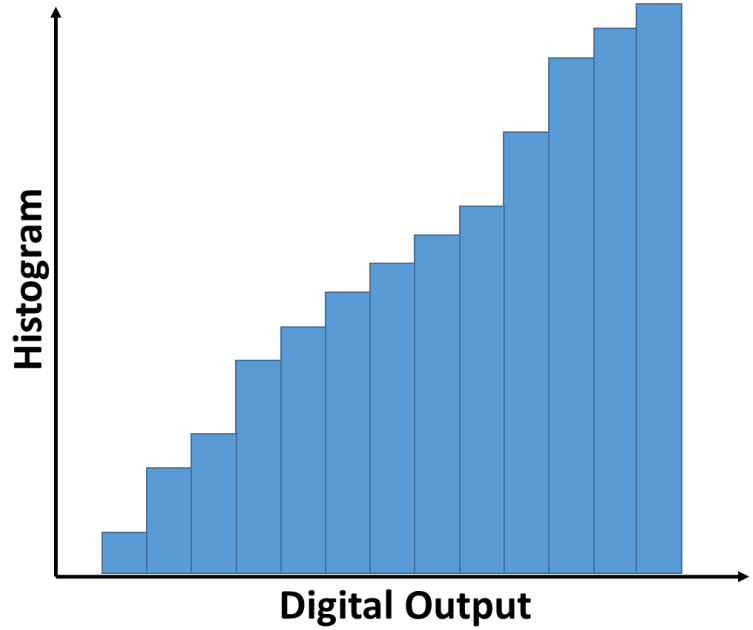
Measurement of Delay Values

Histogram Method

- Delay values can be measured

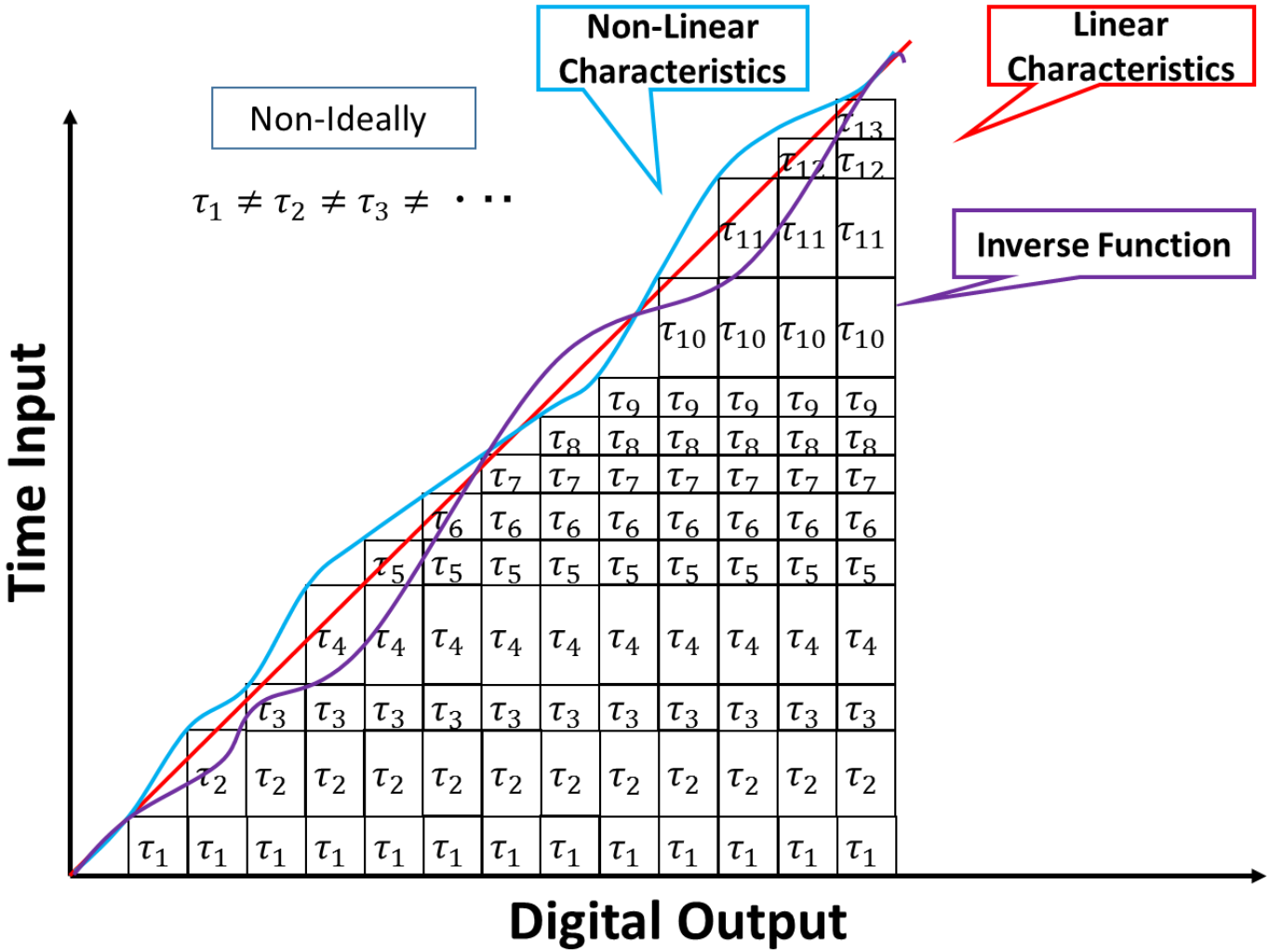




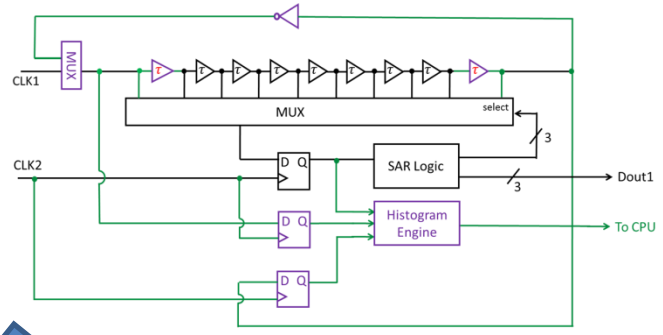


Digital Correction of TDC Nonlinearity

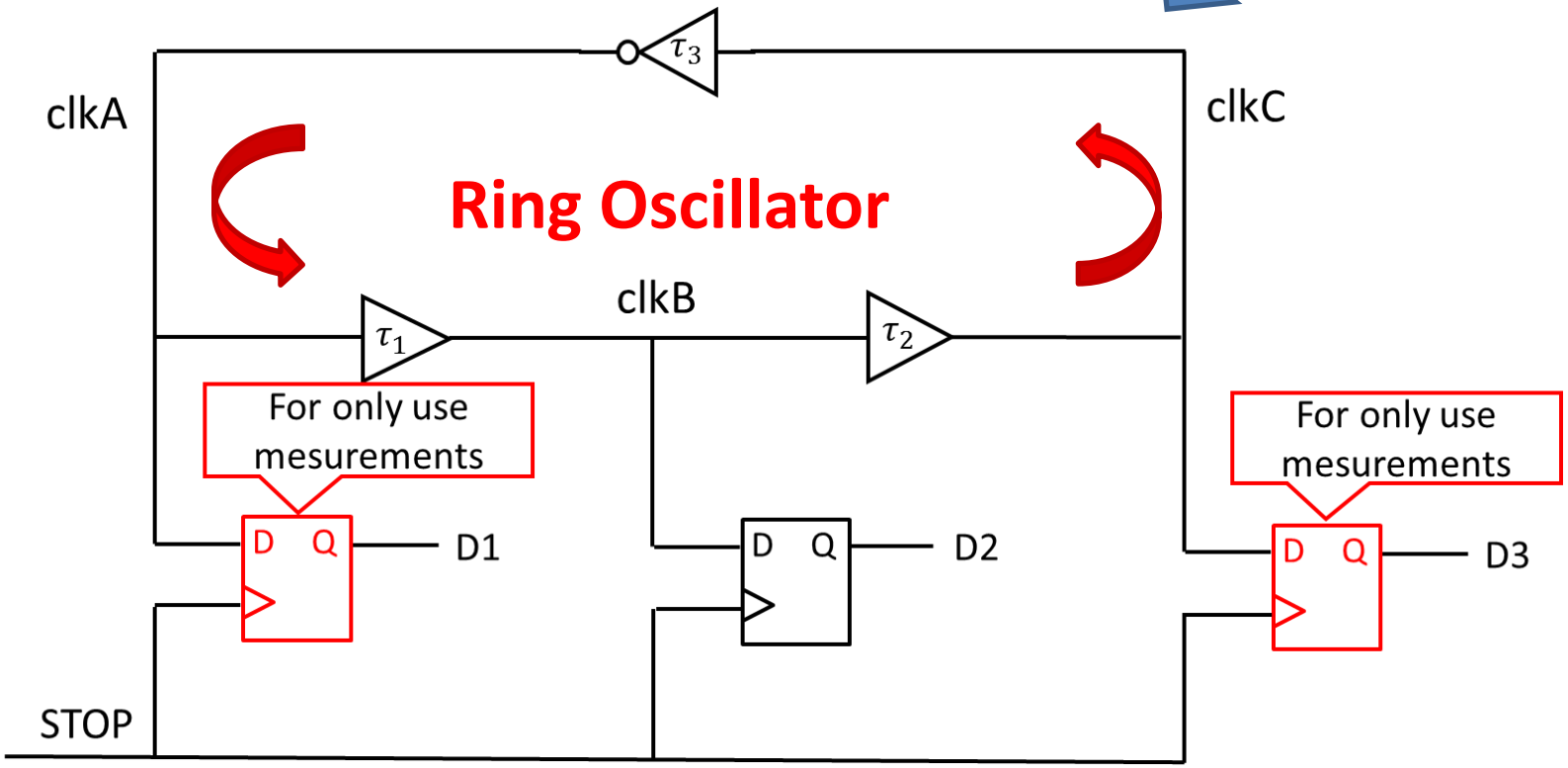
Correction with Inverse Transfer Function



Measurement of Delays with Histogram

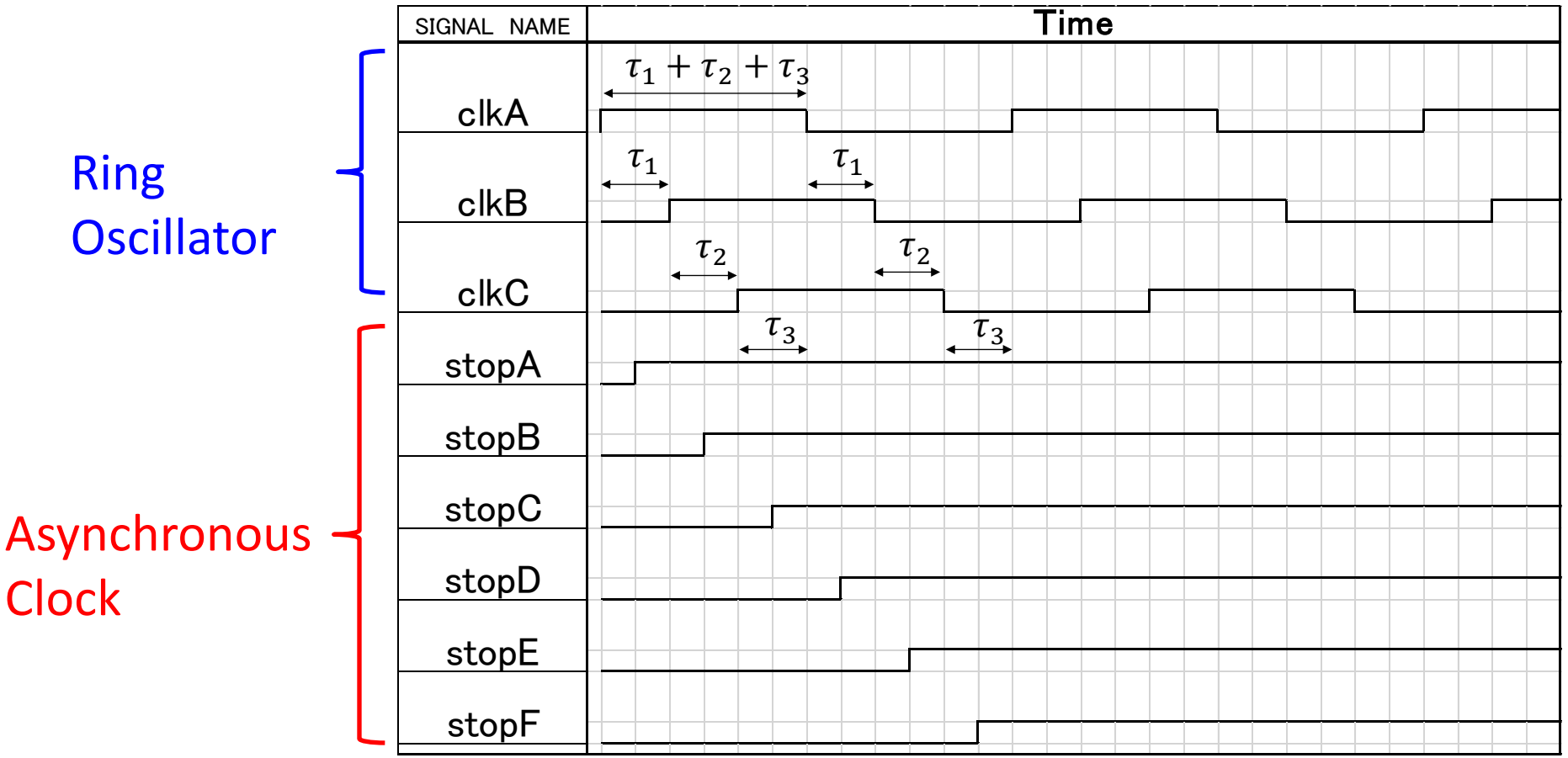


Simplified Model



Operation of Histogram Method

Timing Chart



Digital Error Correction

- TDC linearity self-calibration with histogram

Dout(0)=1
Dout(1)=3
Dout(2)=5
Dout(3)=8
.
.

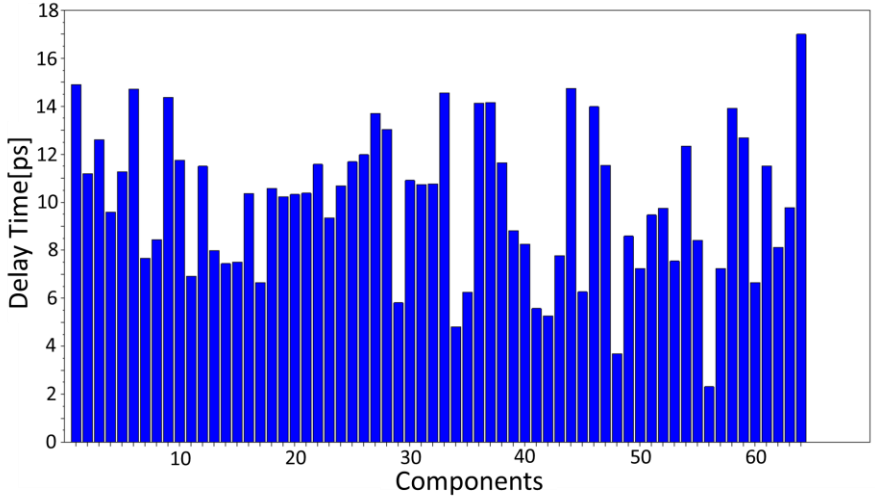
Calibration

Dout(0)=0.3
Dout(1)=2.8
Dout(2)=4.5
Dout(3)=7.3
.
.

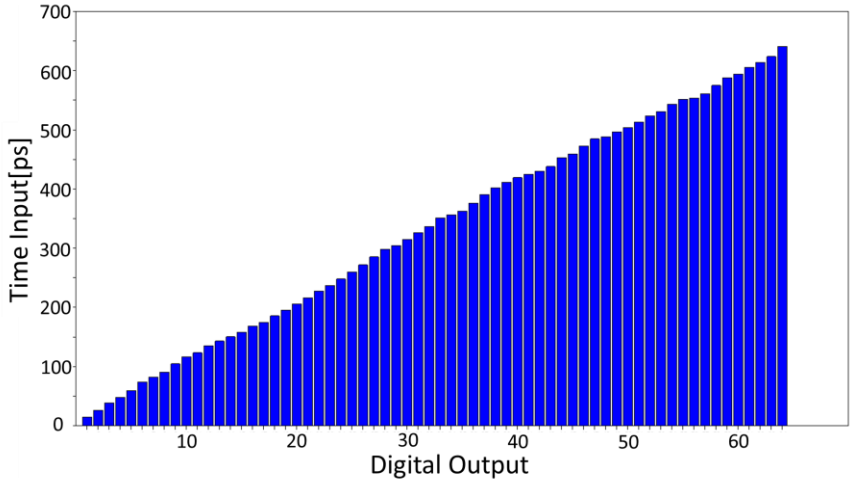
Corrected based on delay variation estimation

Simulation Verification

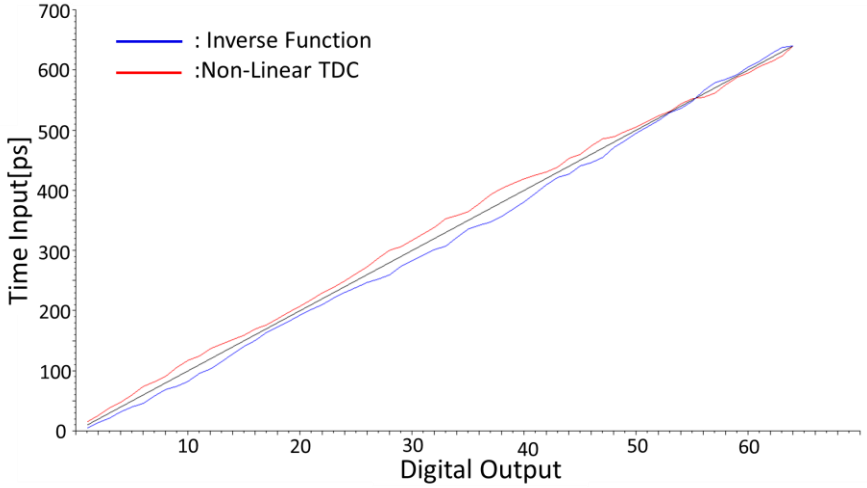
Delay variation

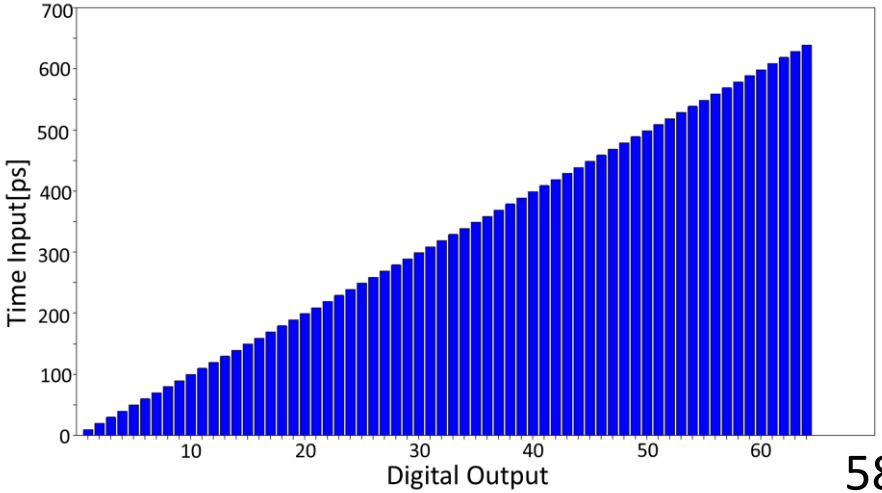


TDC characteristics before calibration



TDC characteristics after calibration



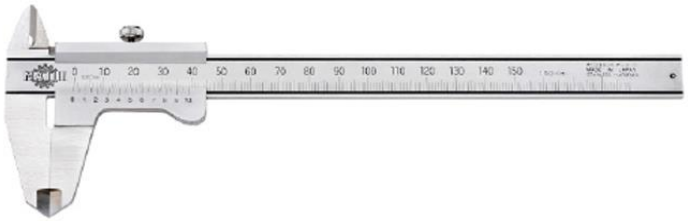


Vernia Invention

"Vernia" technology was invented by French mathematician, Pierre Vernier.

1580- 1637

***"La construction, l'usage, et les proprietes du quadrant nouveau de mathematiques"* (1631)**



Contents

- Research Objective
- TDC Application to LSI Testing Technology
- 4 Types of TDCs Developed at Gunma Univ.
  - ✓ Flash-type TDC
  - ✓ Gray code based TDC
  - ✓ SAR-typeTDC
  - ✓ Delta-Sigma TDC
- Discussions and Conclusion

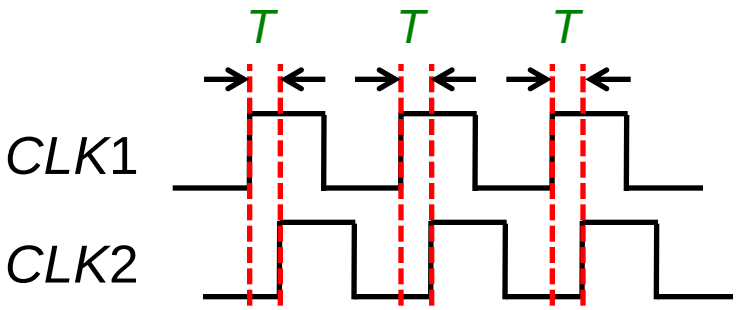
4 Types of TDCs

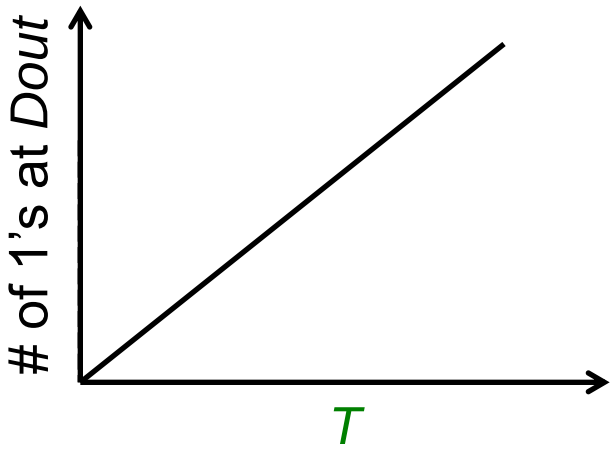
	Clocks Under Test	Measurement Time	Time Resolution	Circuit	FPGA
Flash-type	Single event ○	Short ○	Coarse ✕	Large ✕	Digital ○
Gray code based	Single event ○	Short ○	Coarse ✕	Small ○	Digital ○
SAR-type	Repetitive clock △	Middle △	Middle △	Small ○	Digital ○
Delta-Sigma type	Repetitive clock △	Long ✕	Fine ○	Small ○	Small Analog △

ΔΣ TDC Features

Timing *T* measurement between CLK1 and CLK2

ΔΣ Time-to-Digital Converter (TDC)

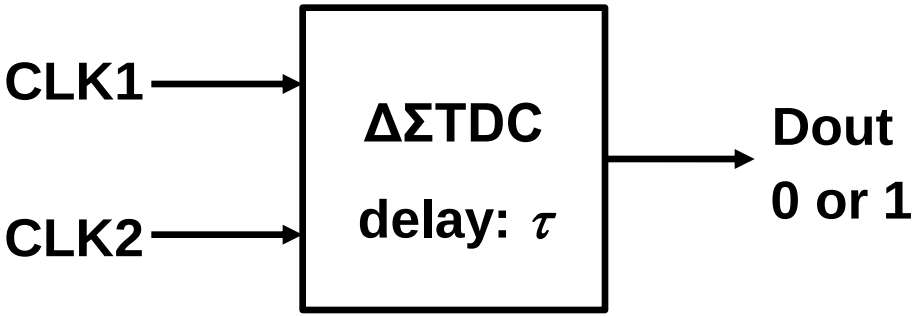


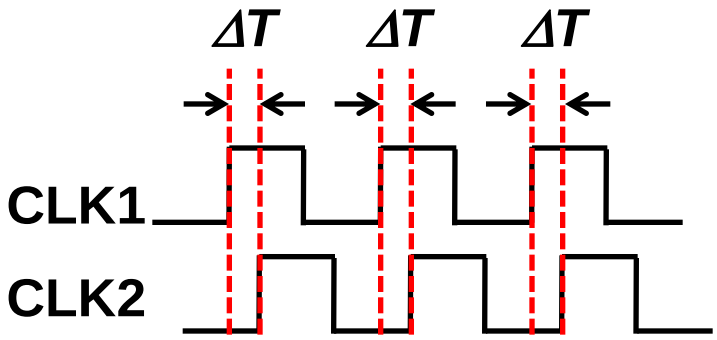


T ∝ # of 1' at *Dout*

- Simple circuit
- High linearity
- Measurement time → longer ⇒ time resolution → finer

Principle of ΔΣTDC





Dout # of 1's is proportional to ΔT

ΔT

# of 1's

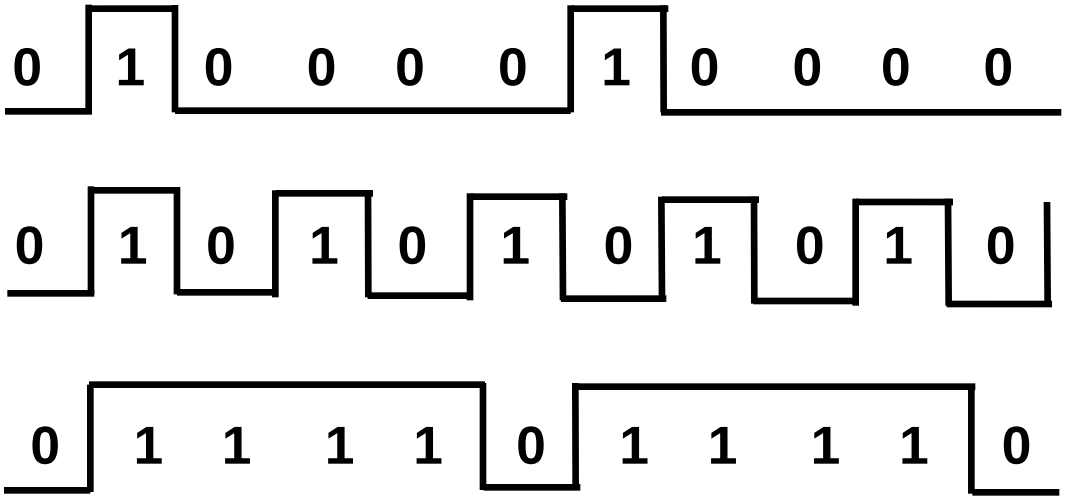
Dout

short

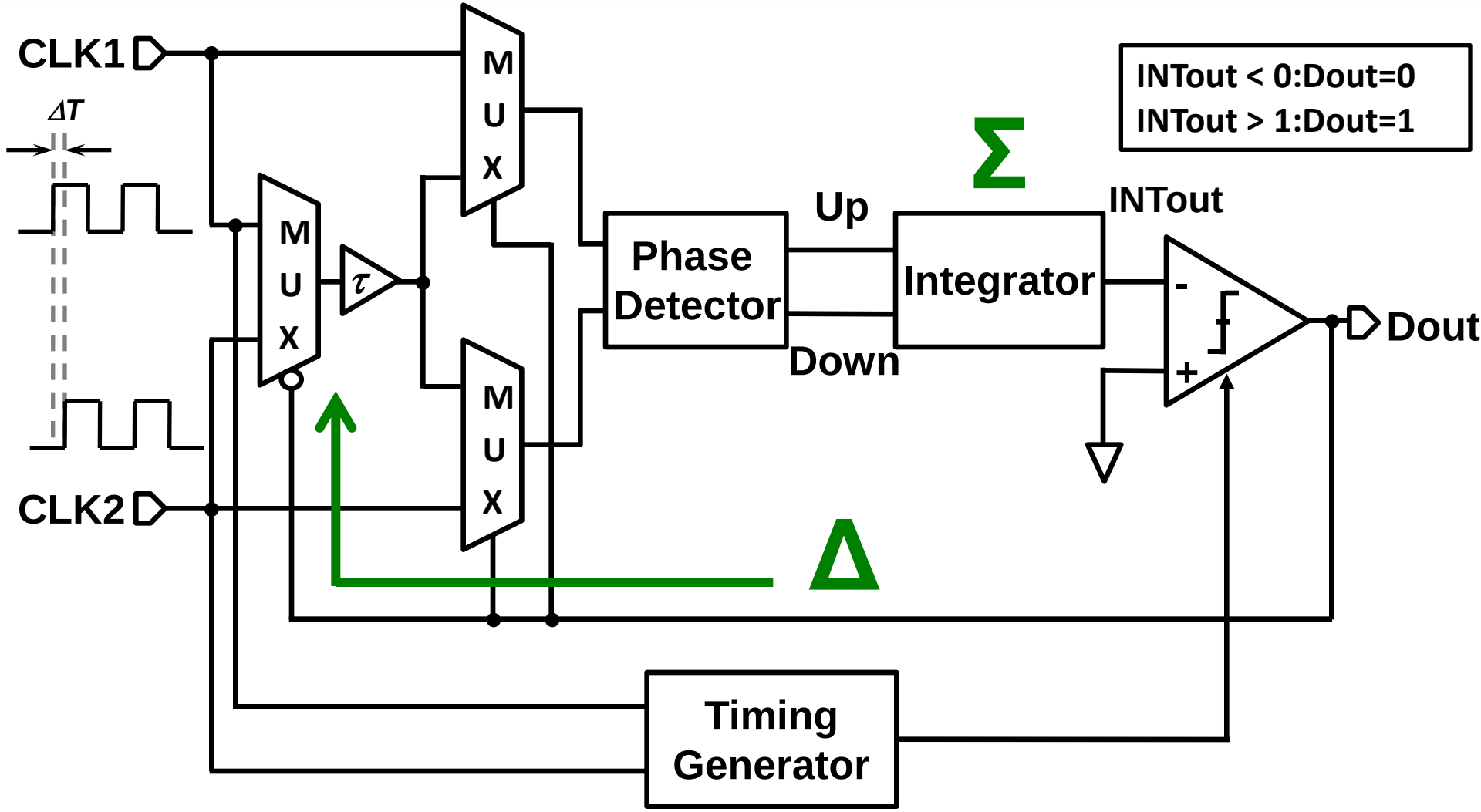
few

long

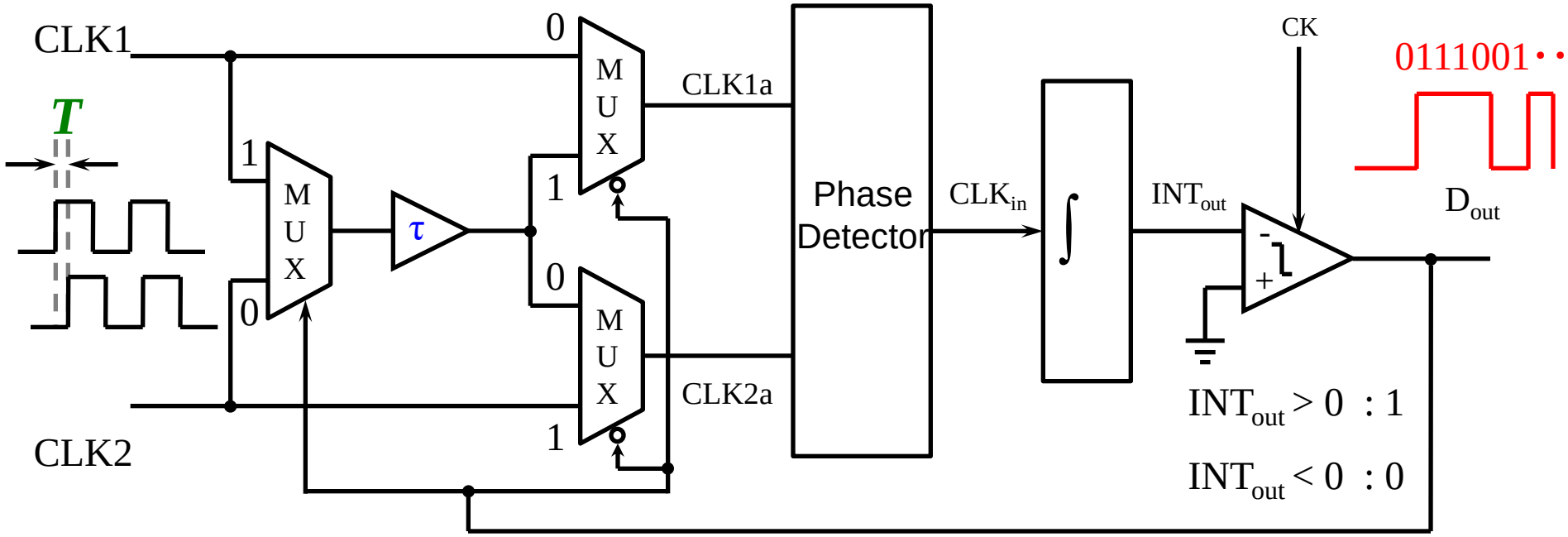
many



ΔΣTDC Configuration

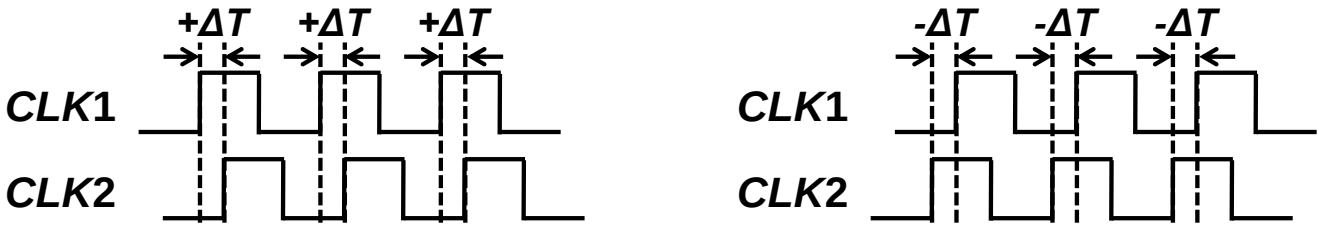


Single-Bit ΔΣ TDC



Time resolution : $\frac{2\tau}{\#\ of\ Dout \quad N_{DATA}}$

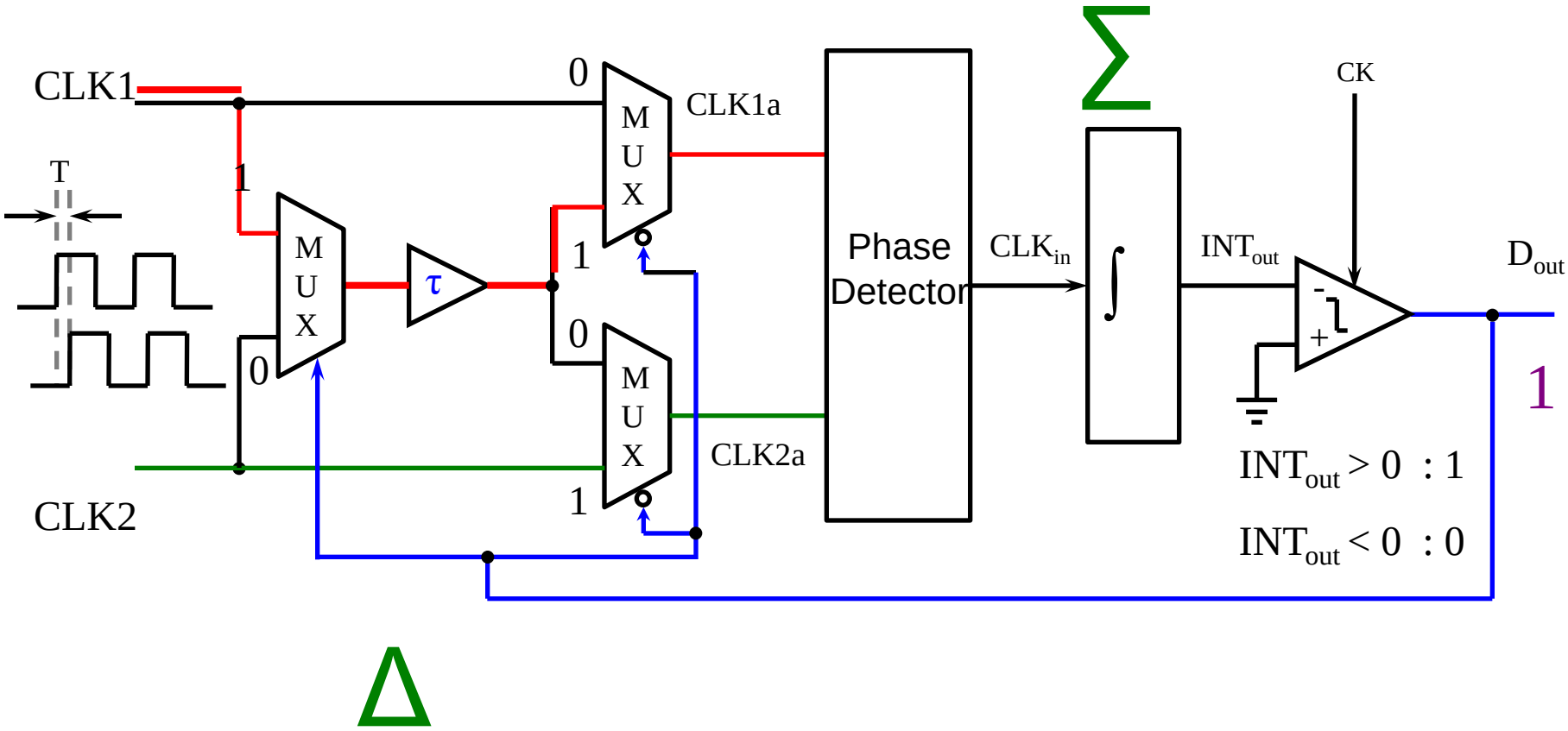
I : $-\tau < \Delta T < +\tau$



Delay line with 1bit digital input is inherently linear.

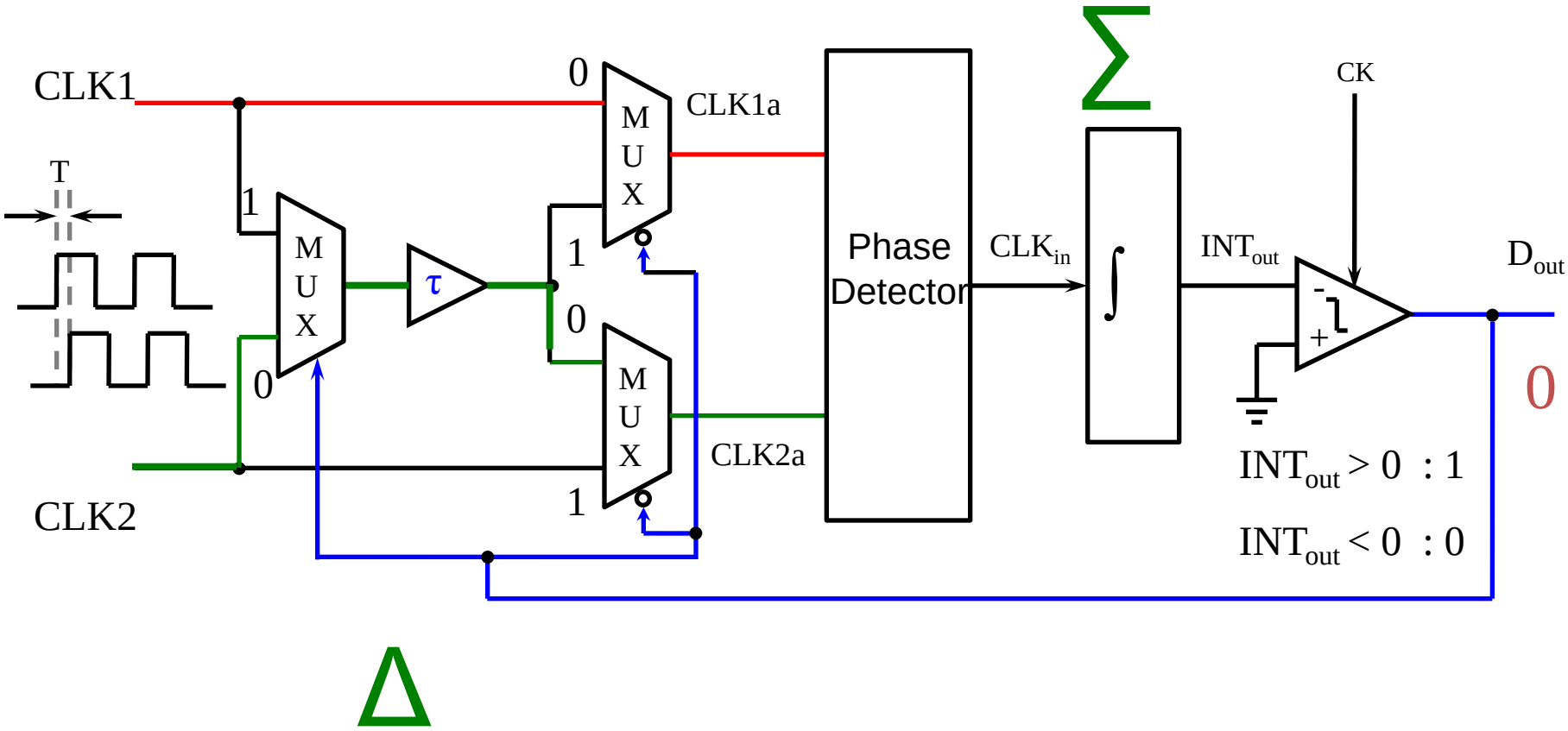
Operation of Single-Bit ΔΣ TDC

In case Dout =1

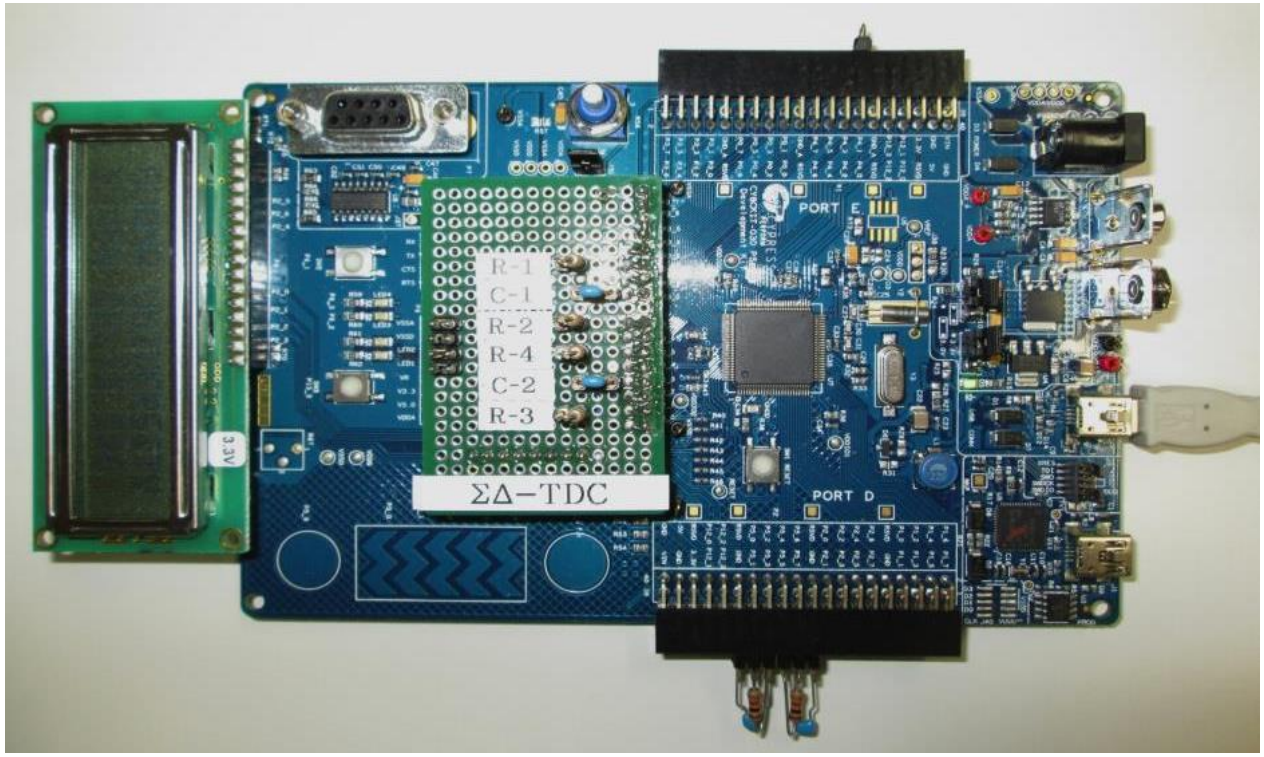


Operation of Single-Bit ΔΣ TDC

In case Dout =0



ΔΣ TDC Implementation with Analog FPGA



Analog FPGA PSoC (Programmable System on Chip) Cypress

[1] T. Chujo. H. Kobayashi, et. al.,
"Timing Measurement BOST With Multi-bit Delta-Sigma TDC",
20th IEEE International Mixed-Signal Testing Workshop,
Paris, France (June 24-26, 2015).

ΔΣ or ΣΔ ? That is a question

Delta-sigma modulator was invented by Prof. Yasuhiko Yasuda in 1960 at University of Tokyo, Japan.

Prof. Yasuda

ΔΣ Prof. Yasuda insists

ΣΔ In many IEEE papers

I use the term "ΔΣ" according to Prof. Yasuda.

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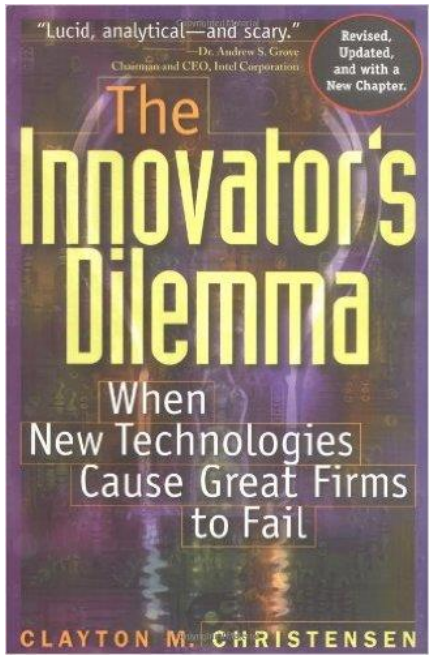
TDC Possibility for Timing BOST

- TDC can be implemented with FPGA
  - It can be realized with full digital circuit.

  ADC cannot be.
- FPGA implementation of TDC can be disruptive innovation.
- IC designers & researchers tend to be interested in full custom IC design, instead of FPGA.



Summary

- Two-step SAR TDC with self-calibration has been introduced.
- 4-types of TDCs are compared.
  - ⇨ They have their own advantages and disadvantages.
- TDC can be implemented with FPGA
  - ⇨ It can be used for timing BOST.

Time continues indefinitely.

Kobayashi Laboratory

Time is GOLD !!

TDC is a key.