ITC 2016
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INTERNATIONAL TEST CONFERENCE
November 15-17, 2016
Fort Worth Convention Center
Fort Worth, Texas

Welcome Message

It is our privilege to welcome you to the 47th International Test Conference (ITC) sponsored by IEEE and the IEEE Philadelphia Section. ITC is the world's premier conference dedicated to electronics test. Our volunteer committees worked very hard to provide to you an exciting event with a balance of the latest research, practical applications, and networking opportunities. We are holding ITC in Fort Worth, Texas the week of November 14, 2016.

Our topics include heterogeneous integration, high-speed interface, emerging devices, emerging test needs for automotive and IoT, hardware security, system test, analog and mixed-signal test, ATE, yield learning, test analytics, pre-silicon test optimization, test cost, test methodology, test standards and industrial practices.

The conference is organized in a way to provide you various methods to learn and discuss topics related to electronics test. Our **keynote** speakers are well known industry leaders and academic researchers that provide exciting insights. The **technical papers** are 20 minute presentations of papers that were selected from a rigorous review process with a few minutes for questions at the end of each paper. The **exhibition floor** consists of solutions providers who are available to discuss and learn about their offerings. A **corporate forum** is held on the exhibit floor where exhibiting companies present about their products. This year we have one **poster session** held on the exhibition floor. Posters provide a very comfortable and informal environment to discuss details with the authors.

We recognize that networking is extremely valuable to our attendees. Multiple breaks and social events are integrated in the program to allow you to network with colleagues and other specialists. Free lunches are provided in the exhibit hall for full- and one-day ITC conference attendees.

On behalf of the 2016 International Test Conference steering committee, program committee and all the dedicated volunteers who are key to making the program complete, we welcome you to this year's exciting technical program and exhibits.

Ron Press
General Chair

Li-C Wang
Program Chair

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Test Week Highlights

	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday
12 Half-Day TTTC Tutorials A great way to prepare for the ITC Technical program	●	●		●		
Five Panels		●	●		●	
Plenary Session and Keynotes			●	●	●	
74 Technical Presentations			●	●	●	
Eight Special Sessions			●	●	●	
World-Class Exhibits Free admission to exhibits floor on all days			●	●	●	
Exhibits Passport Program Visit booths and be eligible for a prize			●	●		
Corporate Forum The latest technical innovations from our exhibitors and corporate supporters			●	●		
24 Posters				●		
Two Embedded Tutorials Included within the technical paper sessions				●	●	
Two-Day Workshops Two to choose from					●	●
ITC Receptions		●	●			
Fringe Technical Meetings	●	●	●	●	●	●

Become an ITC corporate supporter or utilize marketing opportunities

http://www.itctestweek.org

www.twitter.com/itctestweek

Test Week At-a-Glance

SUNDAY, NOVEMBER 13 – HALF-DAY TUTORIALS			
8:30 a.m. – 12:00 p.m.	Tutorial1 Testing of TSV-based 2.5D- and 3D-Stacked ICs	Tutorial 2 From Data to Actions: Application of Data Analytics in Semiconductor Manufacturing and Test	Tutorial 3 Test Opportunities and Challenges for Secure Hardware and Verifying Trust in Integrated Circuits
1:00 p.m. – 4:30 p.m.	Tutorial 4 Testing of Automotive ICs: introduction and Advances	Tutorial 5 Diagnosis-driven Yield Analysis	Tutorial 6 Targeting "Zero Defect" IC Quality: Advanced Cell-aware Fault Models and Adaptive Test

MONDAY, NOVEMBER 14 – HALF-DAY TUTORIALS			
8:30 a.m. – 12:00 p.m.	Tutorial 7 Memory Test and Repair in the FinFet Era	Tutorial 8 Test, Diagnosis, and Root-Cause Identification of Failures for Boards and Systems	Tutorial 9 Mixed-Signal DFT and BIST: Trends, Principles and Solutions
1:00 p.m. – 4:30 p.m.	Tutorial10 Automotive Reliability and Test Strategies	Tutorial 11 Combining Structural and Functional Test Approaches Across System Levels	Tutorial12 Practices in High-Speed I/O Testing

MONDAY, NOVEMBER 14 – PANEL	
4:45 p.m. –6:30 p.m.	Panel 1 The Unknown Unknowns in Test

MONDAY, NOVEMBER 14 – POST-PANEL RECEPTION	
6:30 p.m. –8:00 p.m.	Post-Panel Reception/Social

TUESDAY, NOVEMBER 15 – TECHNICAL SESSIONS					
9:00 a.m. – 10:30 a.m.	Plenary – Keynote Address *The Business of Test: Test and Semiconductor Economics* Walden C. Rhines				
10:30 a.m. – 5:30 p.m.	Exhibits				
12:00 p.m. – 2:00 p.m.	Corporate Forum				
12:00 p.m. – 2:00 p.m.	Lunch				
2:00 p.m. – 4:00 p.m.	Session 1 Diagnosis	Session 2 DFT	Poster Preview Talks	Special Session 1 Test of Low/High-Power Devices	IEEE TTTC E. J. McCluskey Best Doctoral Thesis Award: Final Round
4:30 p.m. – 6:00 p.m.	Special Session 3 Test for Security and Trust	Panel 2 Phased Array 5G:Is Test Connected or Disconnected?	Panel 3 Test Cost Reduction —Is There More to Cut?	Special Session 2 3D-IC Test Standard IEEE P1838	Embedded Tutorial 1 Diagnosis to Failure Isolation: The Journey to Root Cause

TUESDAY, NOVEMBER 15 – ITC WELCOME RECEPTION	
6:30 p.m. –8:30 p.m.	ITC Welcome Reception

Test Week At-a-Glance

WEDNESDAY, NOVEMBER 16 – TECHNICAL SESSIONS					
8:30 a.m.–10:00 a.m.	Session 3 Analog I	Session 4 Memory	Session 5 Analytics I	Special Session 4 IEEE 1687.1: What, Why and How	Special Session 5 mmWave ATE HVM Technology
9:30 a.m.–4:30 p.m.	Exhibits				
10:30a.m.–12:00 p.m.	Session 6 IEEE 1687	Session 7 Analog II	Session 8 Analytics II	Session 9 Emerging Devices	Special Session 6 Heterogeneous Integration Pushes the Test Roadmap
12:00 p.m.–2:00p.m.	Poster Session - Lunch				
12:00 p.m.–2:00p.m.	Corporate Forum				
2:00 p.m.–3:30 p.m.	Session 10 Test Vehicle Design	Session 11 ATE I	Session 12 Security	Session 13 Methodology	Special Session 7 Design, Test and Reliability of STT-MRAM
4:30 p.m.–5:45 p.m.	Keynote Address in honor of E. J. McCluskey *Hardware Inference Accelerators for Machine Learning* Rob A. Rutenbar				

THURSDAY, NOVEMBER 17 – TECHNICAL SESSIONS				
9:00 a.m.–10:30 a.m.	Session 14 ATE II	Session 15 Reliability	Session 16 Test Generation	Special Session 8 Automotive IC Quality & Reliability: Today's Challenges & Solutions
9:30 a.m. – 1:30 p.m.	Exhibits			
11:00 a.m.–12:00 p.m.	Keynote Address: *Addressing Semiconductor Industry Needs: Defining the Future Through Creative, Exciting Research* Ken Hansen			
12:00 p.m.– 1:30p.m.	Lunch			

1:30 p.m.– 3:00 p.m.	Session 17 Mixed-Signal	Session 18 Practices	Panel 4 ATE Revisited – Where Are We Today and Where Should We Be Heading?	Embedded Tutorial 2 ISO 26262	Panel 5 Test, Validation and Security for IoTs

THURSDAY, NOVEMBER 17 – WORKSHOPS		
4:00 p.m. – 4:30 p.m.	Opening Address	
4:30 p.m. – 6:30 p.m.	Automotive Reliability and Test	Defects, Adaptive Test and Data Analysis
7:00 p.m. – 9:00 p.m.	Workshop Reception	

FRIDAY, NOVEMBER 18 – WORKSHOPS		
8:00 a.m. – 4:00 p.m.	Automotive Reliability and Test	Defects, Adaptive Test and Data Analysis

TTTC Half-Day Tutorials

TTTC TEST TECHNOLOGY EDUCATION PROGRAM (TTEP) 2016

The Tutorials & Education Group of the IEEE Computer Society Test Technology Technical Council (TTTC) organizes a comprehensive set of Test Technology Tutorials to be held in conjunction with several TTTC-sponsored technical meetings worldwide. The mission of the Test Technology Educational Program (TTEP) is to serve test and design professionals by offering fundamental education and expert knowledge in state-of-the-art test technology topics. TTEP offers tutorial participants the opportunity to earn official certification from IEEE Computer Society TTTC. Each half-day tutorial corresponds to two TTEP units. Upon completion of 16 TTEP units, official recognition in the form of an IEEE TTTC Test Technology Certificate will be presented to the participant. For further information regarding TTEP, please visit http://ttep.tttc-events.org/ttep/index.html

At ITC 2016, TTTC/TTEP is pleased to present 12 **half-day tutorials** on topics of current interest to test professionals and researchers. All tutorials qualify for credit towards IEEE TTTC certification under the TTEP program. Six tutorials are held on Sunday, November 13. Six tutorials will be held on Monday, November 14.
The **one-day** tutorial registration fee is for two tutorials—a morning tutorial and afternoon tutorial, both on the same day, e.g., Tutorial 1 and Tutorial 4 on Sunday. You may register for up to four tutorials (two consecutive on Sunday and two consecutive on Monday).
The **all-access pass** tutorial registration provides in-and-out access to all twelve tutorials over both days.
(see registration page or http://www.itctestweek.org for further information). *Admission for onsite registrants is subject to availability.*

Tutorial attendees receive study material, breaks and lunches on the days attended. Tutorial registration, coffee and pastry are available at 7:00 a.m. on Sunday and Monday.

Sunday 8:30 a.m. – 12:00 p.m.

TUTORIAL 1

Testing of TSV-based 2.5D- and 3D-Stacked ICs

Presenters EJ. Marinissen, K. Chakrabarty

Summary Stacked ICs with vertical interconnects containing fine-pitch micro-bumps and through-silicon vias (TSVs) are a hot-topic in design and manufacturing communities. These 2.5D- and 3D-SICs hold the promise of heterogeneous integration, inter-die connections with increased performance at lower power dissipation, increased yield and decreased product cost. This tutorial presents key concepts in 3D technology, terminology, and benefits. We discuss design, test challenges and emerging solutions for 2.5D- and 3D-SICs. Covered topics include overview of 3D integration and trend-setting products such as 2.5D-FPGA, 3D-stacked memory chips, test flows and test content for 3D chips, advanced wafer probing, 3D design-for-test architectures and ongoing IEEE P1838 standardization, and 3D test cost modeling and test-flow selection.

Intended Audience Test and design-for-test engineers and their managers; researchers, university professors, and students; test methodology developers; test-automation tool developers.

TUTORIAL 2

From Data to Actions: Applications of Data Analytics to Semiconductor Manufacture and Test

Presenters H. Stratigopoulos, Y. Makris

Summary This tutorial seeks to elucidate the utility of data analytics in semiconductor manufacturing and test. Relevant concepts from data analytics theory will be introduced and agglomerated with current practice, showcasing effectiveness on actual case studies with industrial data. A comprehensive survey of the relevant literature will be provided, organized around four themes: (i) Test cost reduction through replacement of expensive tests by inexpensive alternatives and/or elimination of superfluous, either statically or adaptively during application, (ii) Pre-deployment evaluation of candidate test methods through probabilistic test metrics, (iii) Post-production performance calibration through cost-effective knob tuning, and (iv) Yield learning and process monitoring through analysis of process variation impact on wafer-level spatial correlation.

TUTORIAL 3

Test Opportunities and Challenges for Secure Hardware and Verifying Trust in Integrated Circuits

Presenters *D. Forte, M. Tehranipoor*

Summary The migration from a vertical to horizontal business model has made it easier to introduce vulnerabilities to electronic component design and supply chain. This tutorial discusses the major issues including securing hardware, verifying trustworthiness of ICs, unique key generation, side-channel attacks and will place emphasis on detection/prevention of hardware Trojans and counterfeit electronic parts and how test can help. (i) Introduction to hardware security and trust (physically unclonable functions, true random number generation, hardware Trojans, counterfeit ICs, side-channel attacks, supply chain vulnerabilities), (ii) Background and motivation for hardware Trojan and counterfeit prevention/detection; (iii) Taxonomies related to both topics; (iv) Existing solutions; (v) Open test challenges; (vi) Design for security and trust, (vii) New and unified solutions.

Intended Audience This tutorial is perfect for either those who are beginners or those who have been involved in hardware security for several years.

TTTC Half-Day Tutorials

Sunday 1:00 p.m. – 4:30 p.m.

TUTORIAL 4
Testing of Automotive ICs: Introduction and Advances

D. Appello, O. Ballan, E. Sanchez

Summary Electronics content in the car is constantly growing. On top of traditional applications for engine control, transmission, braking/steering, passive safety, body and dashboard also multimedia, advanced driver assistance and car2X segments are rapidly growing. The stability and extended duration in manufacturing of these components makes them very attractive for the industry. Extreme product quality achieved with very low cost is the key challenge. The proposed tutorial covers a broad range of topics which are defining the testability, testing and manufacturing requirements of automotive products. Advanced topics like testing of safety critical and secure devices are proposed beside more traditional topics like testability, test development, qualification, industrialization, burn-in and manufacturing. Relevant industrial cases will be proposed to participants.

Intended Audience: Test and product engineers, designers and DFT engineers, quality engineers, student and researchers in the area of test and testability

TUTORIAL 5
Diagnosis-driven Yield Analysis

Presenters W-T. Cheng, W. Yang, Y. Huang

Summary Delivering a stable high-yield product on time is the ultimate goal for the semiconductor industry. Reaching this goal becomes more and more difficult, especially when cell internal defects become prevalent. The main challenges in the yield analysis process are to identify the systematic issues, find their root causes and select associated devices with the identified systematic defects for further validation by physical failure analysis. This tutorial discusses the methodologies that improve yield of digital semiconductor devices through scan-based test, volume diagnosis and diagnosis-driven yield analysis (DDYA). This gives engineers who work on yield improvement a very fast and highly effective way of defect localization and identification, complementing their traditional and hardware-based methods.

Intended Audience: Engineers and managers responsible for design, test, quality or yield of a product; Engineers and managers responsible for product engineering and technology bring-up; Failure analysis lab engineers & managers; Engineers involved in manufacturing production or process development; Anyone involved with the financial impact of low yield or low product quality.

TUTORIAL 6
Targeting "Zero Defect" IC Quality: Advanced Cell-aware Fault Models and Adaptive Test

Presenter A. Singh

Summary Commercial applications continue to demand ever higher IC quality, most notably a “zero defect” target from automotive manufacturers. However, recent experience with new Cell Aware Tests suggests that current structural tests can miss significant defectivity. This two-part tutorial presents a detailed study of the state-of-the-art techniques directed at targeting “Zero-Defect” IC quality. In part one we explain new fault models, including the Cell Aware methodology, for an in-depth understanding of the actual defects in modern standard cells that are missed by stuck-at and TDF tests but detected by the new tests. Part two introduces innovative statistical adaptive techniques that improve test effectiveness by optimizing the test applied to individual parts.

Intended Audience: Test researchers and academics, DFT managers and engineers, EDA test/DFT tool developers, test and reliability managers and engineers, automotive electronics managers and engineers.

TTTC Half-Day Tutorials

Monday 8:30 a.m. – 12:00 p.m.

TUTORIAL 7
Memory Test and Repair in the FinFET Era

Presenter Y. Zorian

Summary Recent growth in content creation has led to an explosion in the use of embedded memories. This tutorial will present the trends and challenges of growing memory content on chip and how to ensure detection of today's defects upon manufacturing and during life time, including process variation and FinFET-specific defects reaching 7-nm level. BIST and repair solutions to address yield optimization, endurance and data retention of failure modes will be presented. Given the tens of thousands of embedded memory instances in today's SOCs, the tutorial will also cover power management constraints, functional timing implications, test scheduling optimization and area minimization options.
Intended Audience DFT, test and reliability engineers, engineering managers, reliability and quality assurance managers, researchers and research students.

TUTORIAL 8
Test, Diagnosis and Root-Cause Identification of Failures for Boards and Systems

Presenters K. Chakrabarty, W. Eklow

Summary The gap between working silicon and a working board/system is becoming more significant and problematic as technology scales and complexity grows. The result of this increasing gap is failures at the board and system level that cannot be duplicated at the component level. These failures are most often referred to as "NTFs" (No Trouble Founds). The result of these NTFs can range from higher manufacturing costs and inventories to failure to get the product out of the door. This tutorial provides a detailed background on the nature of this problem and will provide DFT, test, and root-cause identification solutions at board/system level. Practical insights from industry case studies will be highlighted, and recent research from academia can help solving these problems.
Intended Audience Board/System designers, Board/system test engineers and their managers, researchers, test methodology developers, and test tool developers.

TUTORIAL 9
Mixed-Signal DFT and BIST: Trends, Principles and Solutions

Presenter S. Sunter

Summary We analyze recent trends in IC processes and design, and implications for test, then look at trends in testing. Next, we discuss trends in ad hoc DFT and fault simulation, then all relevant IEEE DFT standards: 1149.1, .4, .6, .7, .8, P1149.10 and 1687. The trend analysis concludes with a review of BIST techniques. Addressed circuits include PLL/DLL, ADC/DAC, SerDes/DDR, general I/Os and last, but not least, random analog. Next, seven essential principles of practical analog BIST are presented. Lastly, we discuss practical DFT techniques, ranging from analog defect simulation and the classic analog bus, to oversampling and undersampling methods that greatly improve range, resolution and reusability.
Intended Audience Designers, DFT engineers, test engineers, and managers responsible for analog/mixed-signal/HSIO functions in SoCs.

Monday 1:00 p.m. – 4:30 p.m

TUTORIAL 10
Automotive Reliability and Test Strategies

Presenters R. Mariani, N. Nandra Y. Zorian

Summary Given the fast-growing automotive semiconductor industry, this tutorial will discuss the implications of automotive test, reliability and functional safety requirements on all aspects of the SOC lifecycle: design, silicon bring up, volume production and, particularly, in the field test. Automotive safety-critical chips that need multiple field test strategies, such as power-on self-test, periodic in-system self-test and error correction will also be covered. The tutorial will discuss how incorporating self-test and repair infrastructure with high-efficiency capabilities can help minimize the impact on power, performance and area, while addressing the need for less than 10 DPPM. The benefits of selecting an ISO 26262-certified IP to ensure functional safety requirements, while accelerating time to market for SOCs.
Intended Audience DFT, test, reliability, and functional safety engineers, engineering managers, reliability and quality assurance managers, researchers and research students.

TUTORIAL 11
Combining Structural and Functional Test Approaches Across System Levels

Presenters A. Jutman, H-J. Wunderlich

Summary This tutorial introduces into the best practices, current challenges and advanced techniques of high-quality system-level test and diagnosis. Specialized techniques and industrial standards of testing complex systems (which may correspond to a system-on-chip, board or interconnected system) are introduced. The reuse for system test of design-for-test structures and test data developed at module level is discussed, including the limitations and research challenges. Structural test methods have to be complemented by functional methods; hence, state-of-the-art and leading edge research for functional testing are covered. Solutions change depending on the scenario (manufacturing test or in-field test) and the goal (test or diagnosis). The tutorial also discusses the role of standards and regulations in the area.
Intended Audience Professionals who want to extend their horizon in the complementary test domain learning best practices in the areas of board and IC testing.

TUTORIAL 12
Practices in High-Speed I/O Testing

Presenters S. Abdennadher, S. Shaikh

Summary This tutorial presents the existing industrial techniques to meet the ever-increasing test complexity of high-speed IO's (HSIO). It first describes the basic design of both serial and parallel HSIOs, and then presents various testing methods of HSIO, such as timing margining, voltage margining, compensation testing, leakage testing, etc. The examples of all these test methods will be presented with special emphasis on DFT and BIST-based approaches of HSIO testing and their suitability to the production-level environment.
Intended Audience This tutorial is most suitable for design, test and DFT engineers involved in actual implementation of high-speed I/O-based systems. The architects and engineering managers would also greatly benefit from this tutorial.

Exhibits

Visit the exhibition that includes the latest high-technology test, design and service products.

Exhibits hours: Tuesday 10:30 a.m. – 5:30 p.m.
Wednesday 9:30 a.m. – 4:30 p.m., Thursday 9:30 a.m. – 1:30 p.m.

FREE ADMISSION TO EXHIBITS

ITC is offering free exhibits-only registration to visit the exhibit hall during all exhibit hours. Onsite registration for this special opportunity begins on Tuesday at the ITC registration area in the Fort Worth Convention Center. Lunch is not included with free exhibits-only admission.

Fill in your Exhibit Hall Passport for a Special ITC Prize.

All registered attendees will receive a passport in their conference bag. Get your passport stamped Tuesday and Wednesday while visiting exhibitor booths and at least one Corporate Forum session. Drop your completed passport into the collection box located in the exhibit hall, and be eligible for the drawing at 4:00 p.m. on Wednesday in the exhibit hall. You need not be present at the time of drawing to win.

Please see the full instructions included with your passport for details.

Participating Exhibitors*

Advantest
Aehr Test Systems, Inc.
Alliance ATE Consulting Group, Inc.
Aries Electronics, Inc.
Astronics Test Systems
Averna
Chroma ATE, Inc.
CMR Summit Technologies
COHU ITS
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Keysight Technologies
Marvin Test Solutions, Inc.
Mentor Graphics
MFG Vision
Micro Control Company
NHK Spring Company
NXP Smarter World Display
Optimal+
PDF Solutions, Inc.
Pickering Switching Solutions
ProbeLogic
Qualtera
Roos Instruments
R&D Altanova
Sager Electronics
SiliconAid Solutions
STAr Technologies
Synopsys, Inc.
TDK-Lamda Americas
Teradyne Global Services Organization
TESEC
Test Insight Ltd
Test Technology Technical Counsel (TTTC)
TSSI
Versatile Power
Winter Logic
XJTAG
Yamaichi Electronics USA, Inc.
yieldWerx Semiconductor

* As of publication date

Corporate Forum

The Corporate Forum track will be on Tuesday and Wednesday in a comfortable meeting area adjacent to the exhibits floor. This will make it easier for ITC exhibit attendees to drop in to see forum presentations. It provides our exhibitors and supporters an opportunity to present the latest developments from their companies, and to promote their activities at ITC.

Our Diamond Supporter, Optimal+ plans to provide a one-hour presentation Tuesday morning followed by a hosted lunch. The remaining presentations will start at 12:00 p.m. at 20-minute intervals, spread across Tuesday and Wednesday to minimize conflict with the conference technical program. The 20-minute length allows attendees to enjoy multiple presentations in a short time span and runs at a fast pace to keep this event more interesting.

A. Downey, Chair

Tuesday 11:00 a.m.–12:00 p.m.

11:00 a.m. Diamond Supporter Event
Optimal+

Tuesday 12:00 p.m.–2:00 p.m.

12:00 p.m. GOEPEL Electronics

12:20 p.m. Mentor Graphics

12:40 p.m. Roos Instruments

1:00 p.m. yieldWerx

1:20 p.m. Advantest

1:40 p.m. Defacto Technologies

Wednesday 12:00 p.m.–2:00 p.m.

12:00 p.m. DR YIELD

12:20 p.m. MFG Vision

12:40 p.m. Marvin Test Solutions

1:00 p.m. Test Insight

1:20 p.m. PDF Solutions

1:40 p.m. Synopsys

Plenary & Keynote Address

Tuesday 9:00 a.m. – 10:30 a.m.

Opening Remarks
Ron Press, *ITC General Chair*

ITC 2016 Program Introduction
Li-C Wang, *ITC 2016 Program Chair*

ITC 2014 and 2015 Paper Awards Presentation
Bill Eklow, ITC 2015 Program Chair

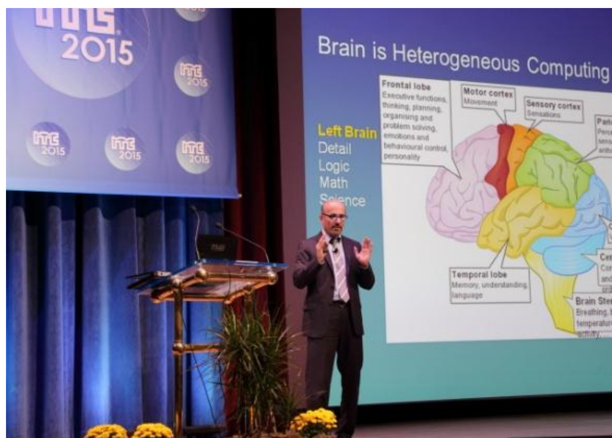
TTTC Awards Presentation
Yervant Zorian, *TTTC President*

Keynote Address
The Business of Test: Test and Semiconductor Economics

Walden C. Rhines, *Chairman and Chief Executive Officer, Mentor Graphics*

Test methodology changes have historically been driven largely by necessity—critical needs for cost reduction or quality improvements. This history makes possible the prediction of future changes. Dr. Rhines will review the driving forces for prior discontinuities in design-for-test, analyze the rates of adoption of new test methodologies, and discuss the likely forces that will change our test priorities in the future.

About the speaker Walden C. Rhines is Chairman and Chief Executive Officer of Mentor Graphics, a leader in worldwide electronic design automation with revenue of $1.2 billion in 2015. During his tenure at Mentor Graphics, revenue has nearly quadrupled and Mentor has grown the industry's number one market share solutions in four of the ten largest product segments of the EDA industry. He joined Mentor in 1993 from Texas Instruments (TI) where he was most recently Executive Vice President in charge of TI's semiconductor business. Rhines has served five terms as Chairman of the Electronic Design Automation Consortium. He is also a board member of the Semiconductor Research Corporation and First Growth Children and Family Charities. He received a BSE degree from the University of Michigan, an MS and Ph.D. from Stanford University, an MBA from Southern Methodist University and Honorary Doctor of Technology degrees from Nottingham Trent University and the University of Florida.



Wednesday Keynote

4:30 p.m. – 5:45 p.m.

Special Keynote in Honor of Professor Edward J. McCluskey*

Hardware Inference Accelerators for Machine Learning

Rob A. Rutenbar, *Professor, University of Illinois at Urbana-Champaign*

Machine learning (ML) technologies have revolutionized the ways in which we interact with large-scale, imperfect, real-world data. As a result, there is rising interest in opportunities to implement ML efficiently in custom hardware. We have designed hardware for one broad class of ML techniques: Inference on Probabilistic Graphical Models (PGMs). In these graphs, labels on nodes encode what we know and "how much" we believe it; edges encode belief relationships among labels; statistical inference answers questions such as "if we observe some of the labels in the graph, what are most likely labels on the remainder?" These problems are interesting because they can be very large (e.g., every pixel in an image is one graph node) and because we need answers very fast (e.g., at video frame rates). Inference done as iterative Belief Propagation (BP) can be efficiently implemented in hardware, and we demonstrate several examples from current FPGA prototypes. We have the first configurable, scalable parallel architecture capable of running a range of standard vision benchmarks, with speedups up to 40X over conventional software. We also show that BP hardware can be made remarkably tolerant to the low-level statistical upsets expected in end-of-Moore's-Law nanoscale silicon and post-silicon circuit fabrics, and summarize some effective resilience mechanisms in our prototypes.

* Special tributes to Professor McCluskey will be presented from 5:30 p.m. to 5:45 p.m.

About the speaker: Rob A. Rutenbar received the Ph.D. degree from the University of Michigan, Ann Arbor, in 1984. From 1984 to 2009, he was faculty at Carnegie Mellon, where he held the Stephen J. Jatras (E'47) Chair in Electrical and Computer Engineering. In 2010 he joined the University of Illinois at Urbana-Champaign, where he is currently the Abel Bliss Professor and Head of Computer Science. His research has focused in three broad areas: tools for a variety of IC design problems; methods to manage the messy statistics of nanoscale chip designs; and custom silicon architectures for challenging tasks such as speech recognition and machine learning. His work has been featured in venues ranging from EETimes to the Economist magazine. He is a Fellow of the ACM and IEEE.

Keynote Thursday 11:00 a.m. – 12:00 p.m.

Addressing Semiconductor Industry Needs: Defining the Future Through Creative, Exciting Research

Ken Hansen, *CEO, Semiconductor Research Corporation*

In the history of the semiconductor industry, there has been no other period in time with as much uncertainty in the way forward. But with uncertainty comes great opportunity. There is a need for transformative innovation fueled by breakthrough research to reinvigorate the growth of the industry. This talk will identify some of the new exciting challenges the industry is facing and research areas where investment is needed to address them. Systems of the future—autonomous vehicles, internet of things, self-adaptive configurations modeled on biology—will require advanced techniques to test them, secure them, reduce their power, and produce them without error. This increase in complexity coupled, with a decreasing ability to rely on deterministic circuits, requires new approaches to be created by cross-disciplinary teams co-optimizing across the entire design hierarchy space.

About the speaker: Ken Hansen joined Semiconductor Research Corporation as its President and CEO in June 2015. Ken brings his experience as the former Vice President and Chief Technology Officer with Freescale Semiconductor. Prior to becoming CTO at Freescale, Ken was Vice President and led Freescale's Chief Development Office where he improved design efficiency and reduced product cost for all Freescale business units. Previously, he held several senior technology and management positions at Freescale and Motorola leading research and development teams. He received the BSEE and MSEE degrees from the University of Illinois where he also has been recognized as an ECE and College of Engineering Distinguished Alumni, is a Fellow of the IEEE, and holds 11 U.S. patents. Ken is an industry veteran, with 40 years of experience in technical management and system/circuit design, primarily in the area of wireless communications.

2:00 p.m. – 4:00 p.m.

SESSION 1
Diagnosis
P. Song, IBM (Chair)
A. Gattiker, IBM (Discussant)

1.1 Diagnostic Resolution Improvement with Active Learning-guided Physical Failure Analysis
Y. Xue, X. Li, R. Blanton, Carnegie Mellon University

1.2 A Novel Diagnostic Test Generation Methodology and Its Application in Production Failure Isolation
E. Amyeen, D. Kim, M. Chandrasekar, M. Noman, S. Venkataraman, A. Jain, N. Goel, R. Sharma, Intel

1.3 Handling Wrong Mapping: A New Direction Towards Better Diagnosis with Low Pin Convolution Compressors
S. Kundu, P. Bhattacharya, R. Kapur, Synopsys

1.4 Using Symbolic Canceling to Improve Diagnosis from Compacted Response
K. Saleem, N. Touba, The University of Texas at Austin

SESSION 2
DFT
P. Wohl, Synopsys (Chair)
V, Chickermane, Cadence Design Systems (Discussant)

2.1 Test Point Insertion in Hybrid Test Compression/LBIST Architectures
J. Tyszer, J. Zawada, Poznan University of Technology; *N. Mukherjee, J. Rajski, E. Moghaddam,* Mentor Graphics

2.2 A Unified Test and Fault-tolerant Multicast Solution for Network-on-Chip Designs
D. Xiang, Tsinghua University; *K. Chakrabarty,* Duke University; *H. Fujiwara,* Osaka Gakuin University

2.3 Putting Wasted Clock Cycles to Use: Enhancing Fortuitous Cell-aware Fault Detection with Scan Shift Capture
F. Zhang, D. Hwong, Y. Sun, A. Garcia, S. Alhelaly, J. Dworak, Southern Methodist University; *G. Shofner, L. Winemberg,* NXP Semiconductors

2.4 Minimal-Area Test Points for Deterministic Patterns
J. Tyszer, Poznan University of Technology; *Y. Liu, S. Reddy,* University of Iowa; *E. Moghaddam, N. Mukherjee, J. Rajski,* Mentor Graphics

* Invited Talk

POSTER PREVIEW TALKS
W. Eklow, (Chair)

Presenters of posters at tomorrow's noon-time poster session in the exhibit hall will give short previews of their work.

SPECIAL SESSION 1
Test of Low/High-Power Devices
V. Devanathan, Texas Instruments (Chair)
H. Kobayashi, Gunma University (Discussant)

S1.1* DFT Test Considerations for Low-Power Devices
T. Mclaurin, ARM

S1.2* Scan-based Low Power Test Generation
X. Lin, Mentor Graphics

S1.3* Got the Power? Test and DFT of Mobile Power Management ICs (PMICs)
H. von Staudt, Dialog Semiconductor

S1.4* Transient Testing of Integrated Power Output Stages
W-T. Ng, University of Toronto

IEEE TTTC E. J. McCLUSKEY BEST DOCTORAL THESIS AWARD: FINAL COMPETITION
K. Huang. University of Texas at Dallas (Chair)

TC1 Memory Repair for High Fault Rates
P. Papavramidou, TIMA, Grenoble

TC2 Output Bit Selection Methodology for Test Response Compaction
W-C. Lien, K-J. Lee, National Cheng Kung University

TC3 Testing of Interposer-based 2.5D Integrated Circuits
R. Wang, Duke University

TC4 TBA
***E. Chielle,* Federal University of Rio Grande Do Sul**

4:30 p.m. – 6:00 p.m.

SPECIAL SESSION 2
3D-IC Test Standard IEEE P1838
E. J. Marinissen, IMEC (Chair)
A. Cron, Synopsys (Discussant)

S2.1* P1838 Overview
E. J. Marinissen, IMEC

S2.2* Serial Control Mechanism
A. Crouch

S2.3* Die Wrapper Register
T. McLaurin, ARM

S2.4* Flexible Parallel Port
A. Cron, Synopsys

S2.5* Description Languages
S. Behatia, Google

SPECIAL SESSION 3
Test for Security and Trust
M. Tehranipoor, University of Florida (Chair)

S3.1* The Enemies of IC Security and Trust and How to Test Them
B. Swarup, University of Florida

S3.2* Is Automated Testing the Panacea Cryptography Needs to Deliver Promised Security Assurances?
A. Vassilev, NIST

S3.3* Hardware Security Assurance: Challenges and Opportunities
A. Khatibzadeh, Intel

EMBEDDED TUTORIAL 1
Diagnosis to Failure Isolation: The Journey to Root Clause
R.Guo, Synopsys (Chair)
E. Amyeen, Intel (Organizer)

Isolation of manufacturing defects drives yield learning for process improvement and is critical for enabling Moore's law and nanoscale technology scaling. In this tutorial, we will review approaches to improve resolution and precision of diagnosis for better defect isolation, cover optical, electrical probing techniques, and failure analysis case studies.

TUT1.1* The Journey to Root Cause—Part I
E. Amyeen, Intel

TUT1.2* The Journey to Root Cause—Part II
A. Maldonado, Intel

Discussants

The discussion at the end of every technical paper presentation is an enhancement of the traditional Q&A activity. It is led by a distinguished member of the test community, who we refer to as the discussant. The discussant will contribute insightful questions and inspire discussions around the topic of the presentation, while sharing the Q&A microphone with session attendees. Key takeaways are sure to emerge from every talk, above and beyond what is available by going through electronic copies of papers or presentations after the conference.

Wednesday Morning

8:30 a.m. – 10:00 a.m.

SESSION 3
Analog I
E. Basker, Texas Instruments (Chair)
H. Stratigopoulos, Sorbonne Universités (Discussant)

3.1 Analog Fault Coverage Improvement Using Final-Test Dynamic Part Average Testing
W. Dobbelaere, R. Vanhooren, W. De Man, K. Matthijs, ON Semiconductor; *A. Coyette, B. Esen, G. Gielen,* KU Leuven

3.2 Effective DC Fault Models and Testing Approach for Open Defects in Analog Circuits
B. Esen, A. Coyette, G. Gielen, KU Leuven; *W. Dobbelaere, R. Vanhooren,* ON Semiconductor

3.3 Fault Simulation for Analog Test Coverage
J. Sequeira, S. Natarajan, P. Goteti, N. Chaudhary, Intel

SESSION 4
Memory
V. Chandra, ARM (Chair)
R, Aitken, ARM (Discussant)

4.1 Defect Tolerance for CNFET-based SRAMs
T. Li, Spreadtrum Communications; *L. Jiang, X. Liang,* Shanghai Jiao Tong University; *Q. Xu,* Chinese University of Hong Kong; *K. Chakrabarty,* Duke University

4.2 A Built-in Self-Repair Scheme for DRAMs with Spare Rows, Columns, and Bits
C-S. Hou, Y-X. Chen, J-F. Li, National Central University; *C-Y. Lo, D-M. Kwai, Y-F. Chou,* Industrial Technology Research Institute

4.3 EMACS: Efficient MBIST Architecture for Test and Characterization of STT-MRAM Arrays
I. Yoon, A. Chintaluri, A. Raychowdhury, Georgia Institute of Technology

SESSION 5
Analytics I
S. Blanton, Carnegie Mellon University (Chair)

5.1 Statistical Outlier Screening As a Test Solution Health Monitor
D. Shaw, K. Butler, D. Hoops, A. Nahar, Texas Instruments

5.2 Accurate Anomaly Detection Using Correlation-based Time-Series Analysis in a Core Router System
S. Jin, K. Chakrabarty, Duke University; *Z. Zhang,* Spreadtrum; *X. Gu,* Huawei Technologies Co.

5.3 Harnessing Process Variations for Optimizing Wafer-level Probe-Test Flow
A. Ahmadi, C. Xanthopoulos, Y. Makris, UT Dallas; *A. Nahar, B. Orr, M. Pas,* Texas Instruments

SPECIAL SESSION 4
IEEE 1687.1: What, Why and How
M. Portolan, TIMA (Chair)
E. Larsson, Lund University (Discussant)

S4.1* Extending the Application of IEEE 1687
T. Waayers, **NXP**

S4.2* P1687.1—Beyond the TAP
N. Parimi, Intel

S4.3* Opening New Portals to IJTAG Networks
J. Rearick, AMD

SPECIAL SESSION 5
mmWave ATE HVM Technology
B. Bartlett, Advantest (Chair)

S5.1* TBD
T. Smith, Phoenix Test Arrays

S5.2* TBD
J. Shelley, Xcerra

S5.3* TBD
R. McAleenan, Advantest

10:30 a.m. – 12:00 p.m.

SESSION 6
IEEE 1687
X. Gu (Chair)
W. Eklow (Discussant)

6.1 A Suite of IEEE 1687 Benchmark Networks
A. Tsertov, A. Jutman, S. Devadze, Testonica Lab; *M. Reorda, R. Cantoro, M. Montazeri,* Politecnico di Torino; *E. Larsson, F. Ghani Zadegan,* Lund University

6.2 Accessing 1687 Systems Using Arbitrary Protocols
M. Portolan, TIMA

6.3 Upper-Bound Computation for Optimal Retargeting in IEEE 1687 Networks
F. Zadegan, E. Larsson, Lund University; *R. Krenz-Baath,* Hochschule Hamm-Lippstadt

SESSION 7
Analog II
M. Slamani, GLOBALFOUNDRIES (Chair)

7.1 Low-Cost Ultra-Pure Sine Wave Generation with Self Calibration
Y. Zhuang, D. Chen, Iowa State University; *A. Unnithan, A. Joseph, S. Sudani, B. Magstadt,* Texas Instruments

7.2 RF Test Accuracy and Capacity Enhancement on ATE for Silicon TV Tuners
Y. Fan, A. Verma, Y. Su, L. Rose, J. Janney, V. Do, S. Kumar, Silicon Labs

7.3 Enabling External Loopback At-Speed HVM Test Using Production Parametric Load-Board
S. Arora, A. Aflaki, S. Biswas, M. Shimanouchi, Intel

SESSION 8
Analytics II
Y. Makris, University of Texas at Dallas (Chair)

8.1 What We Know After Twelve Years Developing and Deploying Test Data Analytics
K. Butler, A. Nahar, Texas Instruments; *R. Daasch,* Portland State University

8.2 Supply-Voltage Optimization to Account for Process Variations in High-Volume Manufacturing Testing
G. Kadam, M. Rudack, J. Alt, Intel; *K. Chakrabarty,* Duke University

8.3 Variation and Failure Characterization Through Pattern Classification of Test Data From Multiple Test Stages
C-K. Hsu, K-T. Cheng, UCSB; *P. Sarson, F. Leisenberger, G. Schatzberger,* ams; *J. Carulli, S. Siddhartha,* GLOBALFOUNDRIES

SESSION 9
Emerging Devices
S. Adham, TSMC (Chair)

9.1 Built-in Self-Test for Microelectrode-Dot-Array Digital Microfluidic Biochips
Z. Li, K. Chakrabarty, Duke University; *K-T. Lai, P-H. Yu, C-Y. Lee,* National Chiao Tung University; *T-Y. Ho,* National Tsing Hua University

9.2 Online Slack-Time Binning for IO-Registered Die-to-Die Interconnects
C-C. Zheng, T-C. Wang, S-Y. Huang, S-K. Lu, National Tsing Hua University; *H. Tsai, W-T. Cheng,* Mentor Graphics

9.3* TBA
J. Ferrario, Global Foundries

SPECIAL SESSION 6
Heterogeneous Integration Pushes the Test Roadmap
D. Armstrong, Advantest (Chair)
T. M. Mak, Consultant (Discussant)

S 6.1* Moore's Law is Done and Heterogeneous Integration is Taking Off
D. Armstrong, Advantest

S 6.2* Probe Challenges Are Changing Rapidly
M. Loranger, FormFactor

S 6.3* Test and Supply Chain Challenges for Heterogeneous Integration
W. Eklow

*Invited Talk

Wednesday Afternoon

2:00 p.m. – 3:30 p.m.

SESSION 10
Test Vehicle Design
S. Venkataraman, Intel (Chair)

10.1 Logic Characterization Vehicle Design Reflection via Layout Rewiring
P. Fynan, Z. Liu, B. Niewenhuis, S. Mittal, R. Blanton, Carnegie Mellon University; *M. Strojwas,* PDF Solutions

10.2 Test Chip Design for Optimal Cell-aware Diagnosability
S. Mittal, Z. Liu, B. Niewenhuis, R. Blanton, Carnegie Mellon University

10.3* TBA
M. Bourland, Qualcomm

SESSION 11
ATE I
R. Arnold, Infineon Technologies (Chair)

11.1 Mixed-Signal ATE Technology and Its Impact on Today's Electronic System Platforms
G. Roberts, McGill University

11.2 Known-Good-Die Test Methods for Large, Thin, High-Power Digital Devices
D. Armstrong, Advantest; *G. Maier,* IBM

11.3 Test-Time-efficient Group Delay Filter Characterization Technique Using a Discrete Chirped Excitation Signal
P. Sarson, ams

SESSION 12
Security
J. Dworak, Southern Methodist University (Chair)

12.1 Securing Digital Microfluidic Biochips by Randomizing Checkpoints
J. Tang, R. Karri, New York University; *M. Ibrahim, K. Chakrabarty,* Duke University

12.2 Machine Learning-based Defense Against Process-aware Attacks on Industrial Control Systems
A. Keliris, H. Salehghaffari, B. Cairl, P. Krishnamurthy, F. Khorrami, New York University; *M. Maniatakos,* New York University Abu Dhabi

12.3 Recycled FPGA Detection Using Exhaustive LUT Path Delay Characterization
M. Alam, M. Tehranipoor, D. Forte, University of Florida

* Invited Talk

SESSION 13
Methodology
V. Chickermane, Cadence Design Systems (Chair)

13.1 Advanced Test Methodology for Complex SoCs
P. Jagannadha, M. Yilmaz, M. Sonawane, S. Chadalavada, S. Sarangi, B. Bhaskaran, A. Abdollahian, NVIDIA

13.2* The DFT Challenges and Solutions for the ARM Mali-Mimir GPU
T. McLaurin, P. Kulkarni, ARM

SPECIAL SESSION 7
Design, Test and Reliability of STT-MRAM
M. Tahoori, Karlsruhe Institute of Technology (Chair)

S 7.1* STTRAM Overview—Circuit and Architecture Perspective
H.Naeimi, Intel

S 7.2* BIST Design for Characterization and Testing of Embedded STT-MRAM
S. Adham, TSMC

S 7.3* Tailoring Design and Test Methodologies to Validate STT-MRAM as High-Performance Nonvolatile RAM
S. Kang, Qualcomm

Free Exhibits Admission Tuesday, Wednesday and Thursday

9:00 a.m. – 10:30 a.m.

SESSION 14
ATE II
G. Roberts, McGill University (Chair)

14.1 Power Supply Impedance Emulation to Eliminate Overkills and Underkills due to the Impedance Difference between ATE and Customer Board
T. Nakura, N. Terao, R. Ikeno, T. Iizuka, K. Asada, the University of Tokyo; *M. Ishida, T. Kusaka,* Advantest

14.2 I-Q Signal Generation Techniques for Communication IC Testing and ATE Systems
M. Murakami, H. Kobayashi, T. Miki, J. Kojima, Gunma University; *S. Mohyar,* Universiti Malaysia Perlis; *O. Kobayashi,* D-Clue Technologies

14.3 Novel Crosstalk Evaluation Method for High-Density Signal Traces Using Clock Waveform Conversion Technique
T. Nakamura, K. Asami, Advantest

SESSION 15
Reliability
L. Winemberg, NXP Semiconductor (Chair)

15.1 BIST-RM: BIST-Assisted Reliability Management of SoCs Using On-Chip Clock Sweeping and Machine Learning
M. Sadi, G. Contreras, M. Tehranipoor, University of Florida; *D. Tran, J. Chen, L. Winemberg,* NXP Semiconductors

15.2 Efficient Cross-Layer Concurrent Error Detection In Nonlinear Control Systems Using Mapped Predictive Check States
S. Banerjee, A. Chatterjee, Georgia Institute of Technology; *J. Abraham,* University of Texas at Austin

15.3 Cross-Layer System Reliability Assessment Against Hardware Faults
A. Vallero, A. Savino, G. Politano, S. Di Carlo, Politecnico di Torino; *A. Chatzidimitriou, S. Tselonis, M. Kaliorakis, D. Gizopoulos,* University of Athens; *M. Riera Villanueva, R. Canal, A. Gonzalez,* UPC; *M. Kooli, A. Bosio, G. Di Natale,* LIRMM

SESSION 16
Test Generation
G. Maston, Synopsys (Chair)

16.1 Transformation of Multiple Fault Models to a Unified Model for ATPG Efficiency Enhancement
C-H. Wu, K-J. Lee, National Cheng Kung University

16.2 An Accurate Algorithm for Computing Mutation Coverage in Model Checking
H. Chao, H. Li, T. Wang, X. Li, State Key Laboratory of Computer Architecture, Institute of Computing Technology; *B. Liu,* Beijing Institute of Control Engineering

16.3 An On-Chip Self-Test Architecture with Test Patterns Recorded in Scan Chains
K-J. Lee, P-H. Tang, National Cheng Kung University; *M. Kochte,* ITI, University of Stuttgart

SPECIAL SESSION 8
Automotive IC Quality & Reliability: Today's Challenges and Solutions
H.-J. Wunderlich, University of Stuttgart (Chair)

S8.1* TBA
D. Appello, ST

S8.2* TBA
C. Eychenne, Bosch

S8.3* TBA
R. Mariani, Intel

S8.4* TBA
Y. Zorian, Synopsys

1:30 p.m. – 3:00 p.m.

SESSION 17
Mixed-Signal
W. Dobbelaere, ON Semiconductor (Chair)

17.1 Automated Measurement of Defect Tolerance in Mixed-Signal ICs
S. Sunter, Mentor Graphics; *A. Valerio, R. Miglierina,* STMicroelectronics

17.2 Automatic Test Signal Generation for Mixed-Signal Integrated Circuits Using Circuit Partitioning and Interval Analysis
A. Coyette, B. Esen, G. Gielen, KU Leuven; *W. Dobbelaere, R. Vanhooren,* ON Semiconductor

17.3 DE-LOC: Design Validation and Debugging with Limited Observation and Control, Pre- and Post-Silicon, for Mixed-Signal Systems
B. Muldrey, S. Deyati, A. Chatterjee, Georgia Institute of Technology

SESSION 18
Practices
P. Maxwell, ON Semiconductor (Chair)
P. Nigh, GLOBALFOUNDRIES (Discussant)

18.1 Pylon: Towards an Integrated Customizable Volume Diagnosis Infrastructure
Y. Pan, R. Desineni, K. Sekar, A. Chittora, S. Fernandes, N. Bawaskar, J. Carulli, GLOBALFOUNDRIES

18.2 A Reconfigurable Built-in Memory Self-Repair Architecture for Heterogeneous Cores with Embedded BIST Datapath
V. Devanathan, S. Kale, Texas Instruments

18.3 Active Reliability Monitor: Defect-level Extrinsic Reliability Monitoring
M. Johnson, B. Noble, C. Manya, J. Deforge, M. Johnson, IBM

EMBEDDED TUTORIAL 2
ISO 26262
K. Butler. Texas Instruments (Chair)

An introduction and overview of the ISO 26262 standard's scope, the functional safety lifecycle concept, the requirements for safety integrity, hardware verification, hardware metrics and system safety integration verification. Intended for engineers and managers involved in development of vehicle safety-related components and systems.

ET 2.1* Overview of the Automotive Functional Safety Standard ISO 26262 Part I—Design Impact
D. Tatman, Texas Instruments

ET 2.2* Overview of the Automotive Functional Safety Standard ISO 26262 Part II—Tools and Methods
S. Mehta, Synopsys

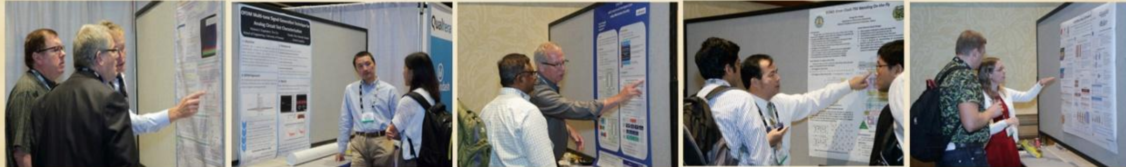
* Invited Talk

Posters

W. Eklow (Chair/Coordinator)

ITC PRESENTS

POSTERS



Wednesday, Noon to 2:00p.m.
in the
Exhibit Hall

PO 1 Double Pumped Memory Fault Modeling and Test
S. Adham, J-D. Yu, A. Lai, H. Liao, C. O'Connell, TSMC

PO 2 Tester Performance Validation (TPV): Methods and Apparatus for Validating Adherence to Published Specs in the Tester Acceptance Process
N. Magdaleno, M. Mohammed, Texas Instruments

PO 3 Does Your Locking SIB Have a Back Door?
S. Kancharla, S. Gupta, J. Kayse, J. Dworak, D. Engels, Southern Methodist University; *A. Crouch,* SiliconAid Solutions

PO 4 Custom Logic BIST in Cutting-Edge SoC FPGA Systems
R. Rajanarayanan, N. Varma, Achronix Semiconductor; *A. Cron,* Synopsys

PO 5 Testing for Connectivity to DDR Memory at Board- and System-Level ; Challenges, Guidance and Success for Boundary-Scan-based Methods
A. Ley, ASSET InterTech

PO 6 Use EDT Dynamic Bandwidth Management to Reduce SoC Patterns
K. Huang, B. Lu, T. Li, L. Xu, Spreadtrum Communications; *Y. Huang, F. Meng,* Mentor Graphics

PO 7 Fault-tolerant Photonic Router for Network-on-Chip with High Reliability
D. Dang, P. Biswas, D. Walker, R. Mahapatra, Texas A&M University

PO 8 Diagnosing Cell Internal Defects for FinFET Technology
H. Tang, W. Yang, M. Abdelwahid, D. Han, Samsung; *S. Park,* Mentor Graphics

PO 9 Exploit Faster-Than-At-Speed Functional Programs Execution for Burn-In Test
A. Bosio, G. Di Natale, LIRMM - Universit de Montpellier II / CNRS; *P. Bernardi, A. Guerriero, F. Venini,* politecnico di torino

PO 10 Note on Critical-Area-aware Test Pattern Generation and Reordering
S. Inuyama, K. Iwasaki, Tokyo Metropolitan University; *M. Arai,* Nihon University

PO 11 Silicon Debug on ATE Using Protocol-aware JTAG-IJTAG EDA Software Tools
A. Crouch, J. Johnson, SiliconAid Solutions; *N. Poulson,* Advantest

PO 12 Assessing Diagnostic Coverage by Transient Fault Injection for ISO 26262
J. Schat, NXP Semiconductors

PO 13 Uninterrupted Hardware Design
X. Qin, H. Li, Z. Wang, Huawei

PO 14 Improved Path Recovery in Pseudo Functional Path Delay Test Using Extended Value Algebra
D. Walker, P. Biswas, Texas A&M University

PO 15 ASICS End-to-End Automated Test Program Generation and Diagnostics Enablement
D. Sprague, R. Bulaga, GLOBALFOUNDRIES

PO 16 Yield Improvement by Optimizing the Impedance of Power Delivery Network (PDN) on Device Interface Board (DIB)
J. Shi, Spreadtrum Communications; *Z. Chen, Y. Huang,* Mentor Graphics; *P. Zhang,* Teradyne

PO 17 1687.1 -- New Connections for a New Standard
A. Crouch, J. Johnson, SiliconAid Solutions; *M. Keim,* Mentor Graphics

PO 18 Combining Channel Sharing and Hierarchical DFT Techniques to Address Pin-limited, Large SoC Challenges
Z. Zhang, L. Kong, K. Huang, B. Lu, Spreadtrum Communications; *R. Fisette, F. Meng,* Mentor Graphics

PO 19 A Smart Software Approach to Implement Real-Time Dynamic Part Average Testing in Production
C. Tsao, Y-T. Hsu, Sigurd Microelectronics

PO 20 CloudTesting Service In Silicon Diagnostics
A. Sivaram, O. Yasuji, Advantest; *B. Zhang, D. Mark, J. Fan,* Xilinx

PO 21 An IJTAG-compatible IDDT Embedded Instrument for Health Monitoring and Prognostics
H. Kerkhoff, A. Ibrahim, University of Twente

PO 22 ECU Testing with Adaptive Random Walks
B. Fath, KIT; *F. Gauterin,* Karlsruhe Institute of Technology

PO 23 Test Matrix Architecture to Test and On-the-Fly Failure Isolation on multiple Instance of Heterogeneous Cores
B. Konda, J. Udyavar, S. Ahmed, S. Kumar, GLOBALFOUNDRIES; *M. Lakshmanan,* Cadence Design Systems

PO 24 Scalable and Reusable Dependability Framework Based on IEEE 1687
A. Ibrahim, H. Kerkhoff, University of Twente

Panels

Monday, 4:45 p.m. – 6:30 p.m.

PANEL 1 The Unknown Unknowns in Test

R. Aitken, ARM (Moderator), *W. Eklow,* (Organizer)

This panel panel will explore the mysteries of unknowns in test. Unknowns are often why we end up solving a wrong problem, taking a wrong strategy, interpreting a result wrongly, all of which can hinder us from performing effective testing. This panel will uncover some of the unknowns and discuss what (if any) we can do to contain the risk from unknowns in test.

A social reception will be held at 6:30 p.m. following Panel 1.

Tuesday, 4:30 a.m. – 6:00 p.m.

PANEL 2 Phased Array 5G: Is Test Connected or Disconnected?

M. Slamani, GLOBALFOUNDRIES (Organizer)

The need for 1000x increase in mobile data rate led to a push for an evolution of wireless networks and a revolution in architecture to meet future demands. The current architecture needs some major changes to keep up with future data needs. Test methods and processes need to evolve to match the new 5G requirements in order to provide a high confidence to operators that the technology and services are implemented according to specification. This panel will highlight the 5G test challenges and explore possible future solutions to enable mass market production.

Panelists *P. Cain,* Keysight • *B. Floyd*, North Carolina State University • *R. McAleenan,* Advantest • *A. Roessler*, Rohde & Schwarz • *M. Roos,* Roos Instruments

PANEL 3 Test Cost Reduction—Is There More to Cut?

H. Kobayashi, Gunma University (Moderator and Organizer)

LSI testing is not just technology, but also it is a part of company management strategies. For example, some companies may use low cost ATE while others may use high-end mixed-signal ATEs as well as its associated services and know how. It also depends on applications of the DUT; for automotive application ICs, reliability and safety are very important and sufficient testing is required. The figure of merit for LSI testing may be test quality / test cost. In this panel, several possible LSI testing methods in terms of test cost reduction will be discussed.

Panelists *R.Bartlett,* Advantest • *W. Dobbelaere,* ON Semiconductor • *R.Knoth,* Cadence • *R. van Rijsinge,* NXP Semiconductors • *P. Sarson,* ams

Thursday, 1:30 p.m. – 3:00 p.m.

PANEL 4 ATE Revisited–Where Are We Today and Where Should We Be Heading?

B. Parnas, Amat (Moderator and Organizer)

Every few years industry trends drive changes in the requirements for test equipment. This panel will look at trends in the last five years and the impact on ATE as well as look into the future.

Panelists *P. Berndt,* Cypress Semiconductor • *B. Bogie,* XCerra • *H. Engelhard,* Advantest • *K. Lanier,* Teradyne

PANEL 5 Test, Validation and Security for IoTs

M. Tehranipoor, University of Florida (Moderator and Organizer)

IoTs are expected to be pervasive in home, businesses, smart communities and cities. IoT devices are now found in commonplace amenities such as cars, phones, watches, appliances, home and business security systems, thermostats, smoke detectors, as well as applications such as utilities, banking, transportation, energy, and (bio)medical industry. The number of devices introduced in the market as IoT has increased drastically, with an estimated 50 billion by 2020, most of which are expected to be fabricated off-shore. The panel discusses the challenges that come with such large scale growth.

Panelists *Y. Iskandar,* Cisco Systems • *Y. Kiki,* Optimal+ • *M. Vai,* MIT Lincoln Lab • *Y. Zorian,* Synopsys

Workshop Registration and Schedule

IEEE Computer Society Test Technology Technical Council Workshops

Thursday and Friday

General Workshop Information

Three workshops are being held in parallel immediately following ITC 2016. They will each start with an opening address on Thursday afternoon, November 17, followed by a technical session. A reception for all workshop participants will be held on Thursday evening. The remaining the technical sessions will be held on Friday, November 18. The technical scope of each workshop is described below.

Workshop Registration

All workshop participation requires registration. To register in advance for one of the workshops, do so online or by faxing the registration form. Otherwise, register onsite at regular rates at the **ITC registration counter** in the **Fort Worth Convention Center** during Test Week**.** *Admission for onsite registrants is subject to availability.* Discount workshop registration rates apply until October 16, 2016. See page 24 for details. Workshop registration includes the opening address, technical sessions, digest of papers, workshop reception, break refreshments, continental breakfast and lunch.

Digest of Papers

A digest of papers will be distributed only to attendees at the workshops as an informal proceedings.

Workshop Schedule

The three workshops will adhere to the same schedule:

Thursday, November 17		**Friday, November 18**	
Registration	2:00 p.m. – 5:00 p.m.	Registration	7:30 a.m. – 10:00 a.m.
Opening Address	4:00 p.m. – 4:30 p.m.	Technical Sessions	8:00 a.m. – 4:00 p.m.
Technical Session	4:30 p.m. – 6:30 p.m.		
Reception	7:00 p.m. – 9:00 p.m.		

Note: Workshop schedule is subject to change

Further Information

For more information on the workshops contact their organizers by e-mail or check the TTTC Web site http://ieee-tttc.org

WORKSHOP RECEPTION

Thursday, November 17
Belt Buckle Lobby of the Ft. Worth Convention Center
7:00 p.m. – 9:00 p.m.

Workshop Summaries

▪ ART: 1st IEEE International Workshop on Automotive Reliability and Test

Scope: The ART workshop focuses exclusively on test and reliability of automotive and mission-critical electronics, including design, manufacturing, burn-in, system-level integration and in-field test, diagnosis and repair solutions, as well as architectures and methods for reliable and safe operations under different environmental conditions. With increasing system complexity, security, stringent runtime requirements for functional safety and cost constraints of a mass market the reliable operation of electronics in safety-critical domains is still a major challenge. The ART workshop offers a forum to present and discuss these challenges and emerging solutions among researchers and practitioners alike. The scope of the workshop includes, but not limited to:

Functional Safety in automotive domain
Validation of automotive systems
Aging effects on automotive electronics
Automotive standards and certification
Power-up and periodic self-test
High-quality test and DPPM minimization

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▪ DATA: IEEE Workshop on Defects, Adaptive Test, Yield and Data Analysis

Scope: The scope of the DATA workshop once again returns to our common theme, which has always been DATA, specifically, semiconductor test and yield data. We in the semiconductor industry create billions of data points every hour, and we've made great strides in capturing, storing, and analyzing these data. As the cost of storage falls, and query and analysis capabilities become ever more powerful, the next horizon for DATA professionals is real-time understanding. How quickly can we turn our copious data from wafer sort, final test, in-line defect inspection, etc., into an understanding that leads to immediate or even pre-emptive action? The time and cost pressures we're facing as an industry make the move towards short-loop process improvement an imperative. Suggested topics include:

Data storage and security
Analog fault modeling and coverage
Test data analysis
Adaptive test for product engineers
Data mining methods for test data processing
High/low-voltage and stress testing
Yield learning and analysis
I/O test, tuning, and adjustment
Defect coverage and metrics
Product and project case studies
Advanced DPPM reduction technique
Fault localization and diagnosis

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Program Chair: Arani Sinha, *Arani.Sinha@intel.com*

ITC Receptions

Monday 6:30 p.m. – 7:30 p.m.

ITC Happy Hour

(Following Panel 1)

Monday, November 14, 6:30 p.m. – 7:30 p.m.

Enjoy a networking gathering following the panel, with beer/wine and appetizers.

Tuesday 6:30 p.m. – 8:30 p.m.

ITC Welcome Reception

Tuesday, November 15, 6:30 p.m. – 8:30 p.m.
Ashton Depot

Join with colleagues and friends for an evening of fine food and libations at Fort Worth's grand and historic Ashton Depot. Opened in 1899, and originally named the Santa Fe Depot, the Beaux Arts-style terminal will welcome you with Texas-style hospitality. "Wranglers" will help guide you to the Aston Depot, a short two blocks from the Fort Worth Convention Center.

Categories & Fees

Register Online or Contact the ITC Office for a Registration Form

All Test Week activities require a registration badge for admittance. Register in advance online. Otherwise, register on-site at regular rates during Test Week at the **ITC registration counter** at the **Fort Worth Convention Center.** See page 25 for registration hours. To obtain a **substantial discount** register no later than October 16, 2016.

▶**ITC Full-Conference Registration** Includes ITC technical paper and panel sessions, exhibits, ITC welcome reception, lunch in the exhibit hall, break refreshments, download ITC 2016 Proceedings and Technical Presentations, ITC bag and shirt. Registration does not include the tutorials on Sunday and Monday or the workshops on Thursday and Friday. You may purchase additional download ITC 2016 Proceedings at $25 each.

▶**ITC One-Day Registration (Onsite-only)** Includes ITC technical program activities, exhibits, lunch in the exhibit hall and break refreshments—all for the day of registration only. Also includes ITC 2016 Proceedings and Technical Presentations, ITC bag and shirt. Registration does not include ITC welcome receptions. You may purchase: additional download ITC 2016 Proceedings at $25 each

▶**ITC Free Exhibits-only Registration (Onsite or Online)** Includes admission to exhibits on Tuesday, Wednesday and Thursday and corporate presentations on Tuesday. Lunch and receptions not included.

▶**Student Rates** IEEE student members must also present their current IEEE Student Member card at the ITC registration counter. Student nonmembers must present their current school student ID.

▶**Tutorial Registration** Tutorials are a half-day in length.
One-Day tutorial registration fee is for two tutorials—a morning tutorial and afternoon tutorial, both on the same day, e.g., Tutorial 1 and Tutorial 4 on Sunday. You may register for up to four tutorials (two consecutive on Sunday and two consecutive on Monday).
All-Access Pass tutorial registration provides in-and-out access to all twelve tutorials over both days.

All registrations include study material, breaks and lunches on the day(s) attended. Tutorial registration does not include the ITC technical program, ITC receptions, exhibits, exhibit hall lunches, ITC publications, ITC tote, shirt or the workshops on Thursday and Friday.

▶**Workshop Registration** Includes the items specified on page 21. Registration does not include the ITC technical program, exhibits, ITC receptions, exhibits, exhibit hall lunches, publications, ITC bag, shirt or the tutorials on Sunday and Monday.

▶**Discount Rates** Early registration rates apply only when you complete your registration by October 16, 2016, either online or with a paper form and payment postmarked or faxed by October 16, 2016. To receive IEEE/Computer Society member or student member reduced rates, you must include your member number, which will be verified.

Registration Fees

Discount Rates*	Full Conference	1-Day-only Conference†	One Day 2 Tutorials	All-Access Tutorial Pass	One Workshop
IEEE/CS Member	$725	n.a.	$225	$550	$240
Nonmember	$940	n.a.	$282	$664	$300
IEEE/CS Student Member	$200	n.a.	$225	$550	$130
Nonmember Student	$250	n.a.	$225	$550	$240

Onsite Rates	Full Conference	1-Day-only Conference†	One Day 2 Tutorials	All-Access Tutorial Pass	One Workshop
IEEE/CS Member	$940	$320	$282	$664	$300
Nonmember	$1170	$400	$428	$976	$375
IEEE/CS Student Member	$200	n.a.	$282	$664	$160
Nonmember Student	$250	n.a.	$282	$664	$300

*not available after October 16, 2016, †Online registration not available.

Refunds

All refund/cancellation requests must be provided in writing and received by October 31, 2016. No refunds will be issued after October 31, 2016. Please submit all refund/cancellation requests to: ITC2016@badgeguys.com. There will be a cancellation fee of $75 and will be deducted from each refund..

Registration Hours

Registration for All Activities

ITC registration counters at the Fort Worth Convention Center

Sunday, November 13 to Thursday, November 17
7:30 a.m. – 5:00 p.m.

Need More Registration Information?

Contact the ITC office
2025 M Street, NW, Suite 800, Washington, DC 20036, USA
Tel. +1 202.973.8665   Fax. +1 202.973.8716

Fringe Technical Meetings

ITC arranges for meeting space for appropriate IEEE- or Computer Society TTTC-sponsored groups wishing to hold their meetings during Test Week, November 13 – 18. Contact the ITC office.

ITC 2016 Proceedings Distribution

ITC proceedings will be delivered electronically.

All ITC full-conference and one-day attendees, including students, will receive access to the ITC online proceedings free of charge.

Preregistered Full-Conference Attendees

All preregistered full-conference attendees will receive an email containing a download link a few days before the conference when the proceedings become available.

Onsite Full-Conference and One-Day Attendees

Full-conference and one-day attendees registering onsite will receive the download link at the time of registration.

Ordering Additional Proceedings with Advance Registration

All preregistered full-conference attendees may also order additional download 2016 proceedings, beyond the free copy, at $25 each.

Purchasing Additional Proceedings at the Conference

Full-conference and one-day attendees may also purchase onsite additional downloads of the 2016 proceedings for $25 each.

ITC 2016 Technical Paper Presentations

Available free for download along with proceedings.

The ITC Program Committee has compiled the slides used for this year's technical paper presentations—including invited presentations—and has them available for download*. You can review sessions that you attended and cover those that you could not attend. This will only be available as a free download to registered full- and one-day conference attendees, including students—one per person. Preregistered attendees will receive a download link a few days before the conference. Others will receive the link when they register onsite.

The paper presentation slides make the perfect complement to the full manuscripts in the proceedings, as they contain the latest data .

*Some authors have chosen not to participate. These omitted papers will be identified. Slides used in panel sessions and the corporate forum are not included.

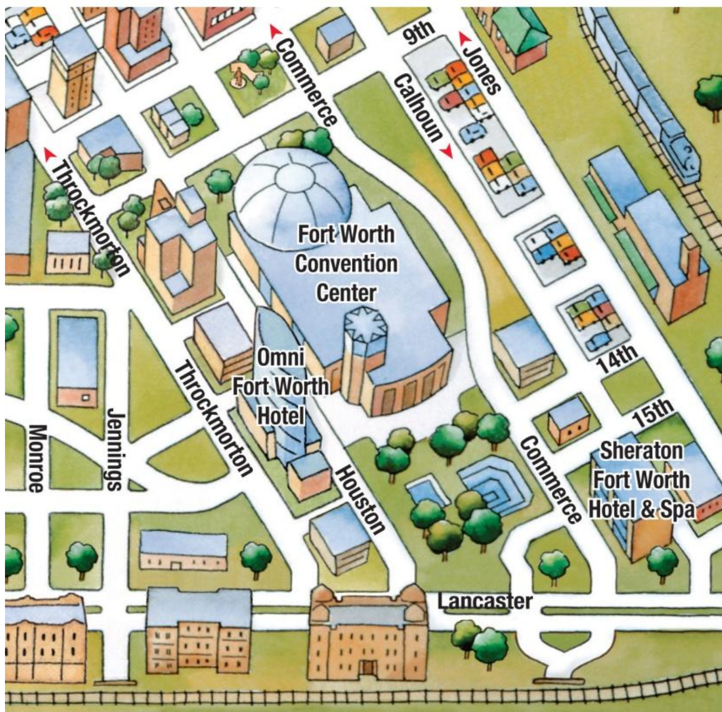
Hotel Reservations

Online Hotel Reservations

Reserve a Fort Worth room online from our **only** official housing vendor by clicking the button above.

- Rooms may be reserved for the period from **October 11, 2016 to October 20, 2016.** The ITC rate is also available three days earlier and later, subject to availability.
- Cancellations: **Omni** - by12:00 p.m. local time on day before arrival; **Sheraton** - by 4:00 p.m. local time on day before arrival.
- The reservation cutoff date is **October 11, 2016 at 5:00 p.m. local time.** Reservations made after that date will be made at the ITC rate on a space-available basis. Contact jay@connectionshousing.com
- *Parking for hotel guests: **Omni,** valet parking $25 per night, self-parking adjacent at $19 per night; **Sheraton**, $20 per night.
- Both hotels offer free internet in guest rooms.
- If you need assistance to reserve 1-9 rooms, contact **Connections Housing** at 404-842-0000 or 800-262-9974 and a call-center agent will assist. For 10 or more rooms, email jay@connectionshousing.com or call 404-918-9129.

* Prices subject to change without notice, plus tax



Omni Fort Worth Hotel
1300 Houston Street
Fort Worth, TX 76102
Phone: 817.535.6664

USD 180.00 Average nightly rate +15% tax

Sheraton Fort Worth Downtown Hotel
1701 Commerce Street
Fort Worth, TX 76102
Phone: 817.335.7000

USD 169.00 Average nightly rate +15% tax

Message to Attendees: ITC has made every effort to secure the best possible group nightly room rate for you at this event. That rate results from a negotiated overall package of event needs such as sleeping rooms, meeting room space and other requirements. Contracts with the venue include a provision to reduce event costs if ITC meets or exceeds its minimum sleeping room block guarantee. Conversely, event costs will increase if ITC falls short of its minimum room block guarantee. Please help ITC keep the costs of this event as low as possible by booking your housing needs at the designated host hotel and through the reservation process created by ITC. Reserving elsewhere means you are booking outside the contracted room block, jeopardizing ITC's ability to meet its contracted obligations and to keep registration fees to a minimum. ITC appreciates your support and understanding of this important issue. Thank you.

Location & Travel

Location

The ITC conference and all associated Test Week events will be held at the Fort Worth Convention Center in downtown Fort Worth, Texas. The two host hotels are only a short walk to the convention center.

Recently named the best downtown in the nation, (according to livability.com) Fort Worth's city center buzzes day and night with people, energy and opportunity. It's one of the cleanest, safest and most walkable urban areas you'll find anywhere – the perfect place to soak up the excitement and friendly ambience of Fort Worth. The heart of downtown is Sundance Square, a 35-block shopping and entertainment district where charming, beautifully restored buildings stand alongside glittering skyscrapers. Here, you'll find locals, downtown residents and visitors among a multitude of restaurants, shops, galleries and performance venues. Sundance square is easily reached via the free Molly the Trolley bus.

Nearby is the Stockyards National Historic District. Once home to cowboys, cattlemen and outlaws, today it is one of the most popular attractions in Texas. Day and night, visitors come to the Stockyards to get a taste of the true American West. The weathered brick streets are lined with historic buildings, restaurants, shops, saloons and other attractions.

Travel

Air
Fort Worth is serviced by the Dallas/Fort Worth International Airport (DFW) which is about 25 miles by road miles from the Fort Worth Convention Center. There are several transportation options from the airport to downtown Fort Worth.

Trinity Railway Express (TRE) Commuter Rail
Travel between the CentrePort/DFW Airport Station and the Fort Worth Intermodal Transportation Center (ITC) is $2.50. **There is no Sunday service.** The DFW station is reached by a shuttle bus that leaves from the terminal areas. The ITC is one-half mile from the convention center. There is the free Molly the Trolley bus service between the ITC and the host hotels.

SuperShuttle
We have established a discount with Super Shuttle and ExecuCar for airport transfers during ITC. The link below will take you to the site where reservations can be made. International Test Conference Discount Link. The fare is approximately $17 by shuttle bus.

You will only receive the discounted fare if you book through our link and use code **WPEH6**
Calls to the reservation desk are charged a $2.00 booking fee.

Taxi
Taxi service from DFWis available for a flat rate of approximately $50.

Car
Driving directions to the Omni Hotel, which is across the street from the convention center.

Information

1. The ITC Advance Program release 2.1 was generated with Adobe Acrobat 8.2.6 on 3-October-2016

2. The program will be updated periodically as new material is available—check back often.

3. Navigate using the tabs and links at the top of each page.

4. Use underlined links in the At-a-Glance to find specific items.

5. For more information contact:

Subject	Contact	Email
Advance Program	Don Denburg Scott Davidson	denburg@rcn.com davidson.scott687@gmail.com
Corporate Forum	Art Downey	artdowney@cruzio.com
Exhibits and Exhibiting	Bill Lowd	bzintrnatl@aol.com
Fringe Technical Meetings	Courtesy Associates	itc@courtesyassoc.com
Hotels	Connections Housing	jay@connectionshousing.com
Posters	Bill Eklow	beklow56@gmail.com
Registration	Courtesy Associates	itc@courtesyassoc.com
Technical Program	Li-C. Wang	licwang@ece.ucsb.edu
TTTC Tutorials	Yervant Zorian	zorian@synopsys.com
TTTC Workshops	Yervant Zorian	zorian@synopsys.com
All Other Questions	Courtesy Associates	itc@courtesyassoc.com

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