

Study on ON-Resistance Degradation Modeling Used for HCI Induced Degradation Characteristic of LDMOS Transistors

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Abstract

This paper reports an on-resistance degradation model induced by hot current injection (HCI) based on the maximum electric field of n-channel laterally diffused MOSFET (LDMOS) transistors for reliability simulations. LDMOS transistors operate under high-voltage and large-current biases, where the electric field increases with biases at the gate edge. Also, DC bias, temperature, and time stress dependencies on on-resistance degradations are formulated by empirical equations. We present investigations, derivations, and verifications of our on-resistance degradation model with measurements and T-CAD simulations.

1. Introduction

Laterally Diffused MOSFETs (LDMOS's) are widely used in RF applications where high voltages and large current are supplied. For fast and low dissipation power switching applications, on-resistance (R_D) of an LDMOS should be low enough in the high voltage region. To reduce the amount of R_D , the drift doping concentration needs to be increased as possible. The heavy doping concentration leads to high lateral electric fields in the device at the gate edge. Since the lateral high electric field degrades the drain channel of the device, an important degradation issue to be considered is the time and temperature degradations of an LDMOS by the hot carrier injection (HCI) effect. It is extremely convenient to predict the amount of HCI in an LDMOS before producing the device for reliability simulations.

The HCI degradation of n-channel LDMOS causes an increase R_D by decreasing carrier in the drift region by lateral maximum electric field of the gate edge [1]. However, the maximum electric field and the on-resistance degradation have been modeled with table-lookup functions in [2] which are not flexible to apply for any process devices. We, therefore, develop the models with empirical equations.

In this paper, we present maximum electric field and hot electron life time function models to represent the on-resistance degradation. Then the model has been verified with measured data and T-CAD simulations. Results show good agreement among these data.

2. Maximum electric field model

Since the HCI stress is dominated by the maximum electric field, E_m , which is correlated with the on-resistance

degradation [3]. To solve E_m , the accurate method is to derive 2D Poisson equation. However, many boundary conditions are needed and then, results include many unknown parameters to be extracted with experiments. We, therefore, apply asymmetric single peak distribution function to decrease the number of parameters without sacrificing model accuracies. The E_m equations are;

$$E_m(V_{DS}, V_{GS}) = Ae^{(-e^{-z}-z+1)}, \quad (1)$$

$$A = \alpha \frac{(V_{DS}-V_{DSAT})}{L_{eff}}, \quad (2)$$

$$z = \frac{V_{GS}-V_{TH}-V_{GS,max}}{\beta k_B T}, \quad (3)$$

where, α and β are the device specific empirical parameters. V_{DS} is the drain-to-source voltage, V_{GS} is the gate-to-source voltage, and V_{TH} is the threshold voltage, respectively. V_{DSAT} is the potential at the pinch-off or the saturation point in the channel. Physical constants L_{eff} , k_B and T are the effective channel length, the Boltzmann constant, and device temperature, respectively. A represents the amplitude of peak value of electric field. Because the magnitude of lateral electric fields and the peak point, z , depend on V_{DS} and V_{GS} [1], the proposed model equations are flexible enough to change the peak value and the location. Fig.1 shows the comparison between the T-CAD simulation results [1] and the proposed function model for maximum electric field of an n-channel LDMOS.

3. On-resistance model

The HCI degradation of n-channel LDMOS causes an increase on-resistance by decreasing carrier in the drift region. The model equation of deteriorated R_D ($R_{D,deg}$) based on fresh R_D ($R_{D,fresh}$) is written based on [1] as;

$$R_{D,deg} = R_{D,fresh} \left\{ 1 + A_1 \cdot \ln\left(1 + \frac{t}{\tau}\right) + A_2 \cdot \ln\left(1 + \frac{t}{\gamma \cdot \tau}\right) \right\}, \quad (4)$$

where, A_1 , A_2 , and γ are device specific parameters, and t is the stress time. When the Si-H excitation (m) occurred to derive carrier life time, τ , conventional model [1] was poorly accurate in our investigation. We, therefore, have modified the τ equation as;

$$\tau = \left(\frac{\alpha W}{I_D}\right)^m \cdot \frac{\phi_b}{E_m \lambda} e^{\frac{\phi_b}{E_m \lambda}}, \quad (5)$$

where, α is the device specific empirical parameter. W is the gate channel width. λ is the mean free path that carriers can travel in this electric field before going through an energy losing scattering event. ϕ_b is the energy needed for

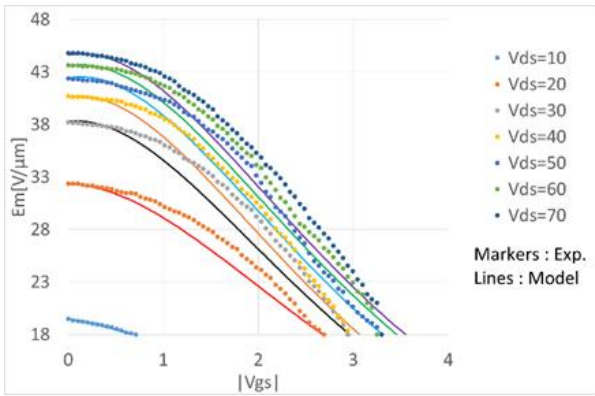


Fig. 1 Comparison between T-CAD simulations [1] and the proposed function model for the maximum electric field of n-channel LDMOS's

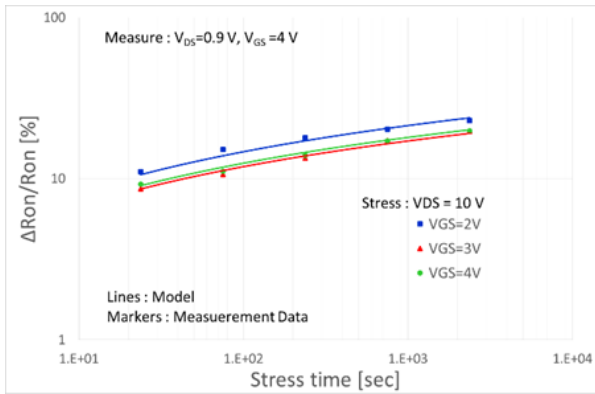


Fig. 2 Comparison between bias stress measurements and calculations of the proposed model.

electrons to surmount the Si-SiO₂ energy barrier.

4. Tests and verifications of the proposed model

We have measured R_D degradation and I-V characteristics as followed by [2]. To simulate I-V characteristics on SPICE, RD_{deg} of the proposed R_D degradation model in Eq. (4) is applied for the model parameter RD in HiSIM-HV model [5]. Fig. 2 shows the comparison between the proposed model calculations and measured R_D of bias dependencies. The proposed model agrees to the measured data with reasonable accuracies. Fig. 3 shows the DC characteristics of an LDMOS that before and after hot-carrier induced degradation. The stress simulation agrees with measured data in Fig.3. Although the stress simulation does not agree with measured data in Fig. 4, it is successfully reproduced that the drain current in the saturation region does not change whereas the drain current in the pinch-off region decreases.

5. Conclusions

In this paper, we have presented the derivation of on-resistance degradation model, and maximum electric field model to analyze hot carrier injection degradations. Furthermore, we have verified our models with DC drain current simulations using HiSIM-HV model compared with

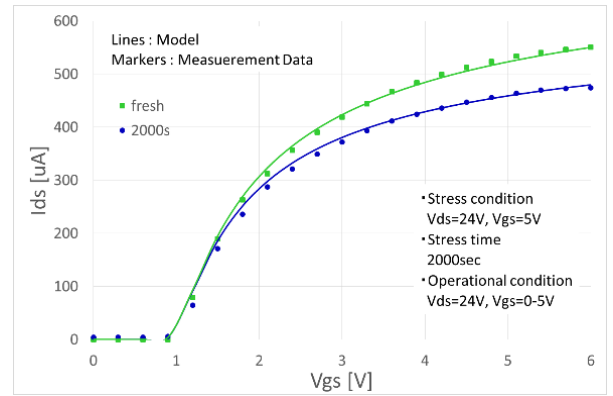


Fig. 3 I_{ds} - V_{gs} characteristics of an n-type LDMOS before and after hot-carrier induced degradations.

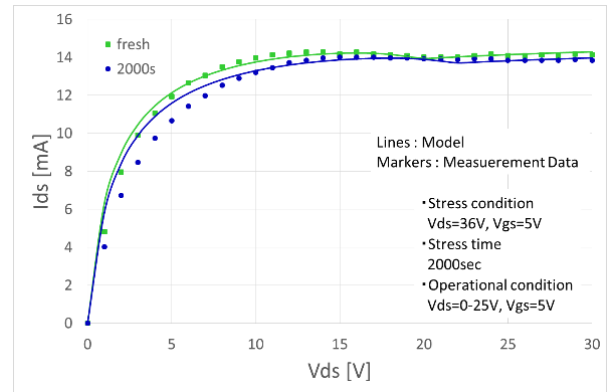


Fig. 4 I_{ds} - V_{ds} characteristics of an n-type LDMOS before and after hot-carrier induced degradations.

device measurements. We are going to enhance our models to support dynamic characteristics.

Acknowledgements

We would like to thank MoDeCH Inc. for their valuable support on this project.

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