Simple Reference Current Source Insensitive to Power Supply Voltage Variation - Improved Minoru Nagata Current Source

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Abstract - This paper describes design improvement of the constant current source (peaking current mirror), originally invented by Nagata Minoru in 1966. Our improved current mirror circuits with MOS and Bipolar are insensitive to wide range of power supply voltage variation; they are realized by addition of multiple current peaks. We show their circuit topologies, operations and simulation results. The proposed reference current circuits are simple, small yet well-insensitive to power supply voltage variations, and hence they can be widely used in analog ICs.

Keywords: Reference current source, Nagata current mirror, Peaking current mirror, Supply voltage variation

I. Introduction

In many analog IC applications, one reference current/voltage source is required; the other current sources can be generated from the reference current/voltage. The reference current/voltage source should be stable against the change of the environment in analog IC.

Representative example of the reference voltage source is a bandgap reference circuit. This circuit provides a stable voltage against temperature and supply voltage variations, but its design is complicated and it occupies relatively large chip area.

Another example is a peaking current mirror invented by Minoru Nagata in 1966 [1,2]; hereafter we call this circuit as Nagata current mirror. Its output current has a peak with respect to the input current change. When it is biased at the vicinity of the peak, its output current change with respect to the input current change is slight. When the input current is realized by a resistor whose one terminal is connected to a power supply voltage (V_{DD}), a constant output current is obtained over the supply voltage fluctuation. Even though this circuit does not take care of temperature variation, it is widely used such as in DC-DC converter ICs due to its simplicity.

In this paper, we propose an improved Nagata current mirror which provides constant current over much wider range of the power supply voltage fluctuation than the original Nagata current mirror, using multiple current mirror circuits with different current peaks. Its MOS and Bipolar circuit configuration, analysis and simulation results are described.

II. Nagata Current Mirror Circuit

Fig. 1 shows the original Minoru Nagata current mirror circuit, and its output current (I_{OUT}) with respect to the input current (I_{IN}) has a peak as shown in Fig. 2. When the input current (I_{IN}) increases from a small value, the output current (I_{OUT}) follows and increases. For further input current increase, a voltage drop (RI_{IN}) between nodes *a* and *b* is caused: then the gate-source voltage of M_2 becomes smaller than that of M_1, and the drain current of M_2 decreases.

We see from Fig. 2 that the output current has a peak, and the input current source can be realized with a resistor whose one terminal is connected to the power supply. Then at the vicinity of the peak, the output current is almost constant with respect to the power supply change, but the peak vicinity is narrow. In the following sections, we will describe its improved circuit whose output current is constant over the wide range of the input current.

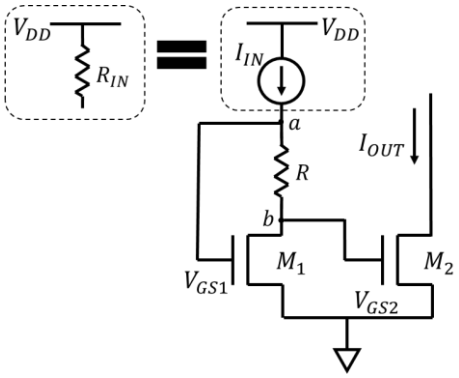

Fig. 1. Nagata current mirror

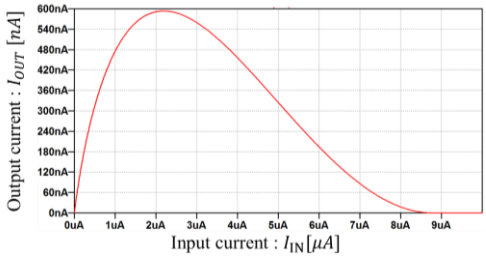

Fig. 2. I_{IN} - I_{OUT} characteristics of Nagata current mirror (SPICE simulation result)

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III. Proposed MOS Reference Current Source

3.1 Proposed Circuit Configuration and Operation

Fig. 3 shows the proposed reference current source, which is an improved MOS Nagata current mirror. It uses multiples of Nagata current mirror circuits with different peaks, and its output current is their total current. As a result, the output current is constant over the wide range of the power supply voltage (or input current) as shown in Fig. 4.

Now we will explain the operation principle of the circuit in Fig. 3. It follows from Kirchhoff Voltage Law (KVL) that

$$V_{GSn} = V_{GS1} - R^{total}{}_{n-1} I_{IN} \qquad (1)$$

$$(n = 2,3,4,5) \quad (R^{total}{}_{n-1} = R_1 + R_2 + \ldots + R_{n-1}).$$

Currents (I_{IN} , I_{OUTn}) flowing into M1 – M5 can be expressed by eqs. (2), (3), using the MOSFET current formula in the saturation region.

$$I_{IN} = K_1 (V_{GS1} - V_{TH})^2 (1 + \lambda V_{DS1}) \qquad (2)$$

$$I_{OUTn} = K_n (V_{GSn} - V_{TH})^2 (1 + \lambda V_{DSn}) \qquad (3)$$

$$\text{where} \quad K_n = \frac{1}{2} \mu C_{ox} \left(\frac{W}{L} \right)_n$$

V_{GS1} and V_{GSn} can be obtained from eqs. (2), (3).

$$V_{GS1} = \sqrt{\frac{I_{IN}}{K_1 (1 + \lambda V_{DS1})}} + V_{TH} \qquad (4)$$

$$V_{GSn} = \sqrt{\frac{I_{OUTn}}{K_n (1 + \lambda V_{DSn})}} + V_{TH} \qquad (5)$$

Eqs. (1) and (2) are substituted into (3), and the output current I_{OUTn} is obtained as:

$$I_{OUTn} = K_n (V_{GS1} - R^{total}{}_{n-1} I_{IN} - V_{TH})^2 (1 + \lambda V_{DSn})$$

$$= K_n I_{IN} R^{total}{}_{n-1}{}^2 \times$$

$$\left(\sqrt{I_{IN}} - \frac{1}{R^{total}{}_{n-1} \sqrt{K_1 (1 + \lambda V_{DS1})}} \right)^2 (1 + \lambda V_{DSn}) \qquad (6)$$

We will find the extreme value of input-output characteristics of the circuit in Fig. 3. Differentiate I_{outn} in eq. (6) with respect to I_{IN} and then we have:

$$\frac{dI_{OUTn}}{dI_{IN}} = K_n R^{total}{}_{n-1}{}^2 (1 + \lambda V_{DSn}) \left(\sqrt{I_{IN}} - \frac{1}{R^{total}{}_{n-1} \sqrt{K_1 (1 + \lambda V_{DS1})}} \right)$$

$$\times \left(2\sqrt{I_{IN}} - \frac{1}{R^{total}{}_{n-1} \sqrt{K_1 (1 + \lambda V_{DS1})}} \right) \qquad (7)$$

For $\frac{dI_{OUTn}}{dI_{IN}} = 0$, we have the following:

$$I_{IN} = \frac{1}{4 R^{total}{}_{n-1}{}^2 K_1 (1 + \lambda V_{DS1})} \qquad (8)$$

Eq. (8) is substituted into (6), and the peak output current is given by

$$I_{OUTn} = \frac{(W/L)_n}{4(W/L)_1} \bullet \frac{1}{4 R^{total}{}_{n-1}{}^2 K_1} \bullet \frac{(1 + \lambda V_{DSn})}{(1 + \lambda V_{DS1})} \qquad (9)$$

We see from eqs. (8), (9) that the input current value at which the output current has the peak, and the amount of the peak output current can be changed by changing resistor values and MOSFET sizes. Fig. 4 shows SPICE simulated characteristics of the proposed reference current source circuit in Fig. 3, where TSMC 0.18μm parameters are used. We see that the total output current (I_{OUT_total}) is almost constant over wide range of the input current I_{IN}.

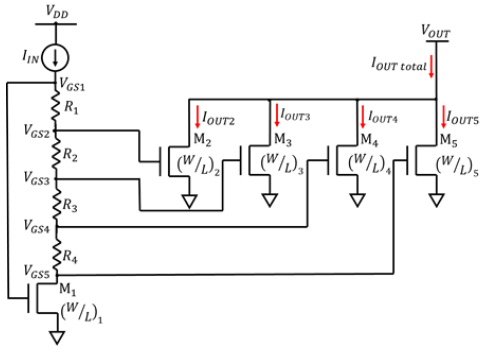

Fig. 3. Proposed MOS reference current source.

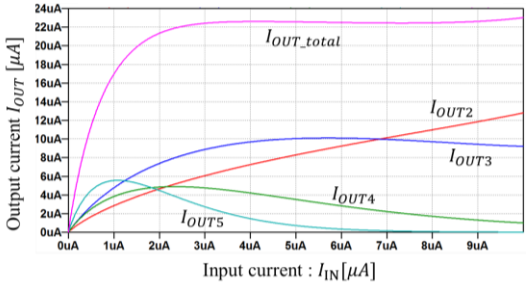

Fig. 4. I_{IN} - I_{OUTn} characteristics of the proposed MOS refence current source.

Note that our simulation circuit has used 4 peaks, however, the number of peaks is not restricted to 4.

3.2 Influence of Resistor Values and MOS Characteristics Variation

In order to investigate the effect of the resistor value variation to the output current, we have performed SICE simulation: all resistance values are uniformly shifted by ±10%. In addition, MOS fast and slow models are used. We see from Figs. 5, 6 that when MOS models and resistor values are varied, the total output current keeps constant, but its magnitude is varied.

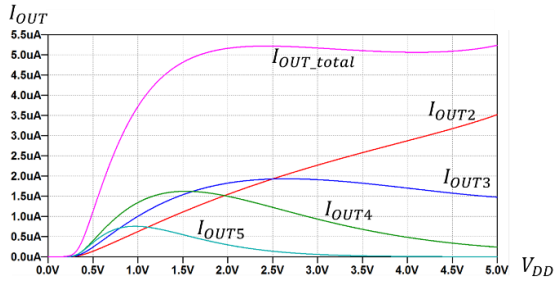

Fig. 5. Simulation results of the proposed circuit in Fig. 3 in case that all resistor values decrease by 10%.

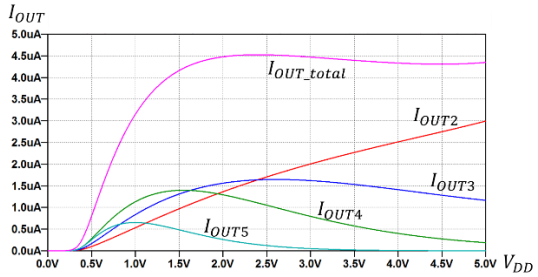

Fig. 6. Simulation results with SLOW NMOS model, of the proposed circuit in Fig. 4.

IV. Proposed Bipolar Reference Current Source

Fig. 7 shows the proposed Bipolar reference current source using multiple Nagata current sources with different peaks. Fig. 8 shows its SPICE simulation result and we see that its output current is constant over the wide range of the supply voltage variation.

Now we will analyze the circuit in Fig. 7. Using KVL, we have the following:

$$V_{BEn} = V_{BE1} - R^{total}{}_{n-1} I_{IN} \qquad (10)$$

$(n = 2,3,4,5)$ $(R^{total}{}_{n-1} = R_1 + R_2 + \ldots R_{n-1})$.

Note that

$$V_{BE1} = V_T \ln\left(\frac{I_{IN}}{I_{s1}}\right) \qquad (11)$$

$$V_{BEn} = V_T \ln\left(\frac{I_{OUTn}}{I_{sn}}\right) \qquad (12)$$

Here a thermal voltage $V_T = kT/q$.

It follows from eqs. (10), (11) and (12) that

$$V_T \ln\left(\frac{I_{IN}}{I_{s1}}\right) - V_T \ln\left(\frac{I_{OUTn}}{I_{sn}}\right) = R^{total}{}_{n-1} I_{IN} \qquad (13)$$

Suppose that all saturation currents (I*sk*, k=1, 2, .. 5) are the same. Then the output current (I_{OUTn}) of each Bipolar transistor is given by

$$I_{OUTn} = I_{IN} \exp\left(-\frac{I_{IN} R^{total}{}_{n-1}}{V_T}\right) \qquad (14)$$

Now differentiate I_{OUTn} with respect to I_{IN}:

$$\frac{dI_{OUTn}}{dI_{IN}} = \exp\left(-\frac{I_{IN} R^{total}{}_{n-1}}{V_T}\right)\left(1 - \frac{R^{total}{}_{n-1}}{V_T}\right) \qquad (15)$$

Then we have the following for $\frac{dI_{OUTn}}{dI_{IN}} = 0$.

$$I_{IN} = \frac{V_T}{R^{total}{}_{n-1}} \qquad (16)$$

Then we have the peak output current:

$$I_{OUTn} = \frac{V_T}{R^{total}{}_{n-1}} \cdot \frac{1}{e} \qquad (17)$$

We see from eqs. (16), (17) that the input current value for the peak output current, and the peak output current value can be changed by the resistor values.

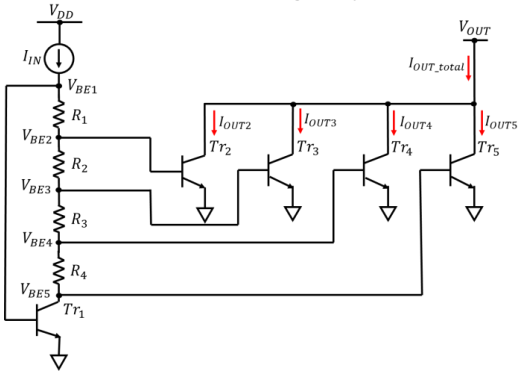

Fig. 7. Proposed Bipolar reference current source.

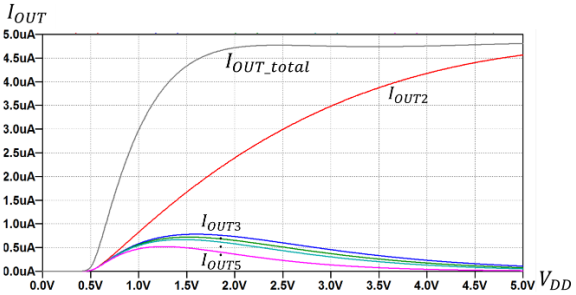

Fig. 8. Simulation results of the circuit in Fig. 7.

V. Conclusion

We have described simple MOS and Bipolar constant current sources, insensitive to wide range of power supply voltage variation; they are realized by addition of multiple current peaks. Their circuit topologies, analyses, and SPICE simulation results are presented.

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