Study of Gray Code Input DAC Using MOSFETs for Glitch Reduction

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Abstract - This paper deals with a technique to reduce glitches in digital-to-analog converters (DACs) using Gray code input. These DACs are designed using MOSFETs, and their operation with glitch reduction was confirmed with SPICE simulation. It has been believed that good topologies of Gray code input DACs do not exist, but we show here their paradox. We also show with simulation that our Gray code input DACs can reduce glitches.

Keywords - Glitch, DAC, Gray code, Binary code, Gray code input DAC, Voltage mode DAC, Current-steering mode DAC

I. Introduction

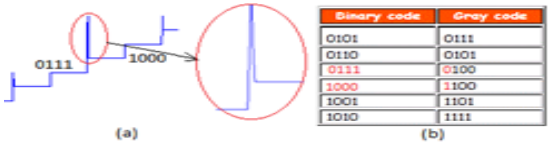
A digital-to-analog converter (DAC) converts digital signals to analog signals (at voltage levels, current levels or electric charge) with various circuit topologies; such as interpolating, binary weighted, R-2R ladder, successive-approximation, thermometer-coded, and hybrid type topologies [1, 2]. The R-2R ladder-type DAC is widely used because of its design simplicity. However it is prone to produce large glitches (output voltage spikes) which cause serious deterioration in the analog output signal such as in Graphic display applications.

Although the DAC is usually followed by a reconstruction analog filter, it comes with a disadvantage of taking chip area in an IC, and/or it requires more components and hence increases the cost. So, techniques to reduce glitches should be implemented especially for the high-speed DAC.

One candidate as glitch reduction technique is using Gray code [3, 4, 5] input DAC which uses only one switch transition at one time for 1-LSB change. However, it has been considered that Gray code input DAC is difficult to realize efficiently and systematically [3, 4]. Here we take challenge to develop some topologies for the Gray code input DAC, using the characteristics that binary and Gray codes can be converted each other using exclusive OR.

II. Glitch in DAC Output

The glitches in the DAC are caused mainly due to differences in how fast switches open and close as well as capacitive coupling. Typically the glitch behavior is dominated by the differences between the switching speeds. The switching of the MSB causes most significant glitches[2] as shown in Fig 1. For example, binary code transition of 0111 to 1000 or 1000 to 0111 causes major glitches in the DAC. Note that large glitch is caused when there are some switches changing their states from ON to OFF and other switches from OFF to ON at once.



Binary code	Gray code
0101	0111
0110	0101
0111	0100
1000	1100
1001	1101
1010	1111

Fig 1 (a): Glitch due to MSB change in a binary DAC
(b) Comparison of switching of binary and Gray codes.

III. Gray Code Input DAC

We study here the following two DAC architectures in comparison with binary input R-2R DACs.

A. Voltage-mode Gray code input DAC
B. Current-steering Gray code input DAC

The Gray code input DAC architecture involves current/voltage switch matrix design as a main component to distinguish between the binary and Gray code input DACs. The current/voltage switch matrix is a double pole double throw (DPDT) switch which has two inputs (IN1 and IN2), two outputs (OUT1, OUT2) and a switch control (CTL) (Fig. 3 (a), (b)). The switch connects IN1 to OUT1 and IN2 to OUT2 when CTL is logic LOW, while it connects IN1 to OUT2 and IN2 to OUT1 when CTL signal is logic HIGH. Gray code input is provided to the CTLs. Fig. 3 (c) shows MOSFET implementation of the current/voltage switch matrix.

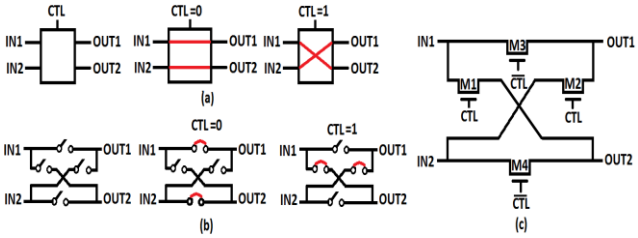


Fig. 3: (a) Current/voltage switch matrix. (b) Switch level design. (c) MOSFET level design.

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A. Voltage-mode Gray code Input DAC

The voltage-mode Gray code input DAC is designed as shown in Fig. 4. The first input terminal IN1 is supplied with a reference voltage and the second input terminal IN2 is connected to the ground. The terminal X0 is connected to the R-2R network, and the other parts are completed as shown. The end terminals are terminated by a combination of 1.5R and 0.5R resistors [3]. The output voltage is taken from the voltage follower configuration, which is given by

$$Vout(D) = \frac{Vref}{2^{n+1}}|(2D-1)| \quad (1)$$

Here n is the total number of bits (or resolution).

D=1, 2, 3….n+1

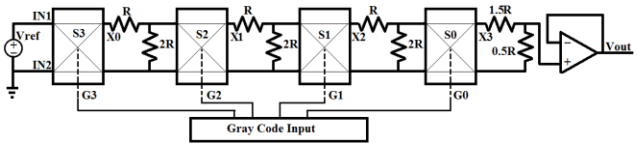


Fig. 4: Voltage-mode Gray code input DAC.

MOSFET implementation [6] of the voltage-mode Gray code input DAC is simply the change of resistors to MOSFETs (Fig 5). The value of R for each MOSFET is calculated by

$$R = \frac{V_{DS}}{\frac{u_n C_{ox}}{2}\times\left(\frac{W}{L}\right)\times[(V_{GS}-V_{TH})^2]} \quad (2)$$

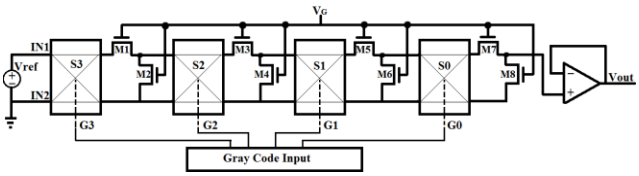


Fig 5: MOSFET level design of volage-mode Gray code input DAC.

B. Current Steering Mode Gray code Input DAC

Fig. 6 shows our current-steering mode Gray code input DAC. The circuit comprises of binary weighted current sources at the terminals IN1, IN2 and the internal nodes. Gray code input only alters the way how switches are triggered, and the current sources are switched accordingly. The output is taken as Iout which is the difference between Iout+ and Iout-. For example, let us consider the case that binary code 1100 is to be converted. First the binary to Gray code converter converts the code 1100 to 1010 Gray code. This code turns S3 and S1 on.

Hence $Iout-= I + 2I - 4I - 8I = -9I$ and

$Iout+= -I - 2I + 4I + 8I = 9I.$

And $Iout = 9I - (-9I) = 18I$

The current-steering mode Gray code input DAC is designed using MOSFETs as shown in Fig 7. The MOSFET current mirrors $M2, M3\ M4, M5$ generate $I, 2I, 4I, 8I$ respectively, while he MOSFETs $M6, M7, M8, M9$ generate currents $I, 2I, 4I, 8I$ respectively in the opposite direction.

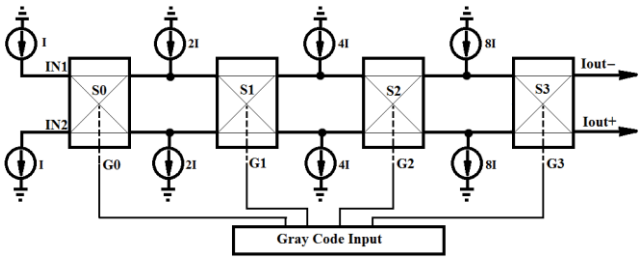


Fig 6: Current-steering Mode Gray code input DAC.

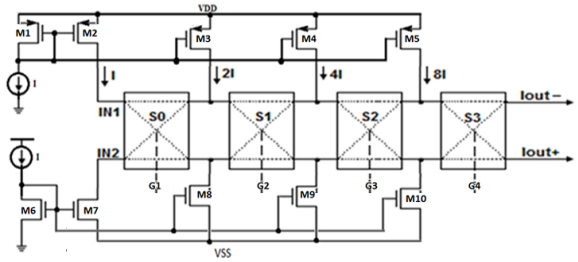


Fig.7. MOSFET level design of current-steering mode Gray code input DAC.

IV. SPICE Simulation Results

SPICE simulations of the above DAC topologies were carried out using TSMC 0.18um CMOS process parameters. First, simulation for the switches in the DAC was carried out and then the DAC was simulated using resistors and current sources. After successful simulation, the resistors and current sources were replaced with their MOSFET equivalents and then simulated. The switches used are DPDT switches modelled using LTSpice switch SW as well as NMOSFETs. The MOSFET aspect ratio is W/L=2u/0.18u.

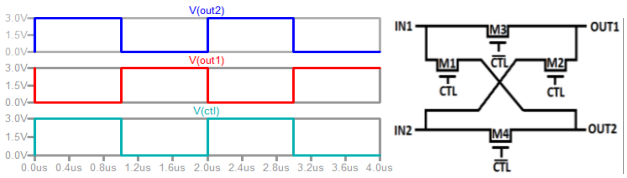


Fig 8: Circuit diagram and simulation results of a DPDT switch using NMOSFETs.

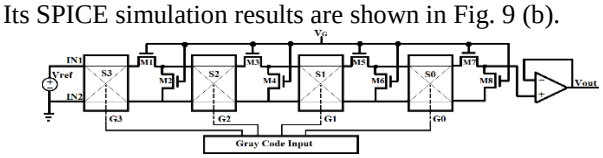
A. Simulation of Voltage-Mode Gray Code Input DAC

The resistor-based voltage-mode Gray code input DAC contains resistor values of R=10k, 2R=20k, 1.5R=15k and 0.5R=5k. Gray code input is applied directly through voltage pulses that are the same as obtained from the binary to Gray code converter. MOSFET based design was carried out using the same configuration with the following MOSFET aspect ratios (Fig.9 (a)):

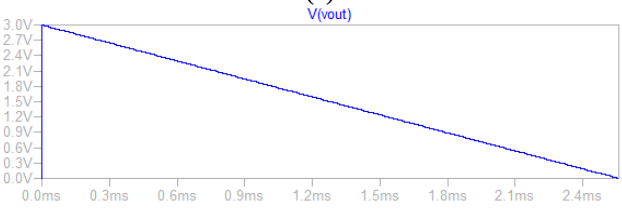
R: W/L=0.58u/1.35u, 2R: W/L=0.576/3u

1.5R: W/L=0.576u/2.162u, 0.5R: W/L=0.57u/0.5u.

Its SPICE simulation results are shown in Fig. 9 (b).



(a)

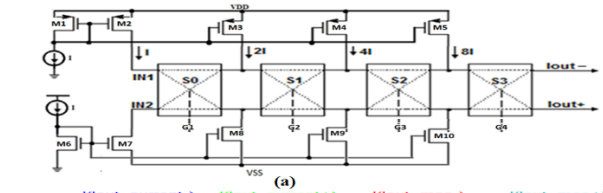


(b)

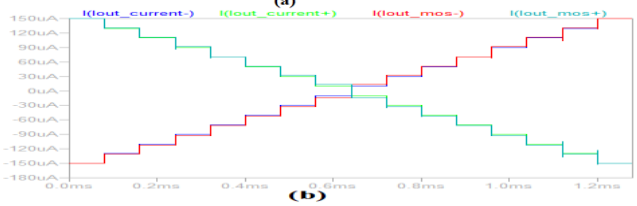
Fig 9: (a) Circuit diagram of voltage mode Gray code input DAC. (b) Simulation results

B. Simulation of Current Steering Gray Code Input DAC

A 4-bit current-steering Gray code input DAC was implemented with current sources of I=10uA, 2I=20uA, 4I=40uA and 8I=80uA. The output is terminated by an operational amplifier with a 1k feedback resistor (Fig.6). Using MOSFET current mirrors to generate currents of 10uA, 20uA, 40uA and 80uA, the current steering Gray code input DAC was designed (Fig.10 (a)), and its SPICE simulation results are shown in Fig. 10(b).

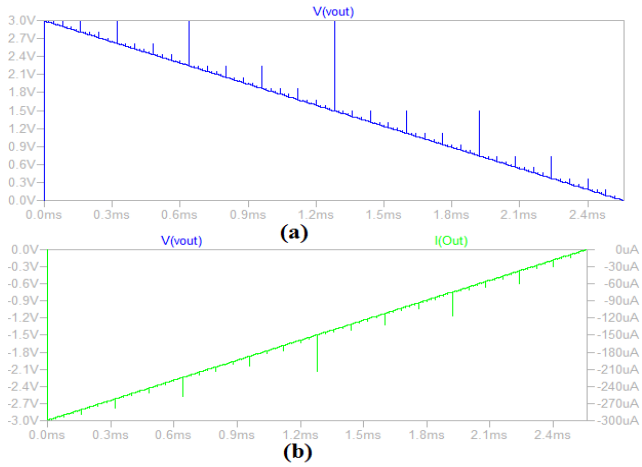


(a)



(b)

Fig 10: (a) Circuit diagram of current steering mode Gray code input DAC and (b) simulation results



(a)

(b)

Fig11: Output waveforms. (a) Voltage mode binary input R-2R DAC. (b) Current mode binary input R-2R DAC.

The outputs of R-2R DAC voltage mode and current mode are as shown in Fig. 11 (a) and (b) respectively, which shows that they are full of glitches. On the other hand, Gray code input versions reduce glitches considerably, as shown in Fig. 9 (b), Fig. 10 (b).

V. Conclusion

We have proposed Gray code input DAC topologies and designed them with voltage and current-steering modes. We have shown with SPICE simulation that the proposed DACs have significantly small amount of glitches compared to conventional binary code input DACs.

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