Optimization and Analysis of High Reliability 30-50V Dual RESURF LDMOS

Jun-ya Kojima, Jun-ichi Matsuda, Masataka Kamiyama, Nobukazu Tsukiji, Haruo Kobayashi

Division of Electronics and Informatics, Gunma University, 1-5-1, Tenjin-cho Kiryu, Gunma, Japan 376-8515
Email: koba@gunma-u.ac.jp

Abstract - This paper describes an optimized dual RESERUF LDMOS with enhanced reliability for 30-50V automotive applications. The proposed LDMOS is designed to suppress drain current expansion due to Kirk effect. Simulation verified that the avalanche breakdown voltage is scalable from 32 to 60V, with the breakdown location always in the bulk, ensuring good ESD performance. Low specific on-resistance of 44.8mΩmm^2 at breakdown voltage of 60.7V is also obtained. Furthermore, the LDMOS indicates superior low power dissipation in the practical switching frequency range of DC-DC converters.

1. Introduction

Lateral Double-diffused MOSFETs (LDMOS) for automotive applications require high reliability, wide Safe Operating Area (SOA), and high Electro Static Discharge (ESD) endurance. However the conventional LDMOS generally has reliability and SOA problems due to impact ionization caused by hot carriers as well as a drain current increase, Current Expansion (CE) phenomenon, due to Kirk effect at high V_{DS} and V_{GS} [1], [2]. In order to overcome the problems, it is necessary to suppress impact ionization around the gate-side drift edge of an LDMOS as well as the CE phenomenon. Furthermore, in order to enhance ESD endurance it is necessary to cause avalanche breakdown not at the surface but in the bulk of an LDMOS.

We proposed a new LDMOS structure for 30-50V operation to meet the above requirements with low specific on-resistance [3], [4]. Here we optimize and analyze electrical characteristics for the new LDMOS in detail by using a device simulator, DESSERT (β version) developed by AdvanceSoft Corporation, and show scalability of avalanche breakdown voltages as well as superior low power dissipation for the LDMOS.

2. Device structures

All the structures simulated are based on 0.35μm CMOS process. Fig. 1 shows cross-sectional views of the conventional ① (Fig. 1a), ② (Fig. 1b) [3], and the proposed LDMOS (Fig. 1c) [4]. The conventional ② and the proposed LDMOS have dual p-buried layers; p-buried layer 1 contributes to a reduced surface field (RESURF) structure near the drift edge strongly, and p-buried layer 2 to that for the rest of the drift layer uniformly. The proposed LDMOS has the Field Plate (FP) over the drift layer. The oxide thickness under the FP is 312nm. The length of the drift layer in the LDMOS (2650nm) is 300nm shorter than that in the conventional ① and ② LDMOS. The LDMOS also has higher impurity doses in the source n+ and the drift regions than the conventional ① and ② LDMOS. Furthermore, the drift layer for all the LDMOS consists of shallow and deep drift layers. The shallow drift layer is effective for enhancement of SOA [5].

3. Simulation Results

3.1 Optimization of proposed LDMOS

In order to obtain maximum avalanche breakdown voltage between the drain and the source, BV_{DS}, we optimized the impurity dose in the shallow drift layer and the FP length, the distance from the drain-side gate edge to the FP edge over the drift layer. Fig. 2 shows BV_{DS} dependences on the impurity dose and the FP length. The BV_{DS} dependence on the impurity dose was observed at a fixed FP length of 1625nm. The dependence has a peak of 60.7V at a dose of 2.13×10^{12}cm^{-2}. With this dose fixed, the BV_{DS} dependence on the FP length was observed. The dependence all but has a peak at the FP length of 1625nm. Therefore the above impurity dose and FP length result in a BV_{DS} of 60.7V. The BV_{DS} is high enough for 50V operation, because it has a margin of more than 10V for breakdown.

3.2 Static electrical characteristics

Fig. 3 shows I_{DS}-V_{DS} characteristics of the conventional ①, ②, and the optimized LDMOS at V_{GS}=5V. Fig. 3 states that the conventional ① LDMOS starts to generate weak CE at around V_{DS} = 30V, while the conventional ② and the optimized LDMOS have current increases different from CE over V_{DS} = 40V because of dual RESURF structure.

Fig. 4 shows hole current density profiles along the surface, caused by impact ionization, at V_{GS} = 5V, V_{DS} = 40V. The hole current density profiles of the optimized and the conventional ② LDMOS are much lower than

978-1-4673-9719-3/16/$31.00 ©2016 IEEE

that of the conventional ① LDMOS near the drift edges. Although the hole current density profile of the optimized LDMOS has a peak around x = 1900 nm, it decreases to almost the same level as that of the conventional ② LDMOS near the gate-side drift edge. Therefore the intrinsic MOSFETs of the optimized and the conventional ② LDMOS suffer much smaller damages from impact ionization than that of the conventional ① LDMOS.

Fig. 5 shows electric filed magnitude profiles along and near the surface at V_{GS} = 5V, V_{DS} = 40V. It is noticed that the profiles for the conventional ① and ② LDMOS have peaks near the drain-side drift edge due to Kirk effect, leading to hole current generation there (see Fig. 4), but that of the optimized LDMOS does not.

Table 1 compares specific on-resistance, $R_{on}A$, and BV_{DS} values between the conventional ①, ②, and the optimized LDMOS. $R_{on}A$ value for the optimized LDMOS is the lowest. Meanwhile, even though BV_{DS} value for the LDMOS is the lowest, it is enough for 50V operation.

Fig. 6 shows $R_{on}A$-BV_{DS} characteristics. Here we obtained an $R_{on}A$-BV_{DS} characteristic from the optimized LDMOS by only changing the lengths of p-buried layer 1 and 2, and FP in proportion to changes in the drift length. The characteristic is linearly scalable in the BV_{DS} range of 32-60V, and it is comparable to state-of-the-art ones.

Avalanche breakdown locations of the conventional ①, ② and the optimized LDMOS are all in the bulk, so all the LDMOS would have good ESD performance.

3.3 Switching loss and total power dissipation

Fig. 7 shows the circuit for switching loss analysis. Table 1 also compares Figure of Merit (FOM) of $R_{on}Q_g$, on-resistance times gate charge. The FOM value for the optimized LDMOS is larger than that for the conventional ② LDMOS due to a larger capacitance between the gate and the drain caused by FP (Miller capacitance), indicating larger switching loss for the optimized LDMOS.

Fig. 8 shows frequency dependence of the total power dissipation density including gate driving loss, switching loss, and on-state conduction loss by changing the duty ratio, D_{ON}, as a parameter. Fig. 8 states that although at D_{ON}=0.1, the frequency range in which the total power dissipation for the optimized LDMOS is smaller than that for the conventional ② LDMOS is less than 1.5MHz, for $D_{ON} \geqq 0.5$, it increases up to more than 9MHz due to the much lower $R_{on}A$ value, albeit the worse FOM value for the optimized LDMOS. Therefore the LDMOS indicates superior low power dissipation in the practical switching frequency range of DC-DC converters.

4. Conclusion

We have obtained an optimized dual RESURF suppressing impact ionization near the gate-side drift edge, causing no drain current expansion, resulting in high reliability and wide SOA suitable for automotive applications by simulation. The LDMOS is scalable in the range of avalanche breakdown voltages of 32-60V with a low specific on-resistance comparable to state-of-the-art performance, and indicates superior low power dissipation in the practical switching frequency range of DC-DC converters. Furthermore, the avalanche breakdown location of the LDMOS is in the bulk, so good ESD performance is expected.

Acknowledgements

We would like to express sincere thanks to AdvanceSoft Corporation for lending us 3D TCAD simulator. The development of this simulator is assisted by A-STEP program of Japan Science and Technology Agency, National Research and Development Agency.

References

[1] Stefano Poli, et al., "Optimization and Analysis of the Dual n/p-LDMOS Device," IEEE Trans. Electron Devices, Vol. 59, No. 3, pp. 745-753 (2012).

[2] Jingxuan Chen, "HV EDMOS Design with Expansion Regime Suppression," Master Thesis of Applied Science, Department of Electrical and Computer Engineering, University of Toronto, (2013).

[3] Jun-ichi Matsuda, et al., "A Proposal of High Reliability LDMOS Structure," EDD-15-066, SPC-15-148, pp. 11-16 (2015).

[4] Jun-ichi Matsuda, et al., "A Proposal of High Reliability Dual RESURF Nch-LDMOS with Low On-resistance," The 63rd JSAP Spring Meeting, Tokyo Institute of Technology, 20a-S422-11 (2016).

[5] P. L. Hower, et al., "Snapback and Safe Operating Area of LDMOS Transistors," IEDM'99, pp. 193-196(1999).

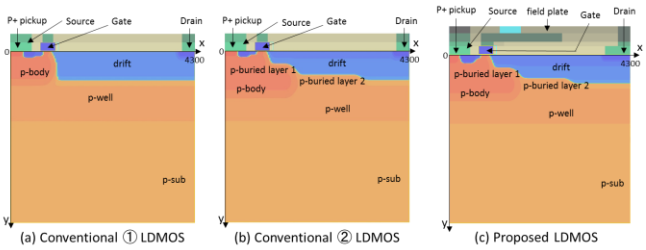

Fig. 1. Cross-sectional views of the conventional ①, ②, and the proposed LDMOS.

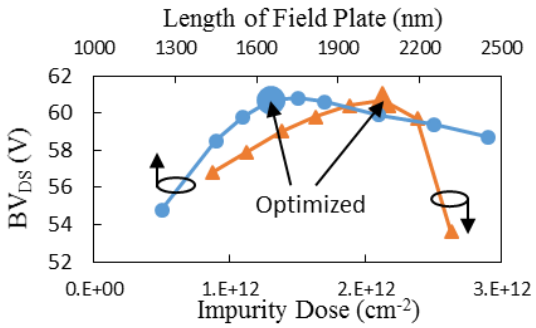

Fig. 2. BV_{DS} dependence on the impurity dose in the shallow drift layer and the length of the field plate for the proposed LDMOS.

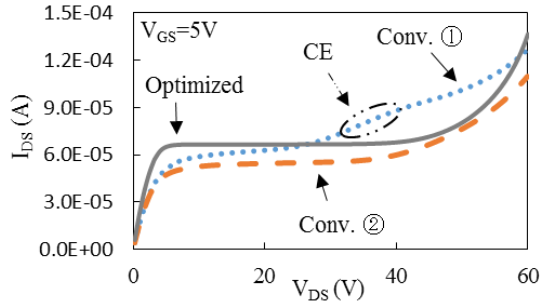

Fig. 3. I_{DS}-V_{DS} characteristics; the gate length and width of the LDMOS are 0.35μm and 0.3μm, respectively.

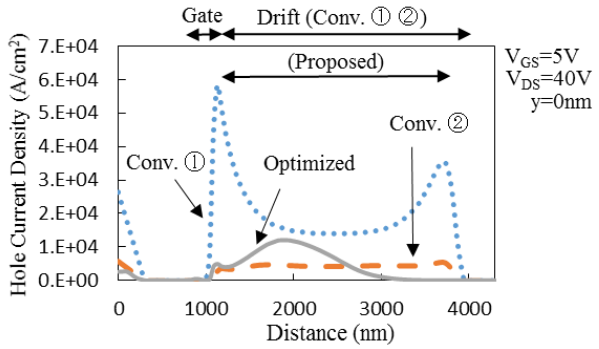

Fig. 4. Hole current density profiles along the surface.

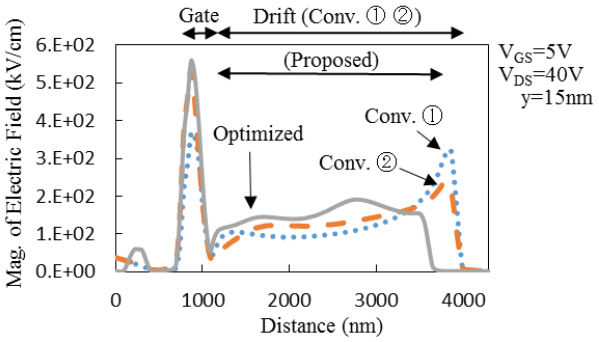

Fig. 5. Electric field profiles along and near the surface.

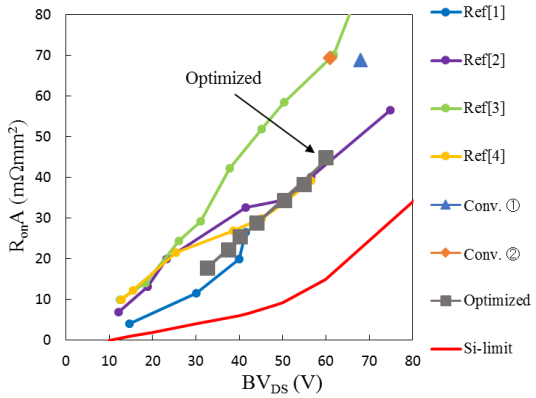

Fig. 6. $R_{on}A$-BV_{DS} characteristics.

Ref[1]:S.Pendharkar, "7 to 30V State-of-Art Power Device Implementation in 0.25μm LBC7 BiCMOS-DMOS Process Technology," ISPSD, p419-422, (2004).
Ref[2]:R.Zhu, "Implementation of High-Side, High-Voltage RESURF LDMOS in a Sub-Half Micron Smart Power Technology," ISPSD, p403-406, (2001).
Ref[3.4]:Choul-Joo Ko, et al., "Implementation of Fully Isolated Low Vgs NLDMOS with Low Specific On-Resistance," ISPSD, pp. 24-27, (2011).

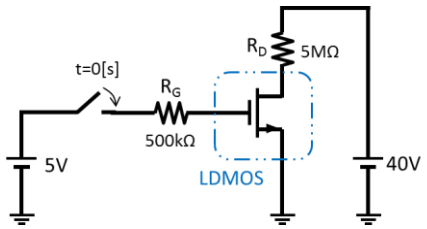

Fig. 7. Circuit for switching loss analysis; the gate length and width of the LDMOS are 0.35μm and 0.3μm, respectively.

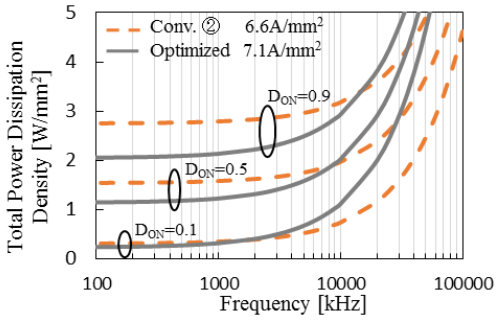

Fig. 8. Frequency dependence of the total power dissipation density.

Table 1. Comparison of $R_{on}A$, BV_{DS}, and FOM($R_{on}Q_g$) values between the conventional ①, ②, and the optimized LDMOS.

Items	Conv. ①	Conv. ②	Optimized
$R_{on}A$ (at V_{GS}=5V) (mΩmm²)	68.7	69.3	44.8
BV_{DS} (V)	67.6	61.0	60.7
FOM (=$R_{on}Q_g$) (mΩnC)		104	141