Limit Cycle Suppression Technique Using Digital Dither in Delta Sigma DA Modulator

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Abstract - This paper proposes a digital dither technique to suppress limit cycles in a ΔΣ DA modulator. It uses an exclusive OR (XOR) gate at the modulator output and the digital dither is generated by another ΔΣD modulator. The resolution of the DAC following the modulator is 1-bit (instead of multi-bit) thanks to XOR gate usage, and the overall SNR does not degrade because the dither is added at the output and hence it is noise-shaped. Our MATLAB simulation and FPGA implementation results have verified the effectiveness of the proposed method.

1. Introduction

A ΔΣ DA converter consists of mostly digital circuit, and it is frequently used for electronic measurement and test equipment as well as audio systems because it can produce highly linear DC and low frequency signal with high resolution (Fig. 1). However the ΔΣ DA modulator suffers from a limit cycle problem when its input amplitude is small [1, 2, 3, 4].

We propose here a digital dither method to solve this problem. It uses an XOR gate at the modulator output and the digital dither. The proposed method has 3 important features: (i) A 1-bit DAC following the modulator can be used thanks to using an XOR gate. (ii) The digital dither is noise-shaped and does not affect the SNR because it is effectively added at the modulator output. (iii) A digital dither is also generated by another ΔΣ digital modulator.

Our MATLAB simulation results as well as FPGA implementation results confirm that the limit cycles are suppressed for all 10, 14, 16, 18-bit cases.

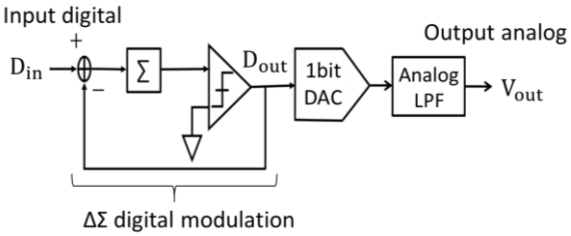

Fig. 1. Block diagram of the first-order ΔΣ DA converter

2. ΔΣDA modulator (Digital modulator)

< 2.1 > ΔΣ DA modulator configuration

A ΔΣ DA modulator consists of all digital circuits with feedback configuration using an integrator and a comparator (Fig. 1). The error signal is accumulated at the integrator, and its output compared by a comparator. The comparator output (0 or 1) is the ΔΣ modulator output. Also the comparator output is fed back to the input. It is known in [1, 2] that the output power spectrum is noise-shaped; quantization noise is reduced at low frequency while increased at high frequency.

< 2.2 > ΔΣ modulator with digital dither

The digital dither, 0 or 1, is defined as (pseudo-)random signal, and it is used to remove the limit cycles of the ΔΣ DA modulator when input amplitude is very small. If the digital dither is added at the input of the modulator, the noise component is increased so that the overall SNR may degrade. On the other hand, if it is directly added to the ΔΣ modulator output, a multi-bit DAC (instead of a 1-bit DAC) following the modulator is required, and the multi-bit DAC suffers from nonlinearity problem [1, 2]. The proposed technique solves these two problems.

< 2.3 > Proposed ΔΣ modulator with XOR

We propose here a new technique using XOR gate whose inputs are the comparator output and the digital dither generated by another modulator (Fig. 2). The modulator output is the XOR output; in case the dither signal (D_{dither}) is 0, the modulator output (D_{out}) is the same as the comparator output (D_{on}) (or no dither is added), while in case the dither signal (D_{dither}) is 1, the modulator output is the reverse of the comparator output (D_{on}) (or effectively dither is added).

Appearance frequency of 1 for the dither signal (D_{dither}) can be adjusted by changing the amplitude and the center value of the input dither signal (D_{ind}). When the amplitude and the center value are very small, the frequency of the dither signal of 1 is low, and vice versa.

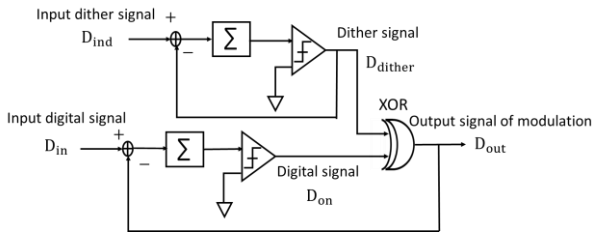

Fig. 2. Proposed ΔΣ DA modulator with digital dither

3. MATLAB Simulation Results

< 3.1 > Limit Cycle Suppression (10 bit case)

We have verified the effectiveness of the proposed

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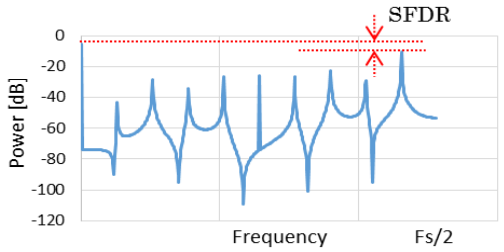
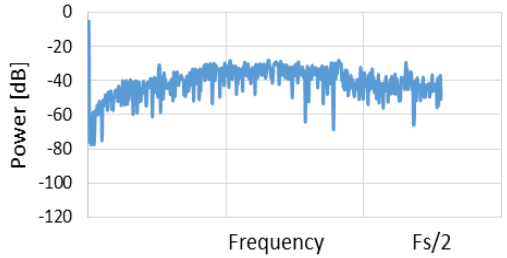
technique (Fig. 2). We use a sinusoidal signal (Dind) whose period is 10K-point for the dither generator and its amplitude and center values are controlled for limit cycle reduction. In addition, we have checked that the numbers of 1's at the modulator output are the same in both cases of with and without dither for DC input (full scale:-1 ~ +1) of Din.

Fig. 3 shows simulation results when the DC input of Din is 0.1. We see that the limit cycle of the proposed circuit with dither (Fig. 3 (b)) is lower than that without dither (Fig. 3 (a)), and also that Spurious Free Dynamic Range (SFDR) with dither (22.9dB) is higher than that without dither (5.4dB).

In a similar manner, Fig. 4 shows the amplitude and the center values of the input sine wave (Dind) adjusted according to the modulator DC input (Din) for limit cycle reduction. We compare SFDRs with dither and without dither and we see in Fig. 5 that it is improved for all range of the DC input (Din).

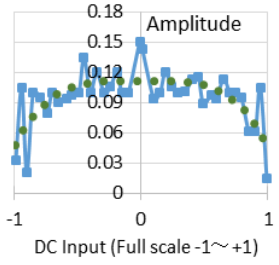


(a) Without dither

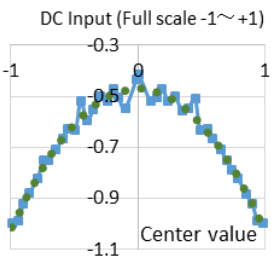


(b) Dither modulator sine wave input (Dind) of amplitude: 0.094, center value: -0.520.

Fig. 3. Power spectrum of ΔΣ modulator output in case that the DC input (Din) is 0.1.



(a) Amplitude



(b) Center value

Fig. 4. Dither generation modulator input sine wave for limit cycle reduction (Dot lines are approximation).

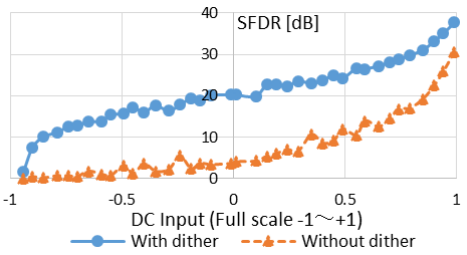
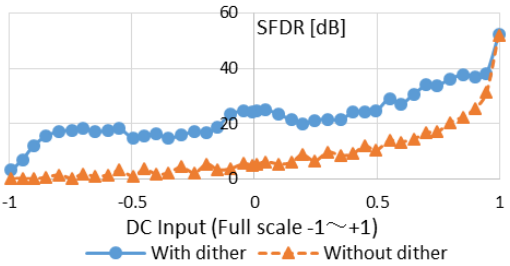


Fig. 5. SFDR comparison (simulation results)

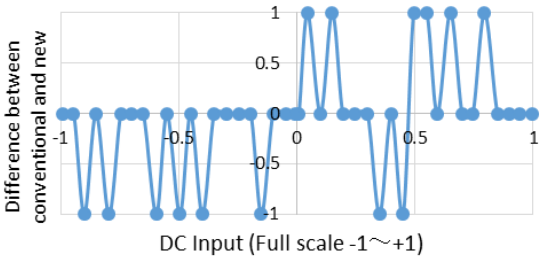
< 3.2 > Study on reduced circuit of the limit cycle (14, 16, 18-bit cases)

Section 3.1 describes the validation of the proposed algorithm. We modify this original method for ease of FPGA implementation; digital sinewave generation with controlled amplitude and center values is complicated for implementation, and here we replace a sinewave with a triangular wave for the dither modulator input.

Fig. 4 shows approximation graph to determine the amplitude and the center value of sine wave for a certain DC input, and there only DC input change is enough. We have simulated using this method in 14, 16, 18-bit cases, and their results are shown as Figs. 6, 7 and 8. We see in Fig. 6(a), 7, 8 that SFDR is improved for the DC input of full scale between -1 and +1. Fig. 6(b) shows the difference of the modulator output 1's numbers with and without the proposed dither in 14-bit case. We see that the proposed circuit maintains the DC linearity because the difference number of 1's is within a ±1 range. We also see in Figs. 7, 8 that the linearity is maintained in 16-bit and 18-bit cases.



(a) SFDR comparison



(b) Linearity

Fig. 6. Simulation results in 14-bit case.

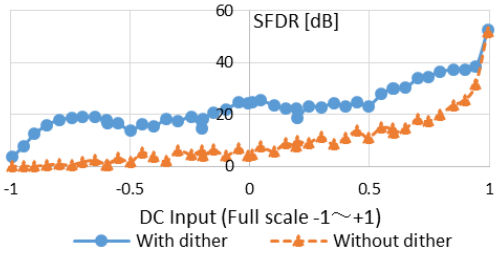


Fig. 7. SFDR simulation results in 16-bit case.

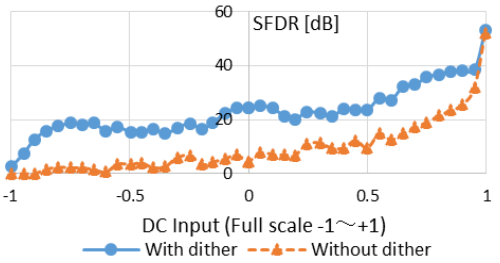


Fig. 8. SFDR simulation results in 18-bit case.

< 3.3 > FPGA design

Fig. 9 shows digital circuit design in Fig. 2, and it was implemented on an FPGA, based on the description in section 3.2. The amplitude of the triangular wave is 0.256 for design simplicity, and its center value is chosen as shown in Fig. 10 (see Fig. 4(b)). Also the DC input (Din) range is from -0.8 to +0.8.

Fig. 11 shows simulation results; we see in Fig. 11(a) that SFDR improves for the DC input from -0.8 to +0.8, and also Fig. 11(b) shows the difference between numbers of modulator output 1's with and without the proposed dither in 10-bit case and we see that the difference is within ±2. Fig. 12 shows the FPGA board.

4. Conclusion

We have proposed a new digital dither technique for limit cycle suppression and SFDR improvement in ΔΣ DA modulators. It uses an XOR gate at the modulator output and the digital dither is generated by another ΔΣD modulator or triangle wave generator (counter). The resolution of the DAC following the modulator is 1-bit (instead of multi-bit) thanks to XOR gate usage, and the overall SNR does not degrade because the dither is added at the output and hence it is noise-shaped. We have performed MATLAB simulation and FPGA implementation which verified the effectiveness of the proposed method.

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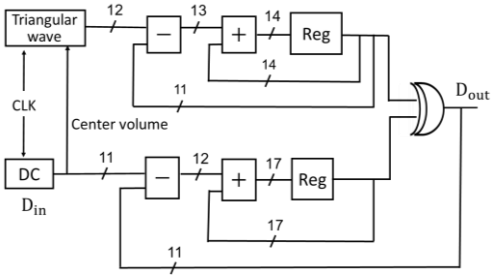


Fig. 9. Digital circuit design of the proposed modulator.

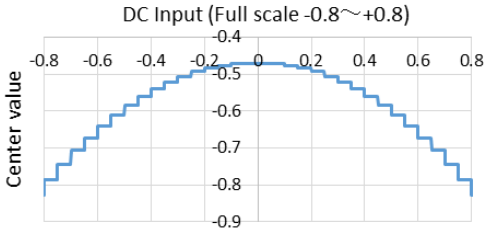
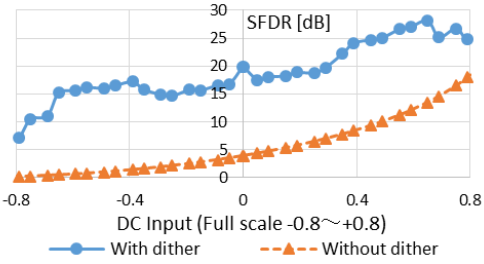
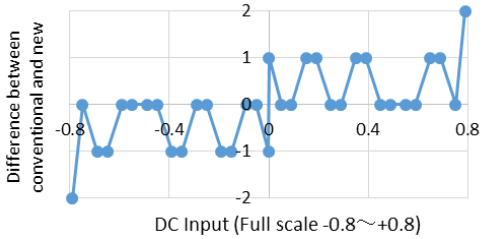


Fig. 10. Input triangular wave center value.



(a) SFDR comparison



(b) Difference between numbers of modulator output 1's with and without the proposed dither.

Fig. 11. FPGA simulation results of the circuit in Fig. 9.

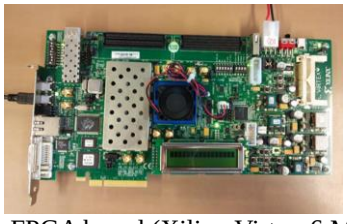


Fig. 12. FPGA board (Xilinx Virtex-6 ML605).