Analog / Mixed-Signal Circuit Design Based on Mathematics

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Abstract - This paper presents that techniques of mathematics, such as number theory, statistics, coding theory, modulation, control theory, and signal processing algorithms besides transistor-level circuit design are required to enhance the performance of analog/mixed-signal circuit performance. Several research examples in the authors' laboratories are shown.
Keywords: analog circuit, mixed-signal circuit, signal processing, number theory, coding theory, statistics

1. Introduction

Analog circuit design at the transistor level is art rather than technology, with which industry can differentiate their products. However, as the LSI technology advances, digital technology can be utilized and so called digitally-assisted analog/mixed-signal circuit technology becomes effective [1]. It uses mathematics such as signal processing and control theory extensively. This paper introduces such research results at the author's laboratory and validates our argument that beautiful mathematics leads to very good circuit/system design.

2. Control Theory and Operational Amplifier Design

We propose to use Routh-Hurwitz stability criterion for analysis and design of the opamp feedback stability, after deriving its small equivalent circuit and transfer function; this can lead to explicit stability condition derivation for opamp circuit parameters, which would be effective when it is used together with Bode plots [2].

3. Fibonacci Sequence and SAR ADC Design

We have investigated a redundant successive approximation register (SAR) ADC design method for high-reliability and high-speed AD conversion using digital error correction [3, 4]. We apply Fibonacci sequence *Fn* and its property of convergence to the Golden ratio φ there.

$$F_{n+2} = F_n + F_{n+1} \qquad F_0 = 0, \qquad F_1 = 1$$

*F*n = 0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, 233,…

$$\lim_{n\to\infty} \frac{F_n}{F_{n-1}} = 1.6180339887 = \varphi$$

We have found that the SAR AD conversion time becomes the shortest when Fibonacci sequence weights are used and the internal DAC incomplete setting is considered. We have come up with simple golden-ratio weighted DAC topologies (R-R ladder, C-C ladder) for its internal usage.

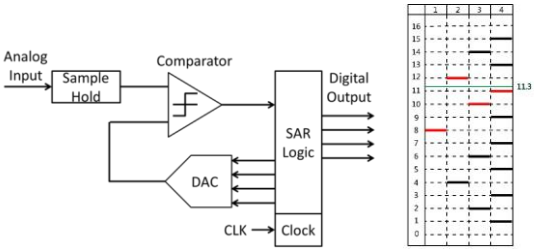
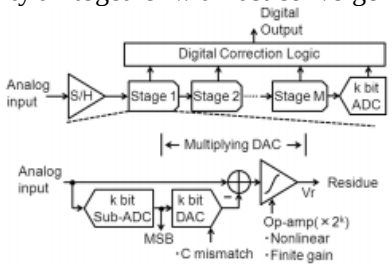


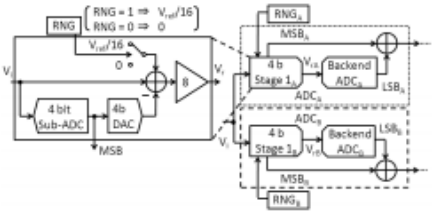
Fig. 1. SAR ADC configuration and operation steps.

4. Adaptive Signal Processing and ADC Calibration

We investigate a background calibration algorithm for a pipelined ADC with an open-loop amplifier using a split ADC structure and adaptive signal processing [5, 6]. The open-loop amplifier is employed as a residue amplifier in the first stage of the pipelined ADC for low power and high speed. However it suffers from nonlinearity, and hence needs calibration. We investigate the split ADC structure for fast background calibration of the residue amplifier nonlinearity and gain error as well as the DAC nonlinearity all together with fast convergence.



(a) Pipeline ADC and stage circuit



(b) First Stage where split ADC is used.

Fig. 2 Investigated pipeline ADC topology

5. Correlation and ADC Timing Correction

We investigate a digital method of reducing timing

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mismatch effects in time-interleaved ADCs (Fig.1(a)) used in ATE systems [7]: we use correlation (Fig.1(b)) among channel ADC outputs to detect channel timing skew, and make successive approximation (SA) adjustments to our linear-phase digital delay filter [8] to compensate for the timing skew. Simulation results validate the effectiveness of the proposed method. We found that using multi-tone input signals with correlation of outputs provided a more robust way of detecting timing skew than using a single-tone input.

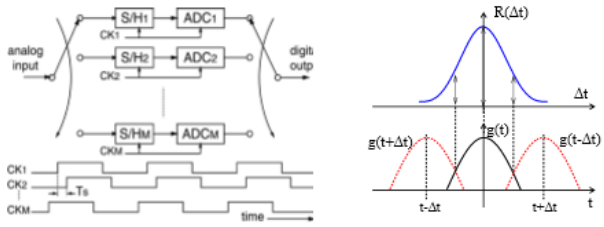


Fig. 3 (a) Interleaved ADC. (b) Auto-correlation (right).

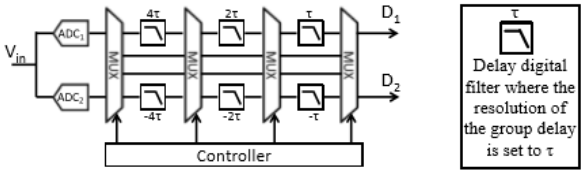
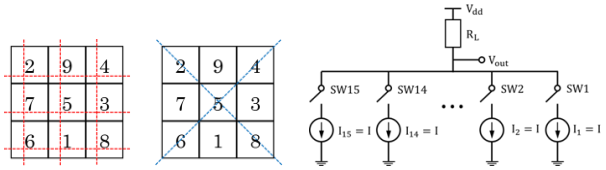


Fig.4 Successive approximation minimization of timing skew using our delay digital filter.

6. Magic Square and DAC Design

We propose a switching or current source sorting algorithm using magic square properties (Fig. 5 (a)) to improve the linearity of a unary digital-to-analog converter (DAC) (Fig. 5 (b)) by canceling random and systematic mismatch effects among unit current cells [8]. Simulation results show DAC linearity improvement with the proposed algorithm.



(a) (b)

Fig. 5. (a) Magic square and constant sum characteristics. (b) Unary current-steering DAC.

7. Residue Arithmetic, Gray Code and TDC Design

A time-to-digital converter (TDC) measures the rising edge timing difference between Start and Stop signals and provides digital output. Fig. 6 shows a basic flash-type TDC, however it requires large hardware and power. We investigate a TDC architecture with residue arithmetic or Chinese Remainder theorem [10], because its residues can be obtained easily with ring oscillators. It can reduce hardware and power significantly compared to a basic flash-type TDC while keeping comparable performance.

However, the residue arithmetic TDC can cause some glitches due to the delay mismatches. Then we came up with its improvement, a glitch-free TDC based on Gray code [11] (Table I, Fig. 7). Gray-code (reflected binary code) is a binary numeral system where two successive values differ in only one bit. So a Gray-code driven DAC is capable to reduce the glitch. The proof-of-concept prototype of Gray code based TDC was implemented on FPGA.

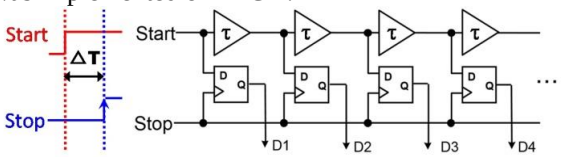


Fig. 6. Basic flash-type TDC

Table I Binary and Gray codes

Decimal numbers	Binary Code	Gray Code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

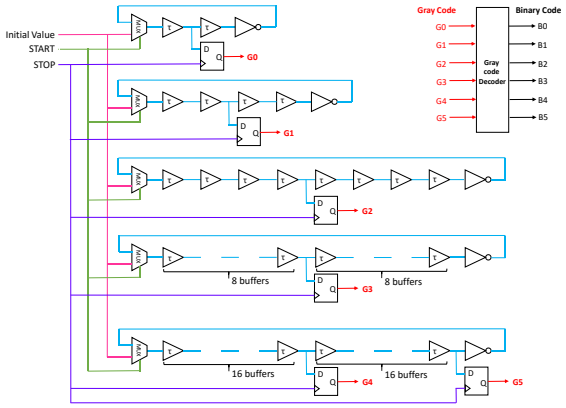


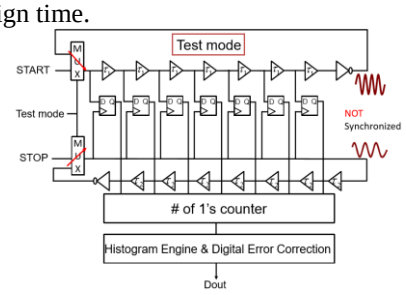
Fig.7 6-bit Gray code based TDC architecture

We have also designed Gray code input DAC topologies (current, voltage and charge modes) for glitch reduction.

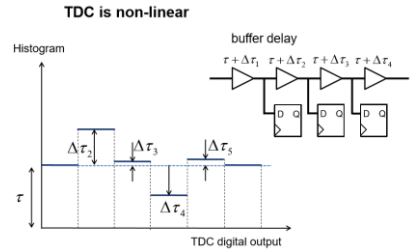
8. Histogram and TDC Linearity Calibration

We have studied the flash-type TDC linearity self-calibration calibration, with histogram obtained by uncorrelated ring oscillators (Fig. 8) [12]. FPGA measurement results show that TDC linearity is improved by the self-calibration [13] (Fig. 9). All TDC circuits, as well as the self-calibration circuits can be implemented as digital FPGA instead of full custom ICs,

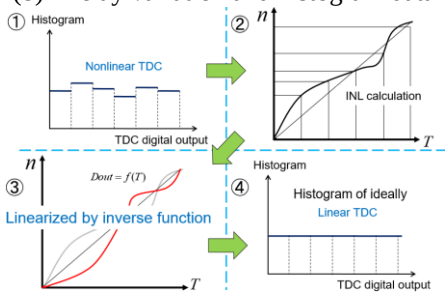
which is suitable for fine CMOS implementation with short design time.



(a) Histogram data acquisition



(b) Delay variation and histogram data



(c) TDC linearity correction with digital calculation

Fig. 8 TDC linearity calibration principle.

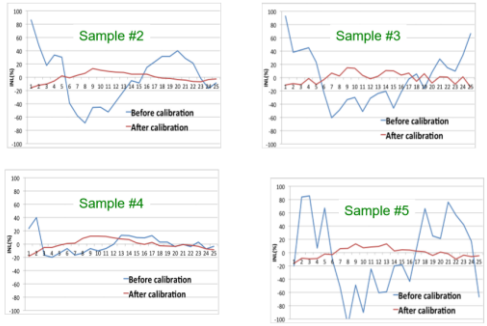


Fig. 9 Measured results of TDC nonlinearity before and after the proposed calibration.

9. Statistics and Fine Time-Resolution TDC Design

We have investigated another TDC architecture to measure the timing difference between single-event two pulses with fine time resolution [12, 14]. Its features are as follows: (i) The architecture is based on stochastic process and statistics theory. (ii) It utilizes the stochastic variation in CMOS process positively for fine time resolution so that MOSFETs with minimum sizes are utilized. (iii) It needs a large number of D Flip-Flops (DFFs) for statistics but advanced fine CMOS technology can realize it. The larger the number of DFFs is, the finer the time resolution is. (iv) The self-calibration technique using the histogram method is applied to compensate the nonlinearity due to the circuit characteristics variation as well as timing skew by layout and routing. (v) The proposed TDC can be implemented with full digital circuit including the self-calibration circuit.

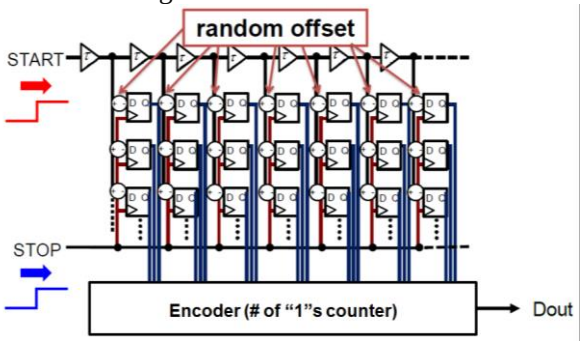


Fig. 10 Investigated stochastic TDC architecture

10. ΔΣ Modulation, DWA and TDC

We investigate design and implementation of a multi-bit ΔΣ TDC with Data Weighted Averaging (DWA) algorithm on analog FPGA [15] (Figs. 11, 12). We propose here simple test circuitry for measuring digital signal timing of I/O interfacing circuits. We focus on ΔΣ TDC for fine timing-resolution, digital output, and simple circuitry. The ΔΣ TDC can measure the repetitive signal timing; as the measurement time is longer, its time resolution becomes finer. We also use multi-bit architecture for short testing time. However, the multi-bit ΔΣ TDC suffers from delay mismatches among delay cells. Then we apply the DWA algorithm, which averages the mismatches in time and obtain good linearity.

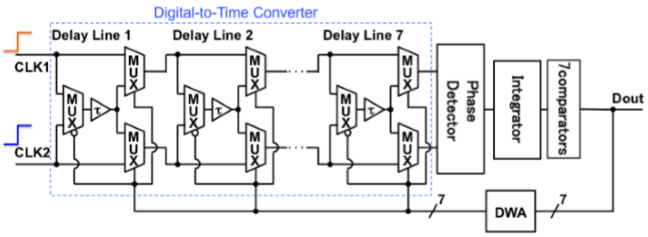
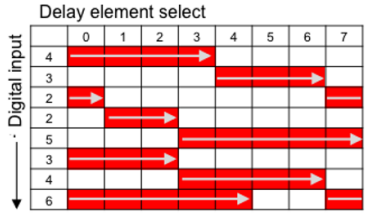
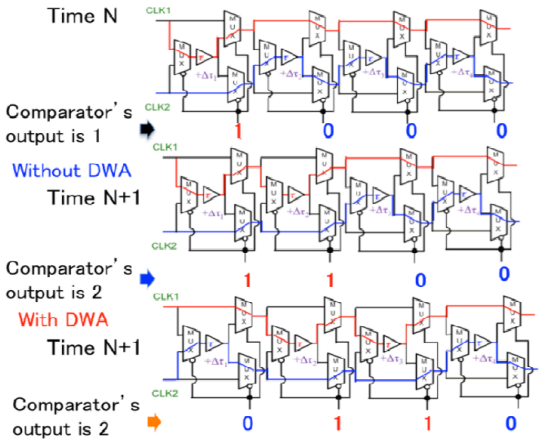


Fig. 11. Multi-bit ΔΣ TDC with DWA logic



(a) DWA operation

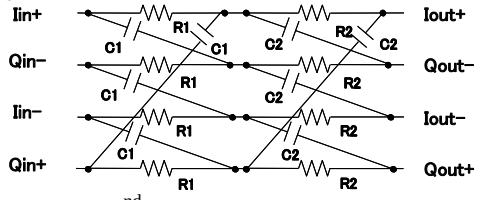


(c) Delay cell selection without and with DWA.

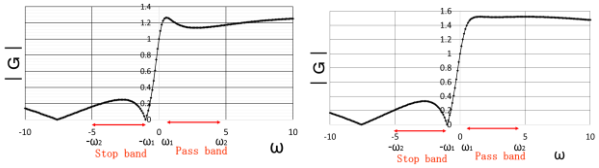
Fig.11 DWA operation in multi-bit ΔΣ TDC.

11. Complex Signal Processing and Analog Filter

We derive a design algorithm of a 2nd-order RC polyphase filter (which has complex or quadrature analog inputs and outputs) to obtain its flat passband gain, using its Nyquist chart [16]. The condition for its solution as well as the image rejection ratio formula are also derived. We also clarify that the RC polyphase filer has characteristics as a complex analog Hilbert filter.



(a) 2nd order RC polyphase filter



(b) Gain characteristics, before and after the algorithm.

Fig. 12 2nd-order RC polyphaser filter and gain characteristics before and after the proposed algorithm

We have also developed complex or quadrature bandpass DWA algorithms [17]; concept of complex signal processing is useful especially communication circuits.

12. Concluding Remarks

This paper has presented that techniques of mathematics besides transistor-level circuit design are attractive to enhance the performance of analog/mixed-signal circuit performance in nano CMOS. It is the authors' experience that beautiful structure / topology of circuits and systems based on mathematics leads to very good performance.

The authors thank their lab members for contributions.

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