SEMICON® JAPAN

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Challenge for Analog Circuit Testing in Mixed-Signal SoC

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1. Introduction

Cost and Quality for Test Cost

- Analog portion continues to be difficult part of SoC test.
- Concept of "cost" and "quality" makes "issues and challenges of analog circuit testing in mixed-signal SoC" clear and logical.
- LSI testing technology reduces cost and improves quality simultaneously.

2. Review of Analog Circuit Testing in Mixed-Signal SoC

Management Strategy

- Strategy 1 :
  Use low cost ATE and develop analog BIST/BOST to make testing cost lower.
- Strategy 2 :
  Use high-end mixed-signal ATE
  as well as its associated services & know how.
  Fast time-to-market & no BIST
  can make profits much more than testing cost.

Save or Earn

ATE: Automatic Test Equipment

BIST: Built-In Self-Test, BOST: Built-Out Self-Testy

Low Cost Testing

Ideal : No testing

- Design guarantee
- 100% chips work well

Reality :

- Low cost ATE
- Short testing time
- Multi-site testing
- Minimum or no chip area penalty for BIST
- Extensive usage of BOST

A penny saved is a penny earned.

Test and Measurement are different

- Production Test : 100% Engineering

  Decision of "Go" or "No Go"

  For example, it can be performance comparison between DUT and "Golden Device".

- LSI testing is manufacturing engineering.

- Measurement : 50% Science, 50% Engineering

  Accurate performance evaluation of circuit

Measurement can be costly, but testing should be at low cost.

DUT: Device Under Test

Analog BIST

- BIST for digital : Successful
  BIST for analog : Not very successful
  ➡ Challenging research
- Digital test : Functionality ➡ Easy
  Analog test : Functionality & Quality ➡ Hard

Analog: parametric fault as well as fatal fault.

Prof. A. Chatterjee
Specification-based Test Alternative Test Defect-based Test

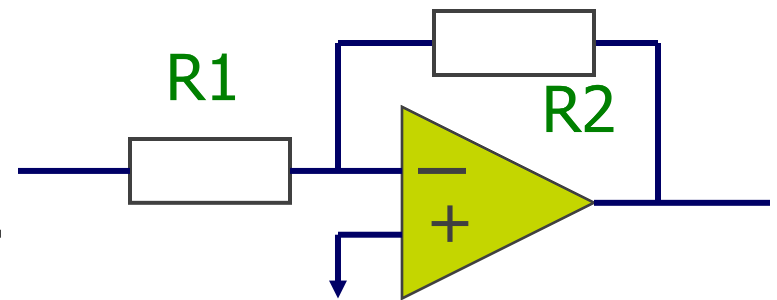
- In many cases
  - Analog BIST depends on circuit.
  - No general method like scan path in digital.
  - One BIST, for one parameter testing

RF / High-Speed IO / Power Device Testing

- RF / HSIO / Power testing is different from analog testing technology.
- These testing technologies are other challenging areas.
- RF testing items examples:
  - EVM test
  - System level testing, GSM/EDGE
  - AM/PM distortion
  - Jitter, Phase noise

Robust Design and Testing

Robust design makes its testing difficult.



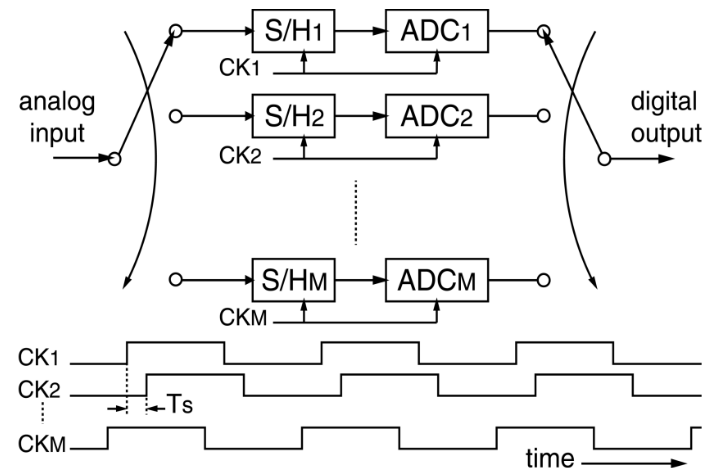
- Feedback suppresses parameter variation effects.
- Self-calibration and redundancy hide defects in DUT.
- Secure DUT is difficult to test.

Robust design (yield enhancement) and testing cost reduction are trade-off.

ATE for Mixed-Signal Testing

- Analog part is costly for development.
- Analog BIST is also beneficial
  for mixed-signal ATE manufacturer
- ATE must be designed with today's technology
  for tomorrow's higher performance chip testing.

Interleaved ADC used in ATE
to realize very high sampling rate
with today's ADCs



Low Cost ATE

- Digital ATE
  - No analog option such as Arbitrary Waveform Generator: AWG
  - Input/output are mainly digital.
- Replacement of analog ATE with digital ATE
  - Multi-site testing becomes possible.
  - Still short testing time is important.
- Secondhand ATE, In-house ATE
- ATE with well balanced modular hardware and software

Cooperation among Engineers

- Collaboration is important
  - Circuit designer
  - LSI testing engineer
  - ATE manufacturer engineer
  - Management
  - LSI testing researcher in academia
- Strong background of analog circuit design as well as LSI testing are required for analog testing research.

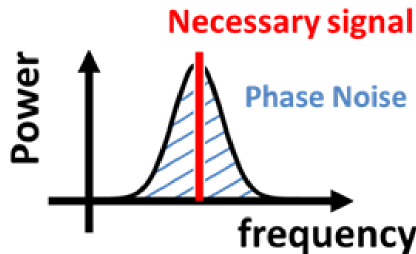
Collaboration with Socionext Inc., STARC and other related industries

3. Research Topics

Phase Noise Test with ΔΣ TDC

BOST solution

Phase noise in oscillator



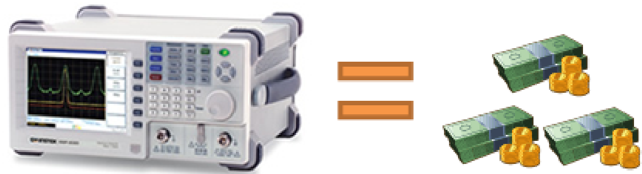
Malfunction of electronic systems

- RF circuit & system
- ADC

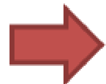
Important

Phase noise test at low cost, in short time

Conventional



- Expensive : Spectrum analyzer
- Long : test time (~10seconds)



cost high

Proposed

Simple circuit

||

ΔΣ Time-to-Digital Converter

Low cost, high quality
Phase noise test

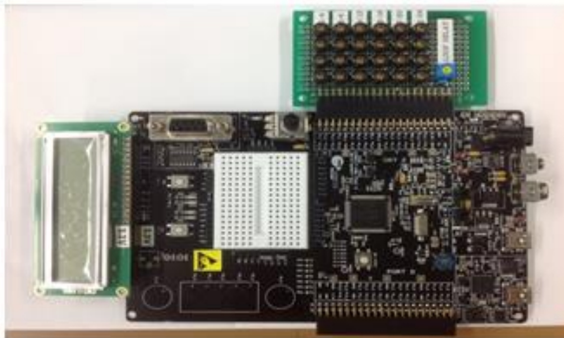
[1] Y. Osawa, H. Kobayashi, "Phase Noise Measurement Techniques Using Delta-Sigma TDC", IEEE International Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW'14), Porto Alegre, Brazil (Sept. 17-19, 2014).

TDC BOSTs for Timing Signal Testing

BOST solution

Single-bit ΔΣ TDC with analog FPGA

Multi-bit ΔΣ TDC with analog FPGA



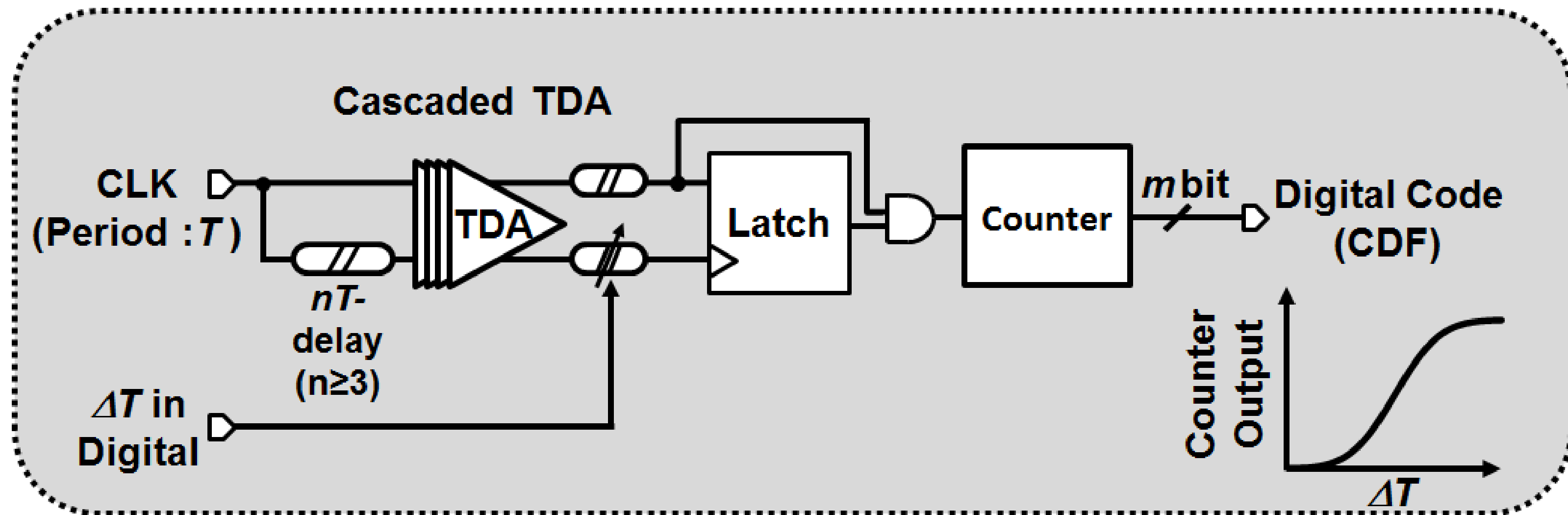
Flash-type TDC with analog FPGA

Flash-type TDC with digital FPGA

[2] R. Jiang, H. Kobayashi, Y. Ozawa, R. Shiota, K. Hatayama, et. al.,
"Successive Approximation Time-to-Digital Converter with Vernier-level Resolution",
IEEE International Mixed-Signal Testing Workshop, Catalunya, Spain (July 4-6, 2016).

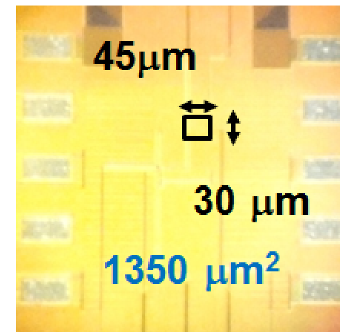
On-chip Jitter Measurement Circuit

BIST solution



Experiments show that 1.67 ps RMS timing jitter can be measured

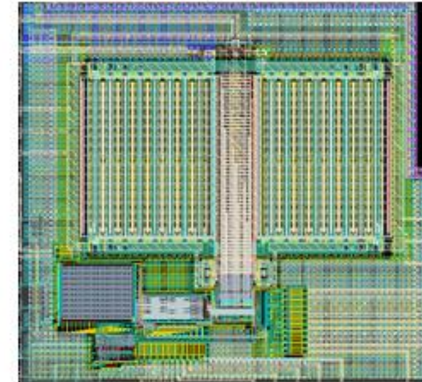
Process : 65 nm CMOS
Supply Voltage : 1.2 V



[3] K. Niitsu, H. Kobayashi , "CMOS Circuits to Measure Timing Jitter Using a Self-Referenced Clock and a Cascaded Time Difference Amplifier with Duty-Cycle Compensation," IEEE Journal of Solid-State Circuits, Nov. 2012.

DFT for SAR ADC Linearity

BIST Solution



A high-resolution, low-sampling-rate ADC requires a long testing time for its linearity.

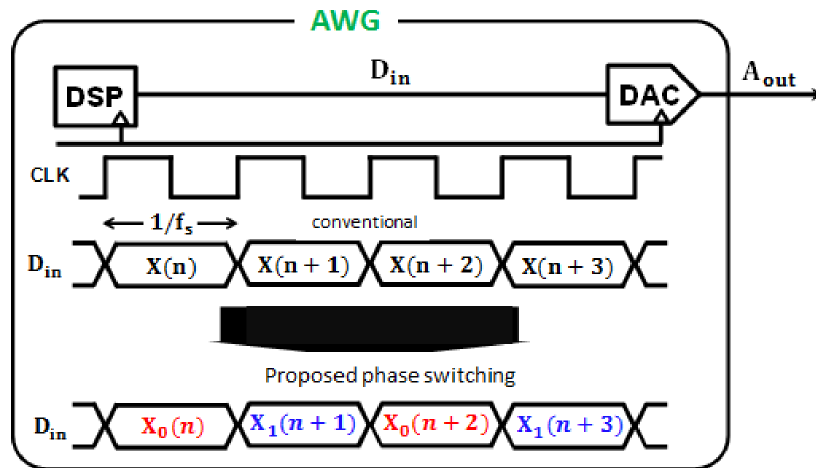
10bit SAR ADC
TSMC 180nm
$1.2 \times 1.2\text{mm}^2$

Shorten SAR ADC linearity test time.

[4] T. Ogawa, H. Kobayashi,
"Design for Testability That Reduces Linearity Testing Time of SAR ADCs",
IEICE Trans. on Electronics (June 2011).

Low Cost ATE

Low IMD3 2-Tone Signal Generation with AWG for Communication Application ADC Testing



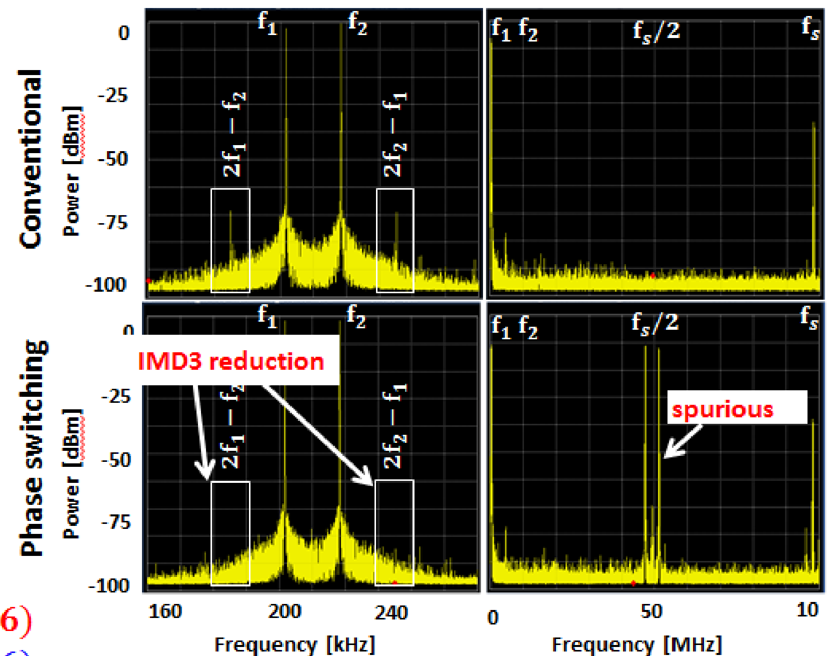
Conventional

$$X(n) = A\cos(2\pi f_1 nT_s) + A\cos(2\pi f_2 nT_s)$$

Proposed phase switching

$$X_0(n) = B\cos(2\pi f_1 nT_s + \pi/6) + B\cos(2\pi f_2 nT_s - \pi/6)$$

$$X_1(n) = B\cos(2\pi f_1 nT_s - \pi/6) + B\cos(2\pi f_2 nT_s + \pi/6)$$



[5] K. Kato, H. Kobayashi,
"Two-Tone Signal Generation for Communication Application ADC Testing",
The 21st IEEE Asian Test Symposium, Niigata, Japan (Nov. 2012).

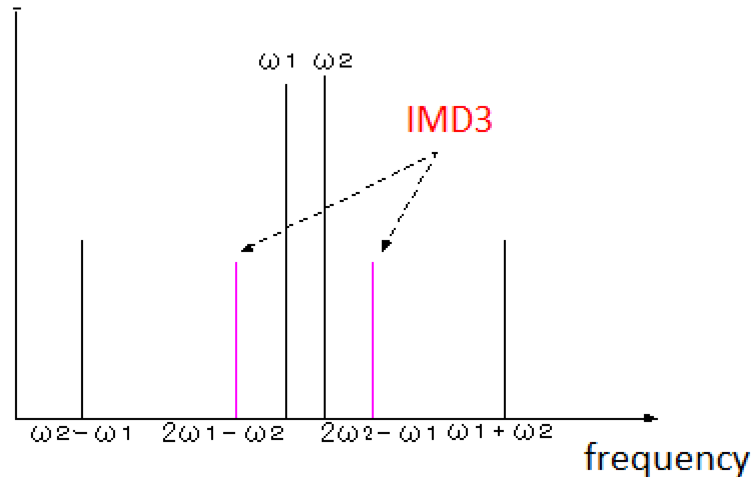
Algorithm

Multi-tone Curve Fitting Algorithm for Communication Application ADC

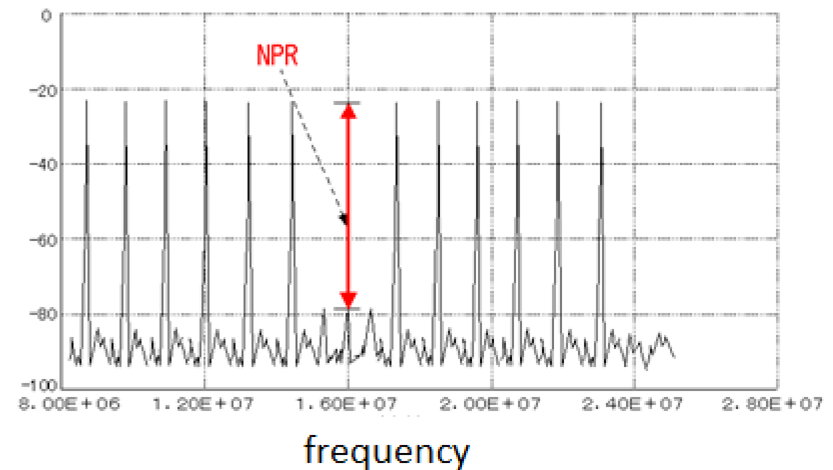
2-tone

Multi-tone

Power spectrum



Power spectrum



No need for expensive instruments

Noise Power Ratio: NPR

ADSL application ADC testing

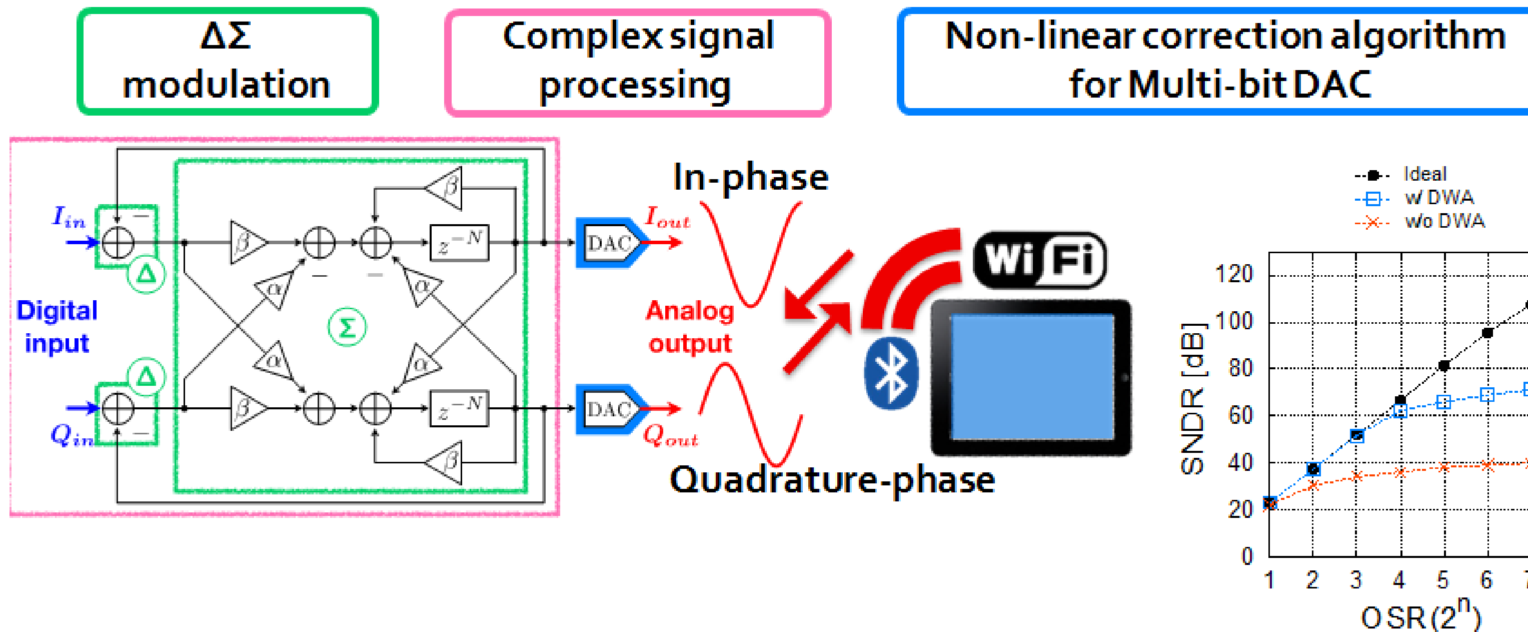
[6] Y. Motoki, H. Kobayashi,
``Multi-Tone Curve Fitting Algorithms for Communication Application ADC Testing'',
Electronics and Communication in Japan: Part 2, Wiley Periodicals Inc. (2003).

Complex Multi-Bandpass ΔΣ Modulator for I-Q Signal Generation

ATE for Mixed-Signal Testing

- Generation of high quality analog I-Q signals
- Testing of communication application ICs
- Digital rich

(Suitable to the realization with nano CMOS → Low cost)



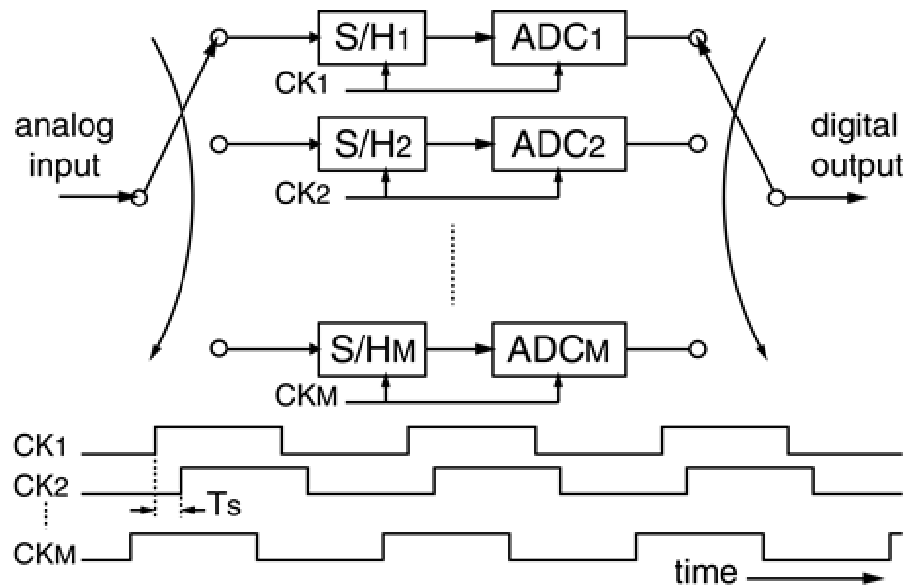
[7] M. Murakami, H. Kobayashi, " I-Q Signal Generation Techniques for Communication IC Testing and ATE Systems", IEEE International Test Conference, (Nov. 2016).

Time Interleaved ADC in ATE System

ATE for Mixed-Signal Testing

Channel ADC mismatch compensation

Cost effective high-speed ADC



[8] N. Kurosawa, H. Kobayashi,
``Explicit Analysis of Channel Mismatch Effects in Time-Interleaved ADC Systems",
IEEE Trans. on Circuits and Systems I (March 2001).

[9] R. Yi, H. Kobayashi,
Digital Compensation for Timing Mismatches in Interleaved ADCs",
IEEE 22nd Asian Test Symposium, Yilan, Taiwan, (Nov. 2013)

[10] K. Asami, H. Kobayashi, "Timing Skew Compensation Technique using Digital Filter with Novel Linear Phase Condition,"
IEEE International Test Conference, Austin (Nov. 2010).

4. Challenges & Conclusion

Challenges of Analog Testing

- Use all aspects of technologies
  - Circuit technique
  - Cooperation among BIST, BOST & ATE
    as well as software & network
  - Signal processing algorithm
  - Use resources in SOC
    such as µP core, memory, ADC/DAC

There is no science without measurement.

There is no production without test

No royal road to analog testing