Self-Calibration and Trigger Circuit for Two-Step SAR TDC

Takashi Ida, Yuki Ozawa, Jiang Richen, Haruo Kobayashi, Ryoji Shiota

School of Science and Technology, Gunma University

Introduction

Time-to-Digital Converter (TDC) measures the time and provides digital output

- Can it be measured more accurately?
- How can we generate repetitive signals of clk 1 and clk 2 with one shot?

Research Background

Development of highly-linear, fine-time-resolution TDC for high-speed digital I/O interface timing measurement

Research Objective

Development of 2 key technologies for time measurement

Our Innovation

[ I ] Two-Step SAR TDC

- Fine time resolution

[ II ] Self-Calibration

- Linear TDC

[ III ] Trigger Circuit

- One-shot timing measurement

Fine time resolution

[ I ] TDC operation

Two-Step SAR TDC operation (SAR TDC + Vernier type TDC)

OP.1: Using 4 buffer → 1
OP.2: Using 6 buffer → 0
OP.3: Using 5 buffer → 0

Digital output: 100

CLK1
CLK2
ΔT = 4.3τ

CLK1
CLK2

[ II ] Calibration algorithm

Explanation of the self-calibration algorithm

- Estimate the delay value of the actual delay element by increasing the number of samples

Linear TDC

[ I ] TDC operation

3bit SAR + 3bit SAR-Vernier TDC

Digital output: 100

CLK1
CLK2

ΔT = 4.3τ

CLK1
CLK2

[ II ] Calibration algorithm

Explanation of the self-calibration algorithm

- Estimate the delay value of the actual delay element by increasing the number of samples

Linear TDC

One-shot timing measurement

[ III ] Self-configuring circuit using trigger circuit

Measurement error of estimated value [τ1]

- When the number of samples is "2"
  - About 3.7%

- When the number of samples is "100"
  - About 1.2%

Measurement error of estimated value [τ2]

- When the number of samples is "2"
  - About 19.5%

- When the number of samples is "100"
  - About 9.0%

Error variation with respect to τ1 (=1.0)

36% → 3%

Error variation with respect to τ2 (=0.1)

320% → 20%

Sufficient reliability!

References

