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Self-Calibration and Trigger Circuit for Two-Step SAR TDC

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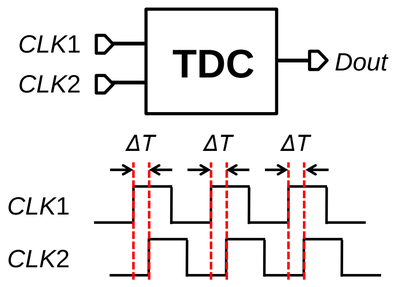
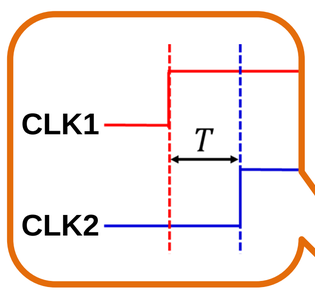
Introduction

Research Background

Time-to-Digital Converter (TDC)
measures the time and provides digital output





- Can it be measured **more accurately**?
- How can we generate **repetitive signals** of clk 1 and clk 2 with **one shot**?

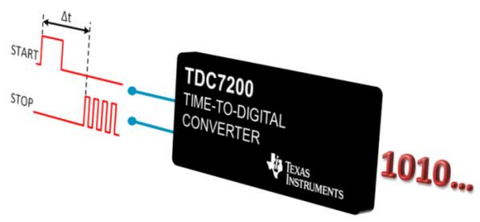
Research Objective

Development of

highly - linear, fine time-resolution TDC

for high-speed digital I/O interface

timing measurement



Our Innovation

Development of 2 key technologies

for time measurement

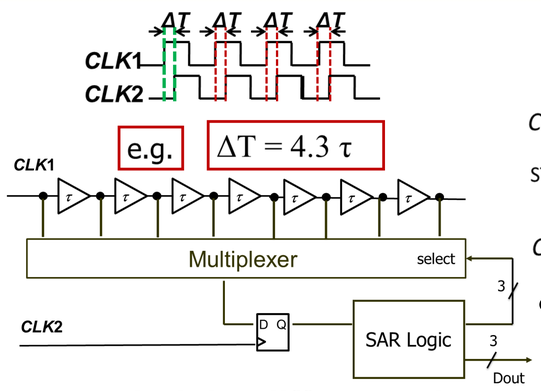
[Ⅰ] Two-Step SAR TDC
➡ Fine time resolution

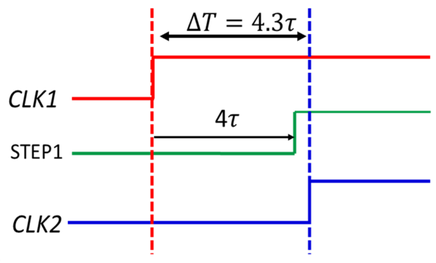
[Ⅱ] Self-Calibration
➡ Linear TDC

[Ⅲ] Trigger Circuit
➡ One-shot timing measurement

Fine time resolution

[Ⅰ] TDC operation





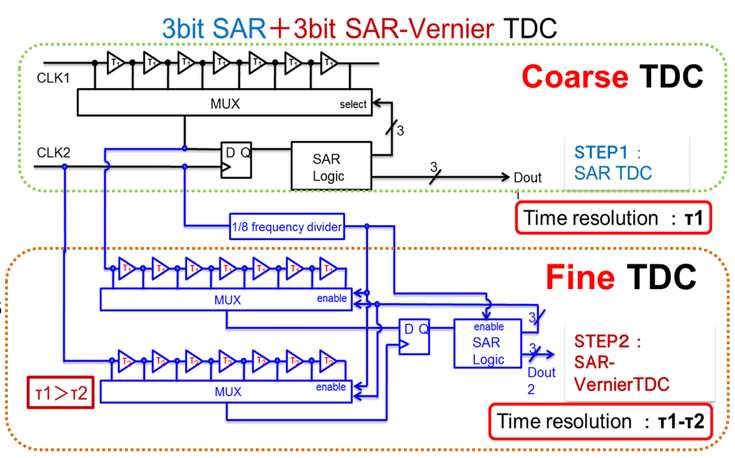
◉ **Buffer increase / decrease is based on binary search**

◉ **Find the difference between clk 1 and clk 2 by using buffer to delay the clock**

OP.1:Using 4 buffer → 1
OP.2:Using 6 buffer → 0
OP.3:Using 5 buffer → 0

➡ **Digital output 100** ➡ 4τ

Two-Step SAR TDC operation (SAR TDC+Vernier type TDC)

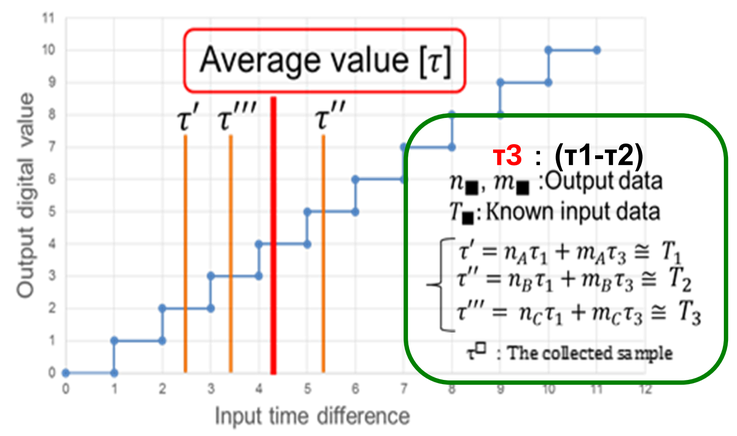


OP.1:Using Coarse TDC(Time resolution τ1)
OP.2:Using 1/8 frequency divider
OP.3:Using Fine TDC(Time resolution τ1-τ2)

Linear TDC

[Ⅱ] Calibration algorithm

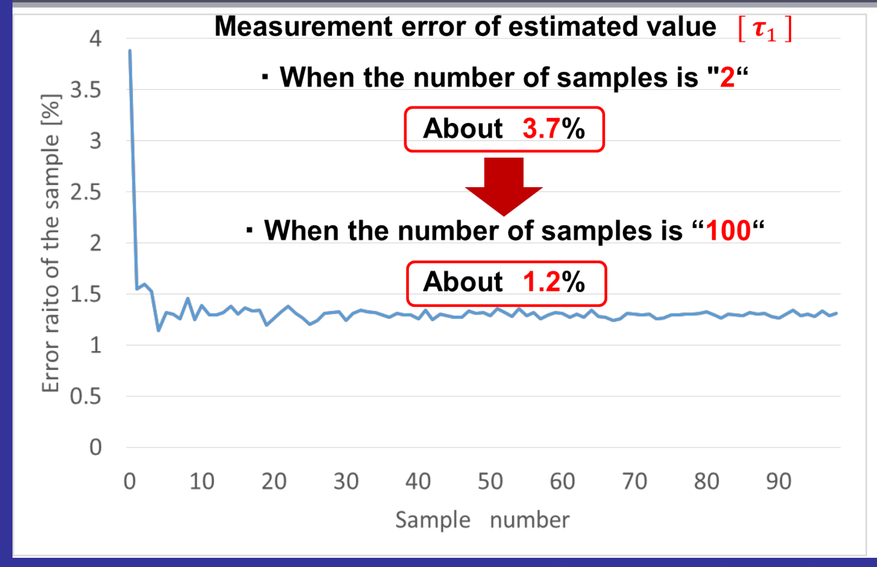
Explanation of the self-calibration algorithm

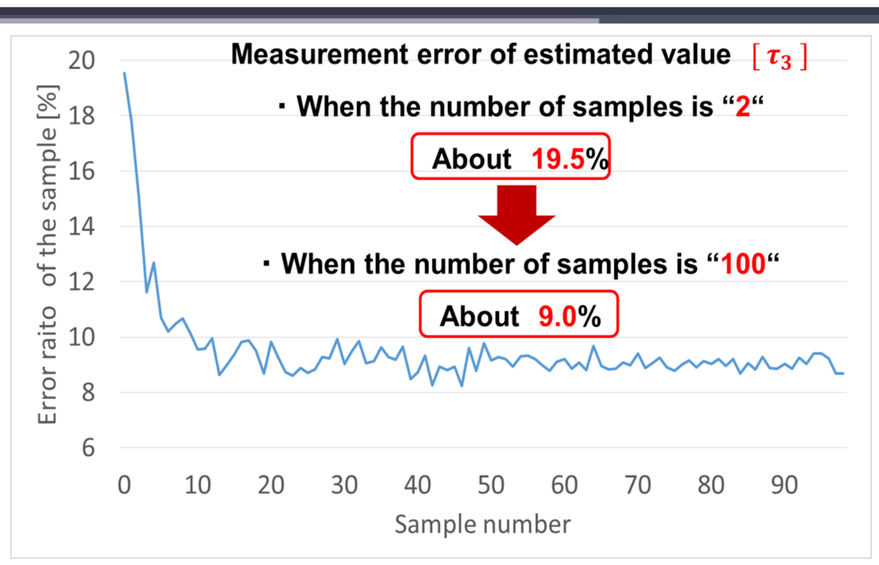


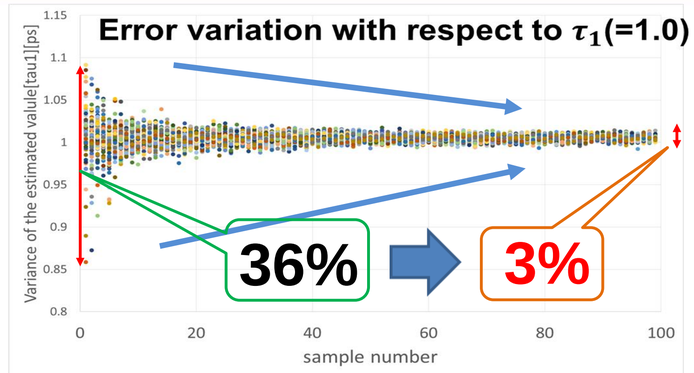
- Estimate the delay value of the actual delay element by increasing the number of samples

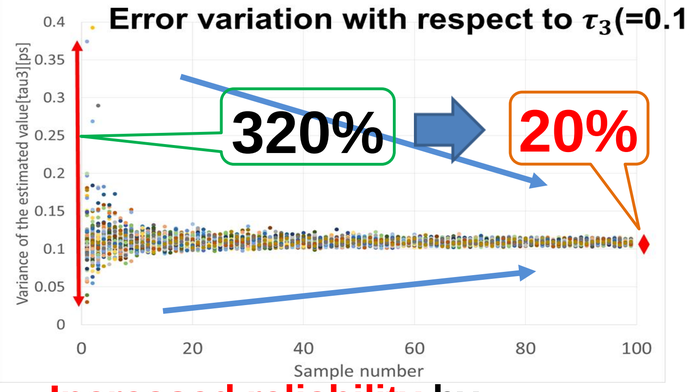
Linear TDC

Simulation Result : Measurement error of estimated value







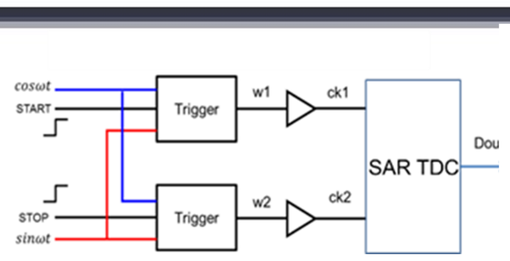


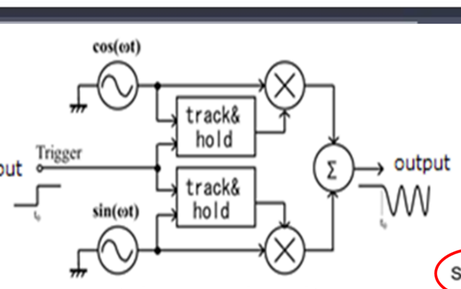
- **Increased reliability by increasing the number of samples**

Sufficient reliability!

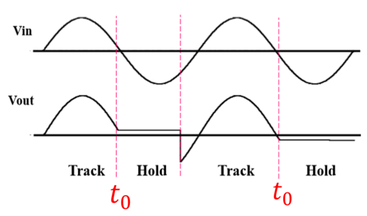
One-shot timing measurement

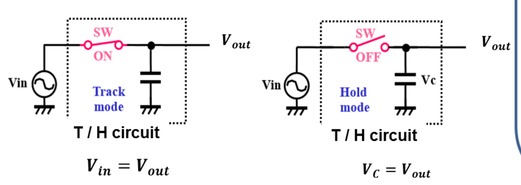
[Ⅲ] Self-configuring circuit using trigger circuit



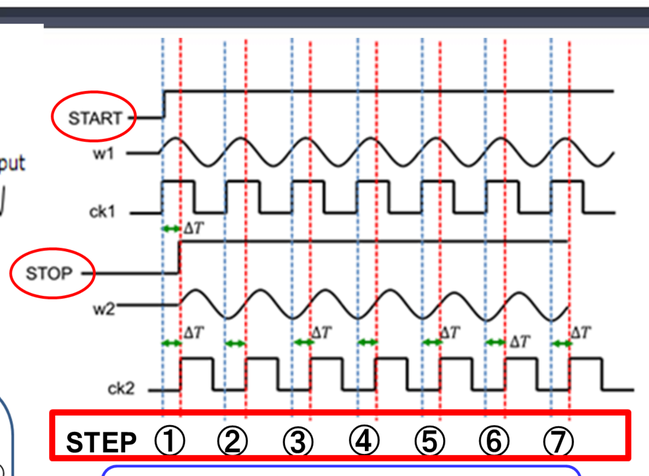


trigger circuit





track-and-hold
▪**track mode**
Vout=cos(ωt)cos(ωt)+cos(ωt+π/2) cos(ωt+π/2)
=cos²(ωt)+sin²(ωt)
=1 （一定の値）
▪**hold mode**
Vout= cos(ωt) cos(ωt_0) +sin(ωt)sin(ωt_0)
=cos(ω(t−t_0))
※ **trigger time:t_0**



Multiple STEPs are required for TDC self-calibration

Repetitive time difference signal is generated by one shot of START signal and STOP signal

References

[1] Y. Arai, T. Baba, “A CMOS Time to Digital Converter VLSI for High-Energy Physics”, IEEE Symposium on VLSI Circuits (1988).

[2] R. Jiang, C. Li, M. Yang, H. Kobayashi, et al., "Successive Approximation Time-to-Digital Converter with Vernier-level Resolution", IEEE IMSTW, Catalunya, Spain（July 2016).

[3] Tektronics, Automatic RF Techniques Group 56th Measurement Conference - Metrology and Test for RF Telecommunications, Boulder, Colorado (Dec. 2000).