ATS

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SAR TDC Architecture with Self-Calibration Employing Trigger Circuit

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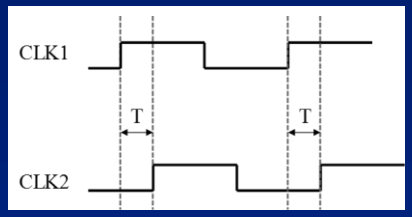
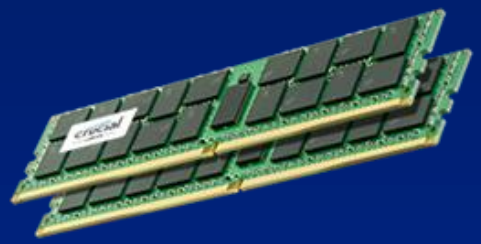
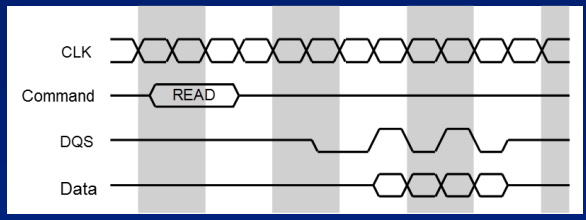
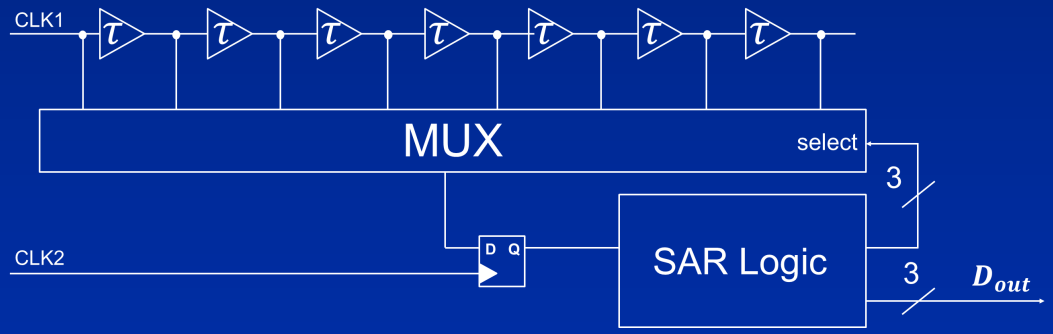
Research Target







High-speed I/O interface signal timing testing



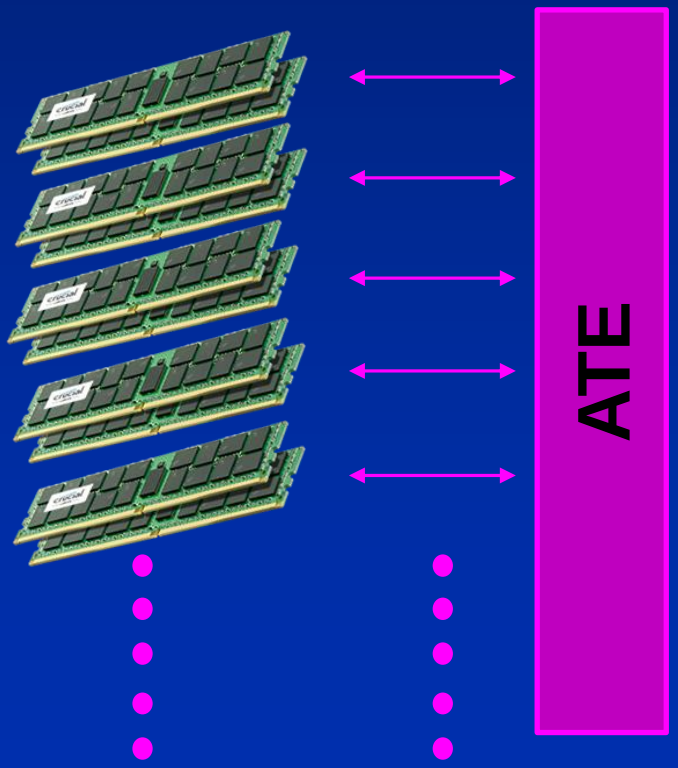
SAR TDC

- ✓ **Small circuit**
- ✓ **Full digital**
- ✓ **High linearity**
- ✓ **High resolution**

Suitable for low cost BOST

Application

Multi channels



Large circuit × Large amounts

High test cost

Small circuit × Large amounts

Low test cost

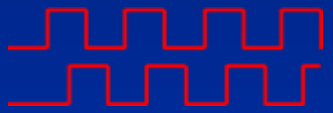
Innovation

✓ **Trigger Circuit**

One-shot timing measurement

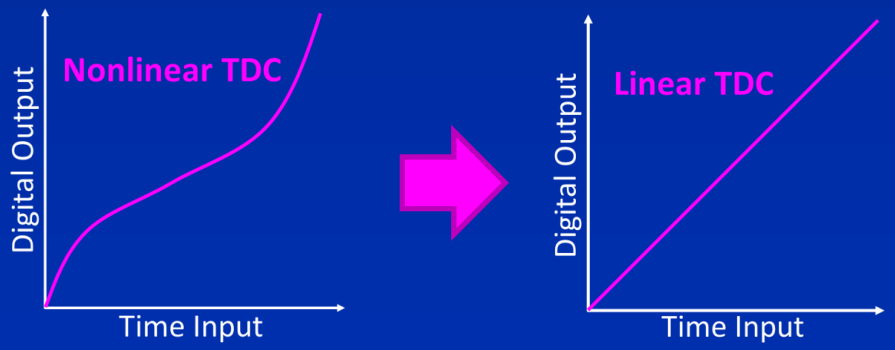
&

Short testing time for low frequency repetitive timing



✓ **Self Calibration**

Linear TDC



Outline

- Research Objective
- TDC Application to LSI Testing Technology
- SAR TDC Architecture & Operation
- SAR TDC with Self Calibration

  -Relative variation

  -Absolute variation
- SAR TDC Employing Trigger Circuit
- Summary

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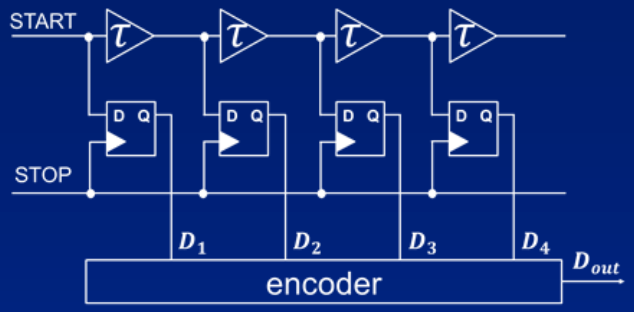
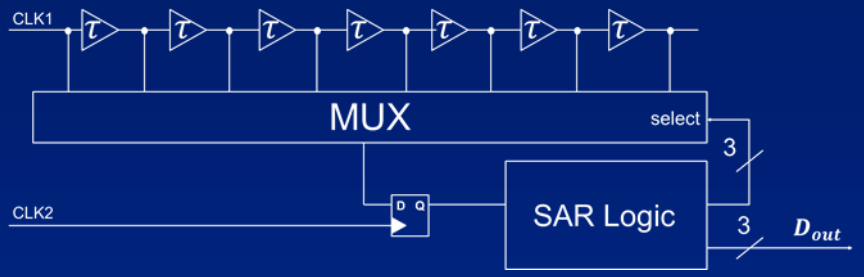
Research Objective

- To develop time-to-digital circuit with small size, low power, fine time resolution & one-shot timing signal measurement capability

Approach(1)



Flash TDC



SAR TDC

Huge (Costly)

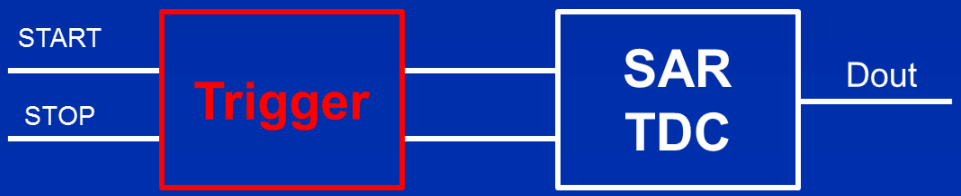
Circuit Scale

Small

One Shot

Timing Signal

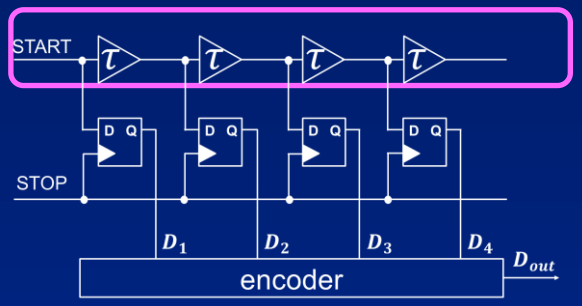
Repetitive



One Shot

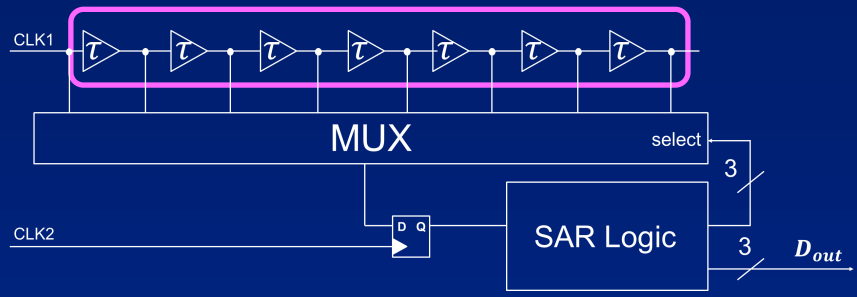
Enable to measure one shot timing with SAR TDC

Approach(2)

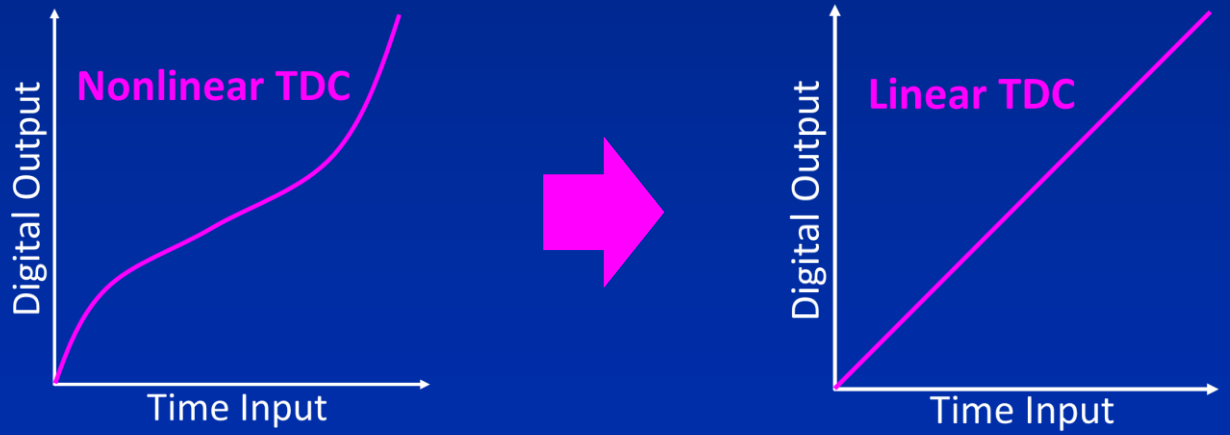


Flash TDC

Variation



SAR TDC



Fine time resolution & high linearity timing measurement with full digital self-calibration method

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  -Relative variation

  -Absolute variation

- SAR TDC Employing Trigger Circuit
- Conclusion

ATE System & TDC

- **“Timing” is very important in ATE systems**
- **Many high-performance TDCs are used there.**

Such as

for clock timing, jitter measurements

[1] K. Yamamoto,at. el. (Advantest Corp.),
“Multi Strobe Circuit for 2.133 GHz Memory Test System,”
IEEE International Test Conference, Paper 6.1 (2006).

Analog/Mixed-Signal BIST, BOST

- **TDC can be used for BIST, BOST**
- **BIST, DFT**

Chip design time become longer — **Long time-to-market**

Chip become larger — **Costly**

Difficult to assure its reliability — **Should be simple**

- **BOST**

Design / implementation after tape out attractive

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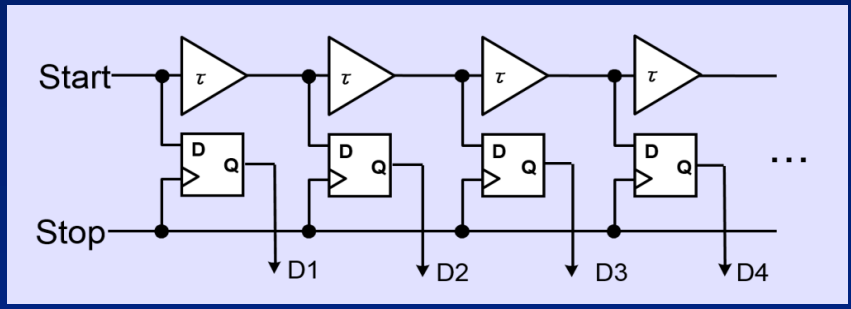
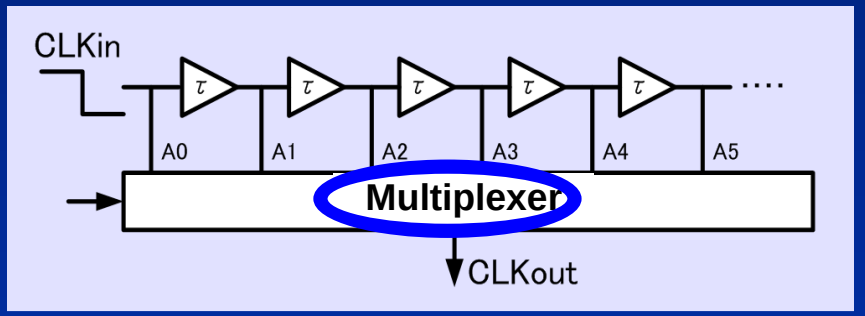
SAR TDC Architecture

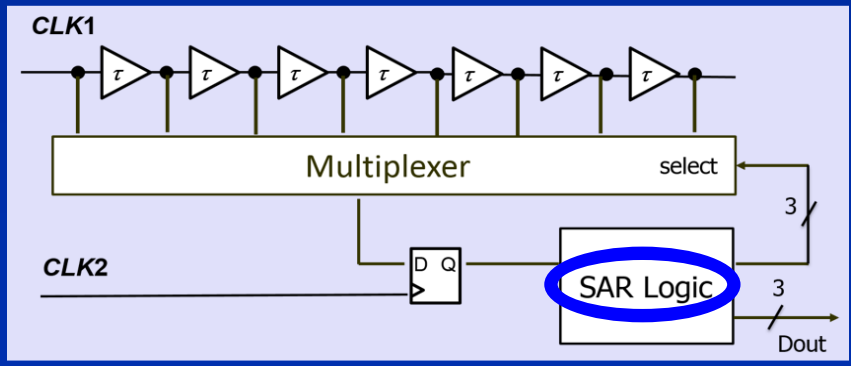
D-FFs can be greatly reduced by using MUX

Circuit operation loop can be made with successive approximation



Flash TDC





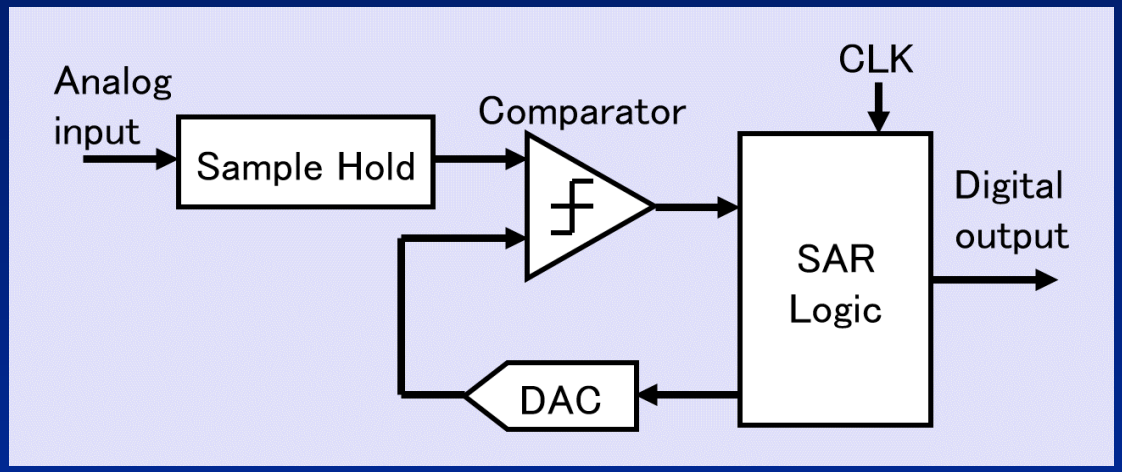
SAR TDC

SAR : Successive Approximation Register

SAR-ADC VS. SAR-TDC

SAR ADC :

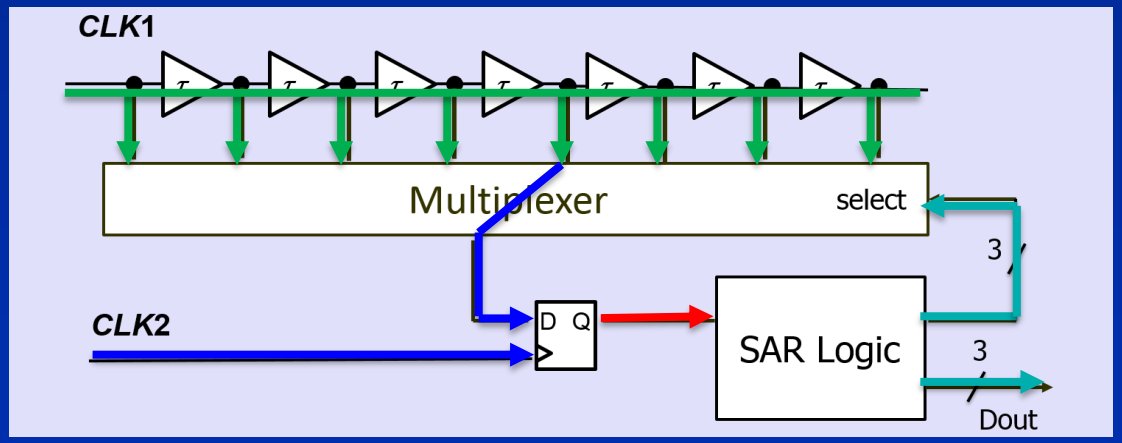
- **Comparator**
- **DAC**



SAR-ADC

SAR TDC :

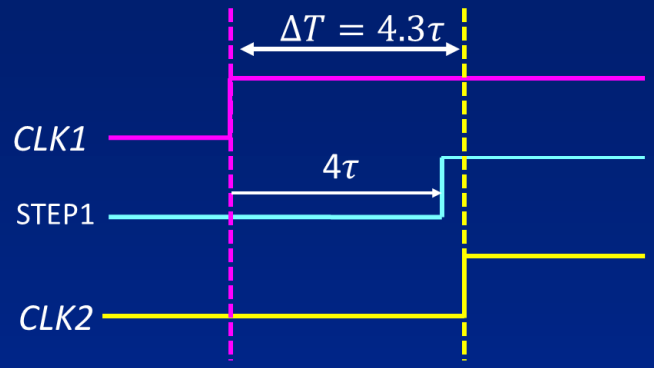
- **D-FF**
- **Delay line**

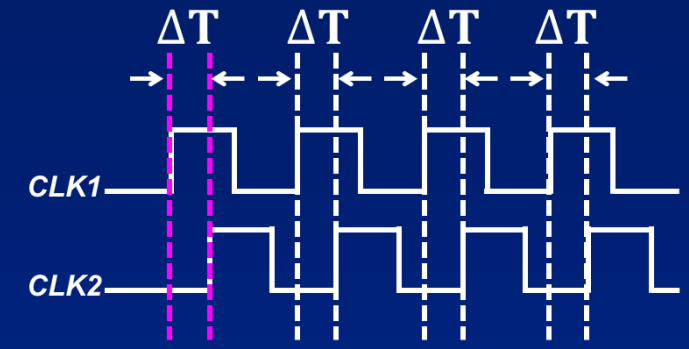


SAR-TDC

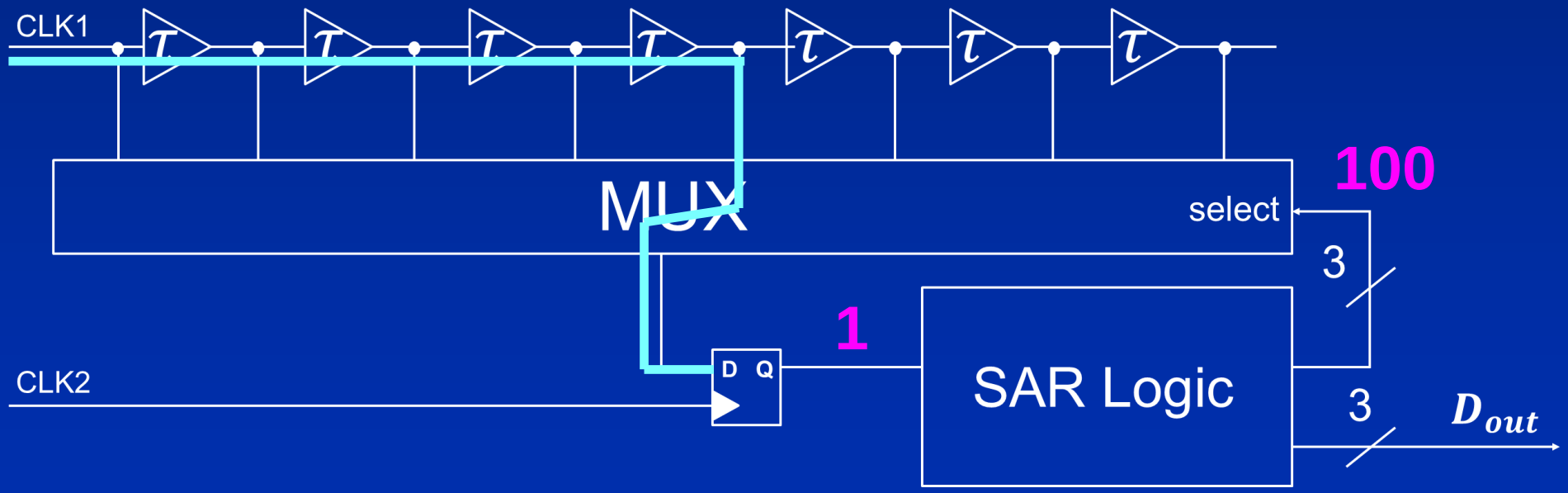
SAR TDC Operation

STEP1



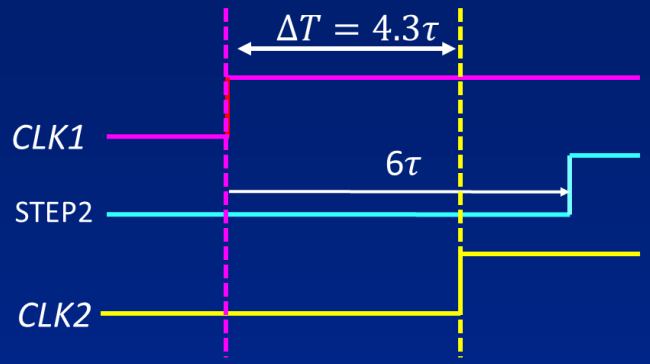


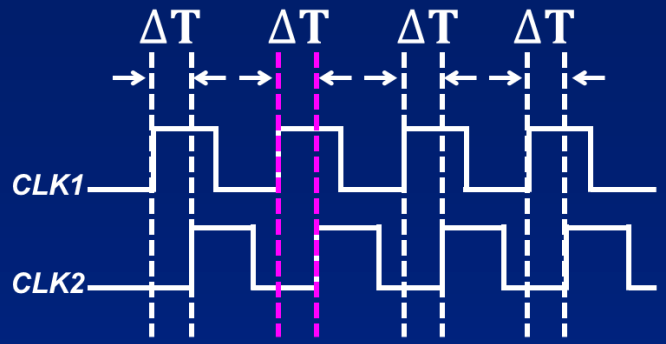
Example $\Delta T = 4.3\ \tau$



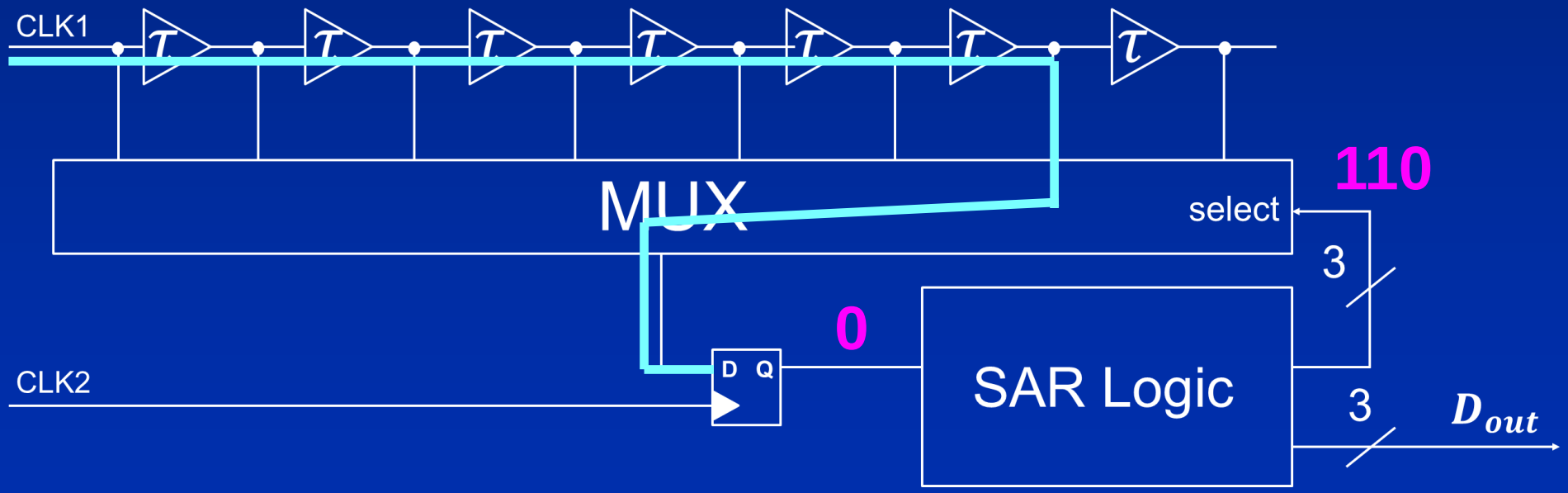
SAR TDC Operation

STEP2



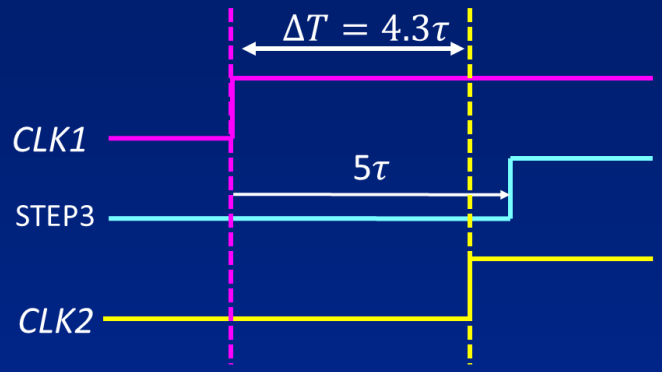


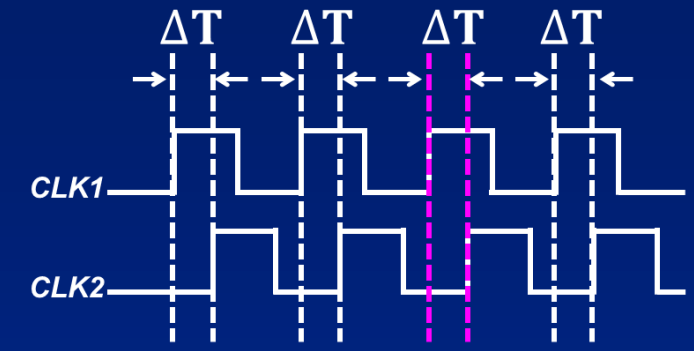
Example $\Delta T = 4.3\ \tau$



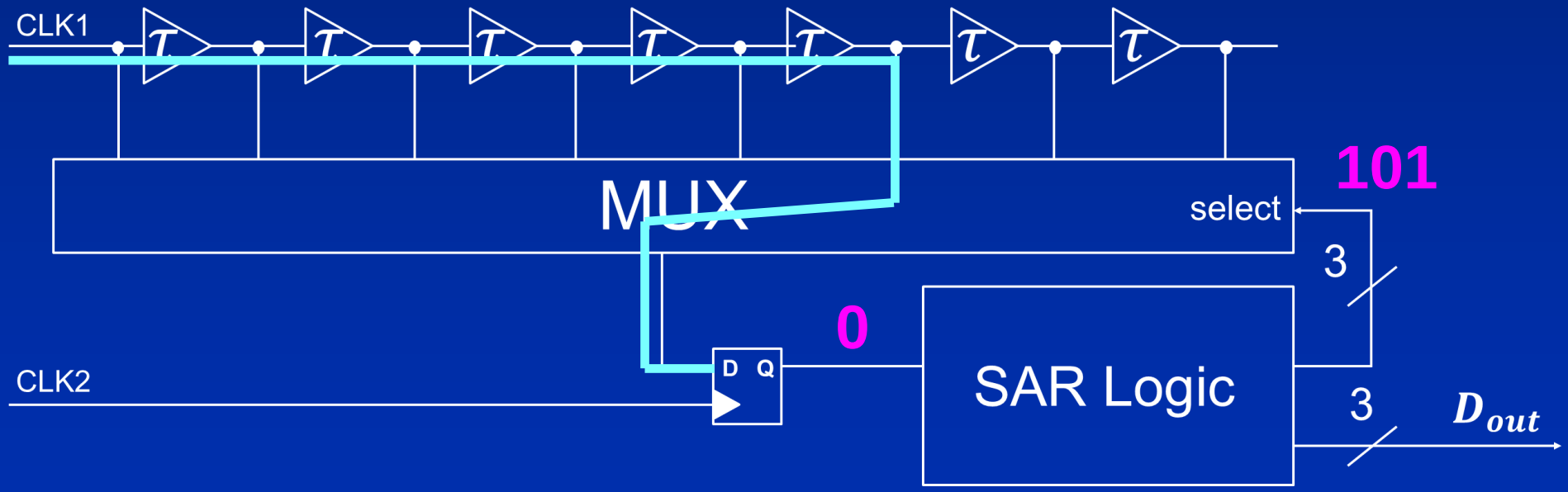
SAR TDC Operation

STEP3



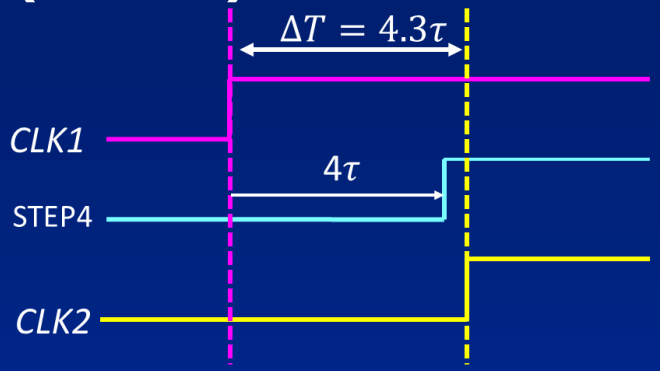


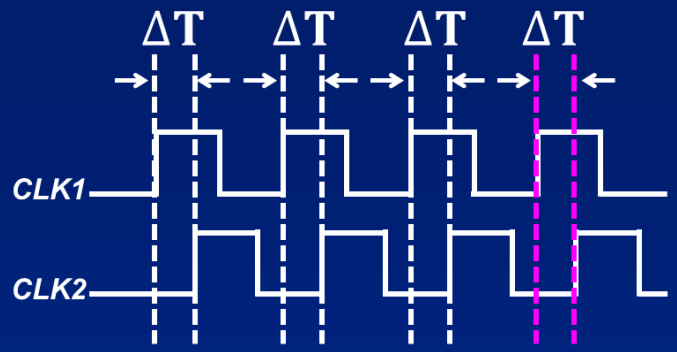
Example $\Delta T = 4.3\ \tau$



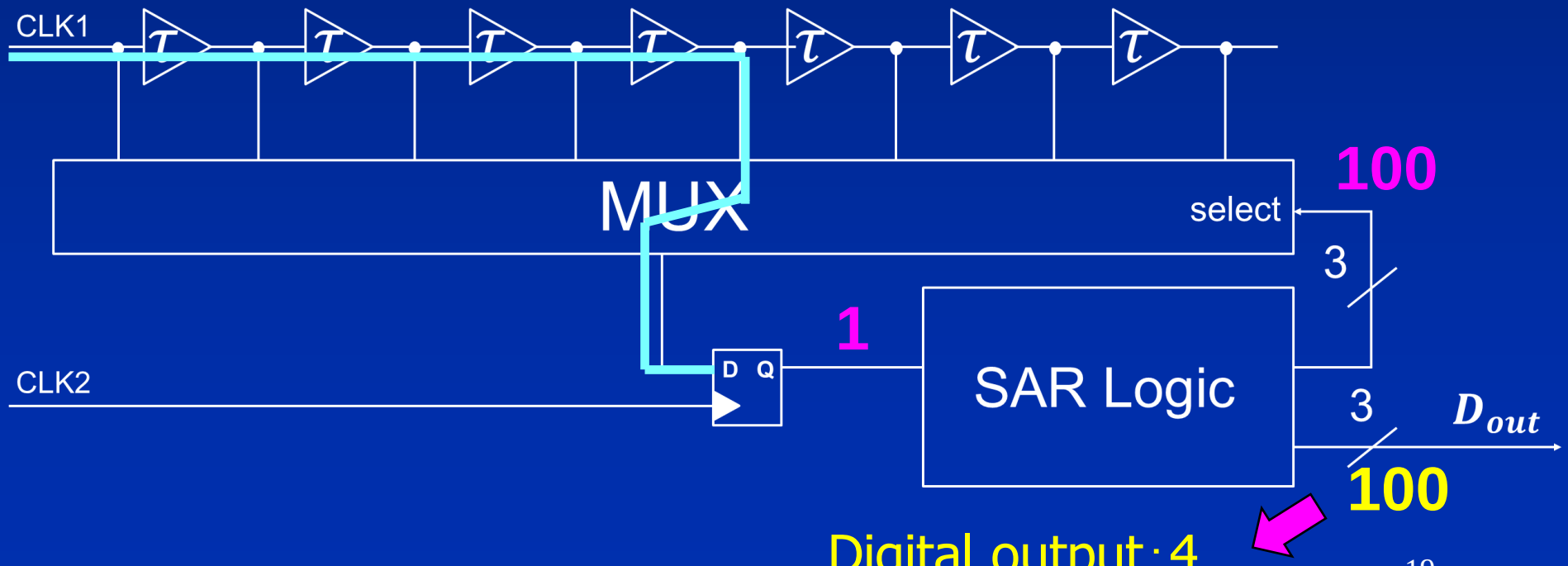
SAR TDC Operation

STEP4 (Stable)





Example $\Delta T = 4.3\ \tau$



Digital output : 4

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Random Variation among Delay Cells

Delay τ variation

Relative variation

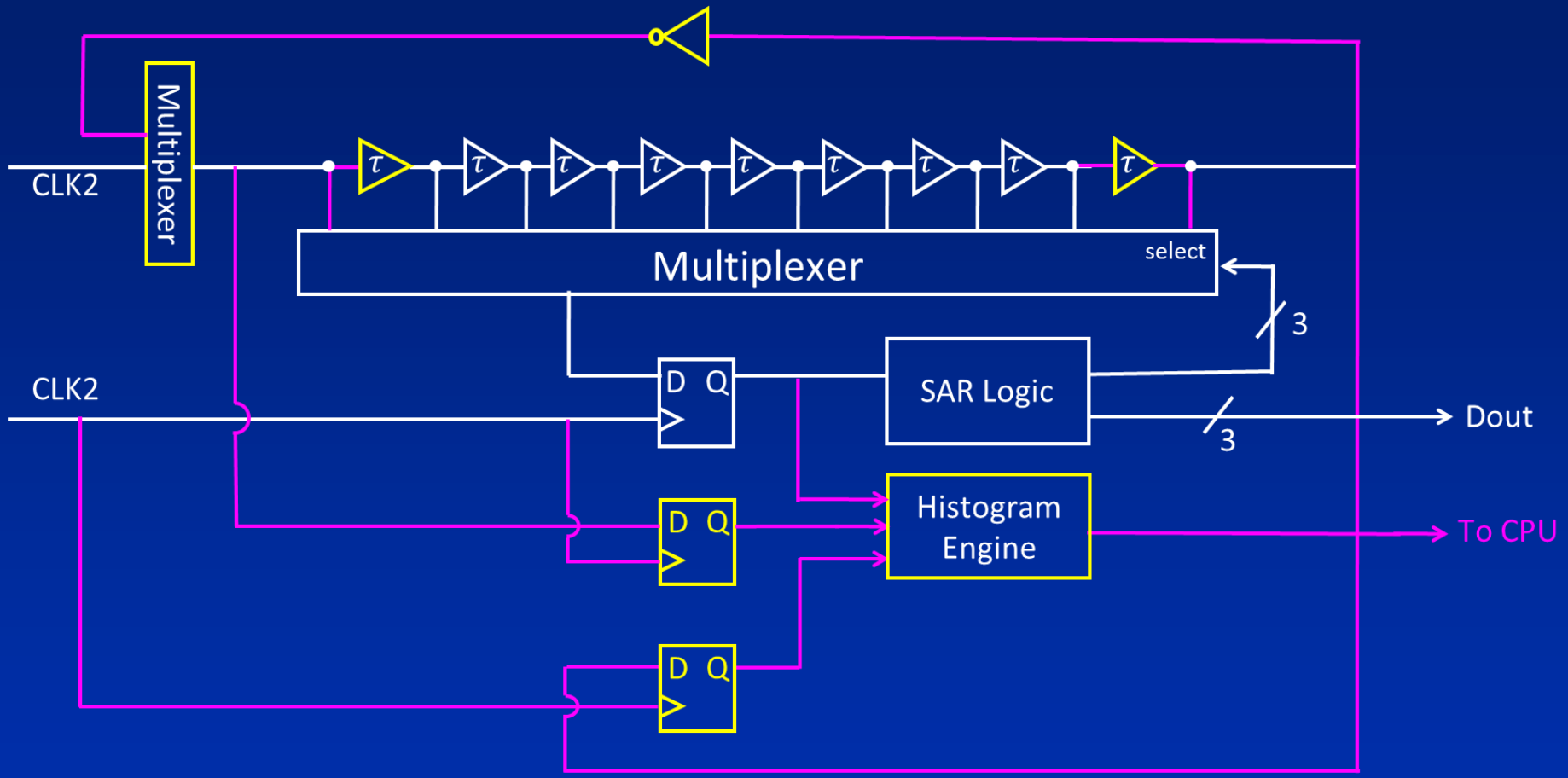
➡ TDC nonlinearity

Absolute（average value) variation

➡ TDC input range & time resolution

SAR TDC with Self-Calibration

Relative variation

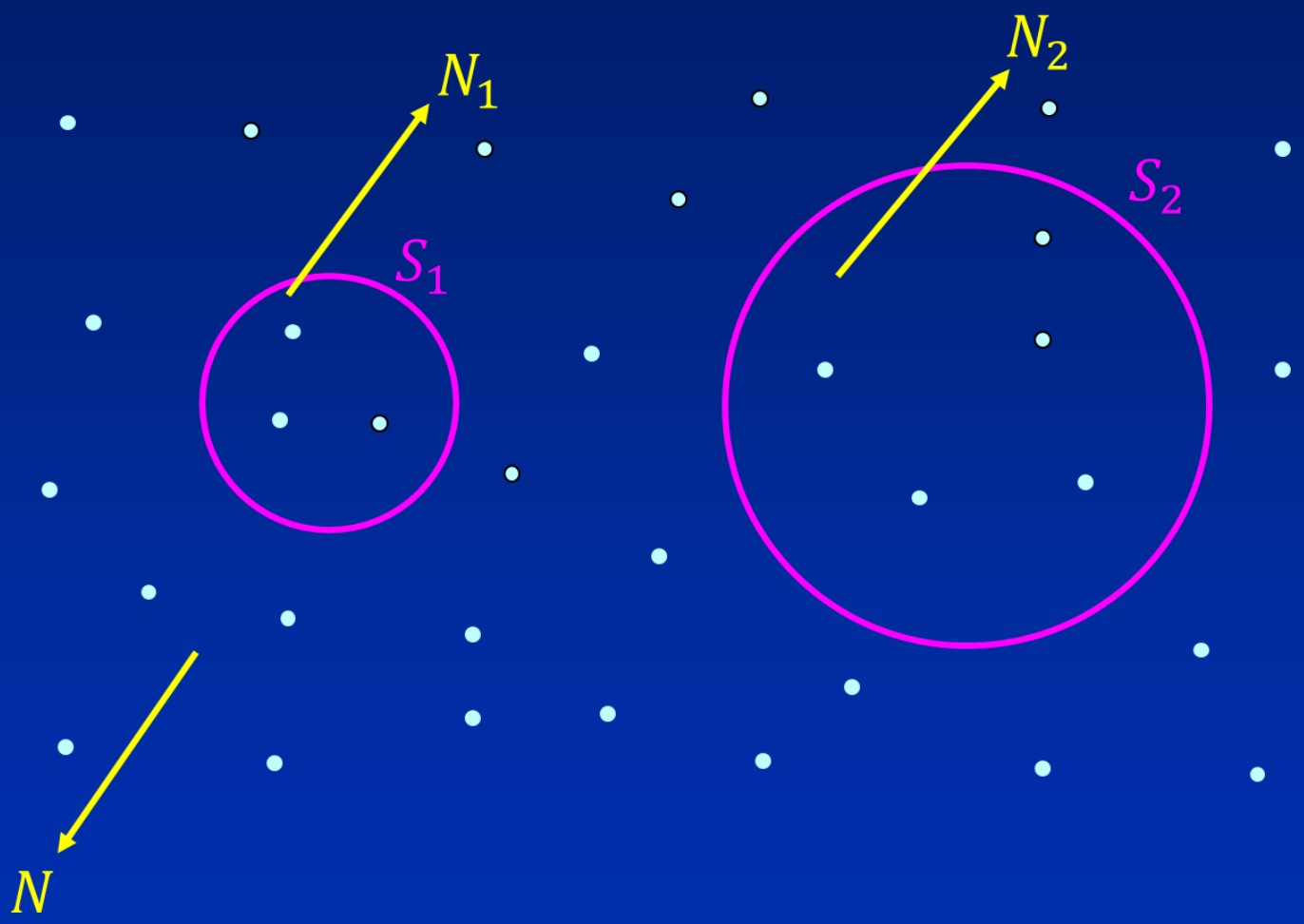


Addition of calibration circuit, interconnection

Measurement with Histogram

Relative variation

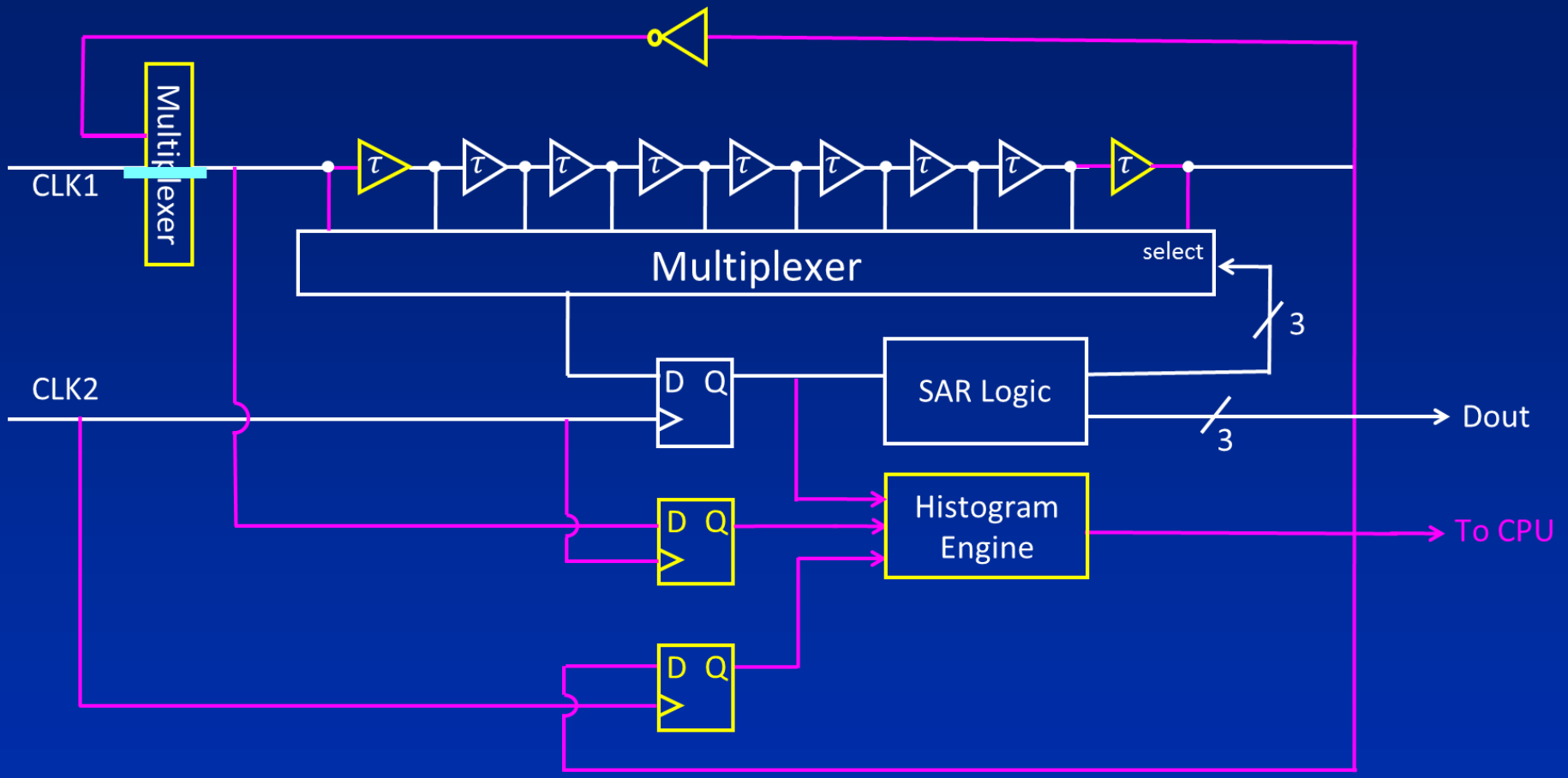
Random dots (Monte Carlo method)



# of dots ratio $\frac{N1}{N2}$ ⇒ **Area ratio** $\frac{S1}{S2}$

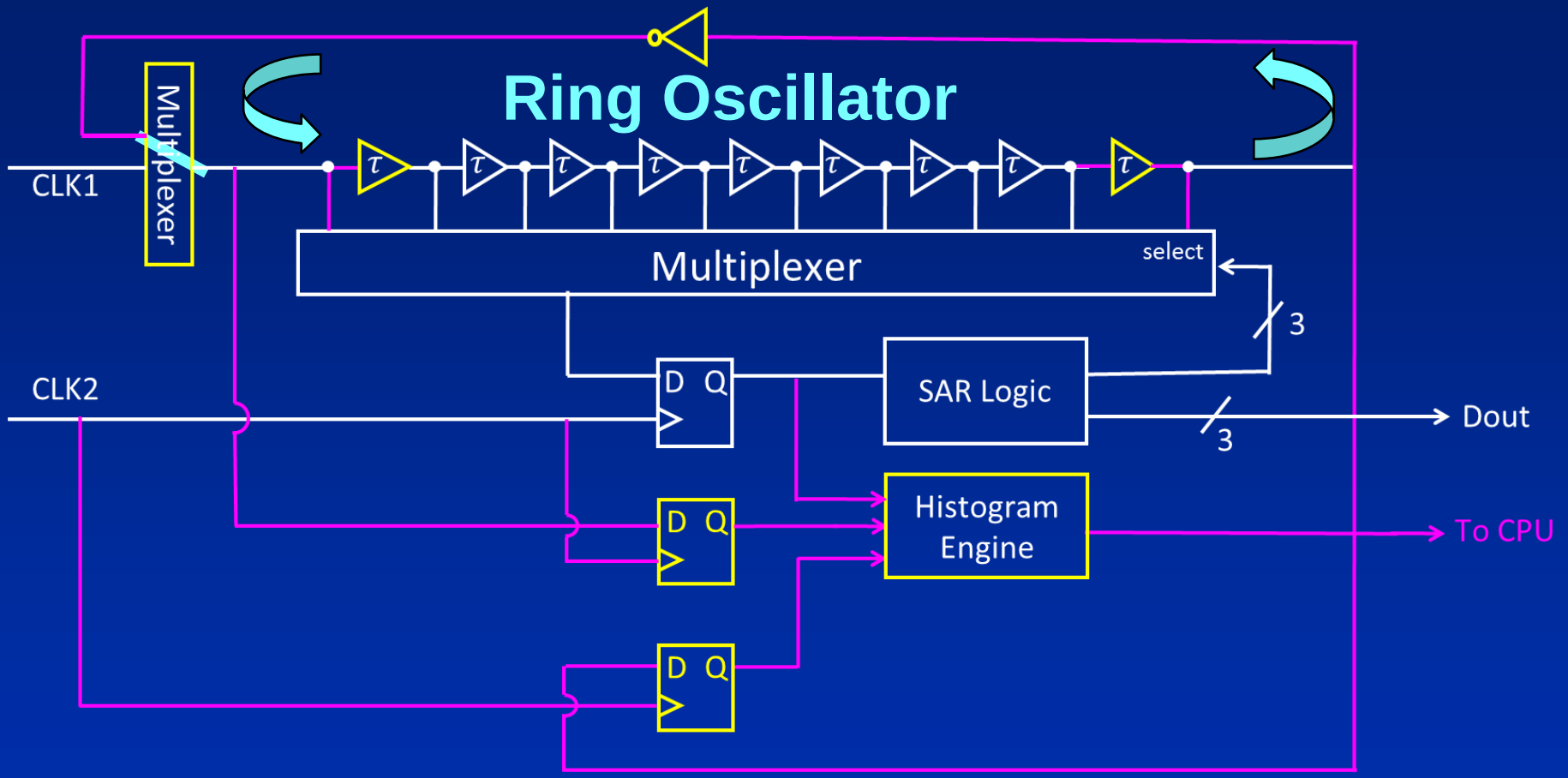
Normal Operation Mode

Relative variation



Calibration Mode

Relative variation



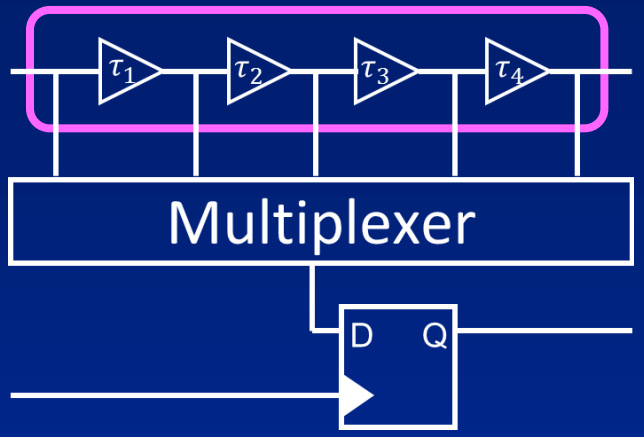
CLK1, CLK2 are NOT correlated. ⟺ **Random dots**

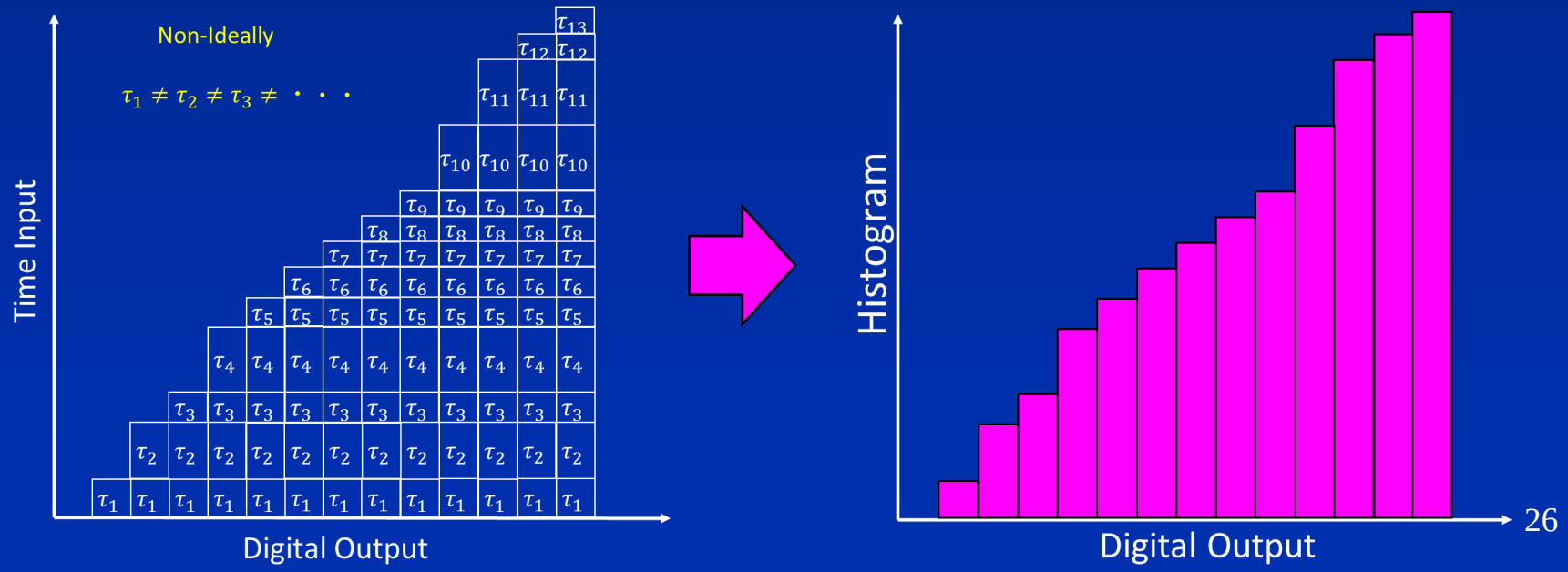
Measurement of Delay Values

Relative variation

Histogram method
(Monte Carlo method)

Delay values can be estimated

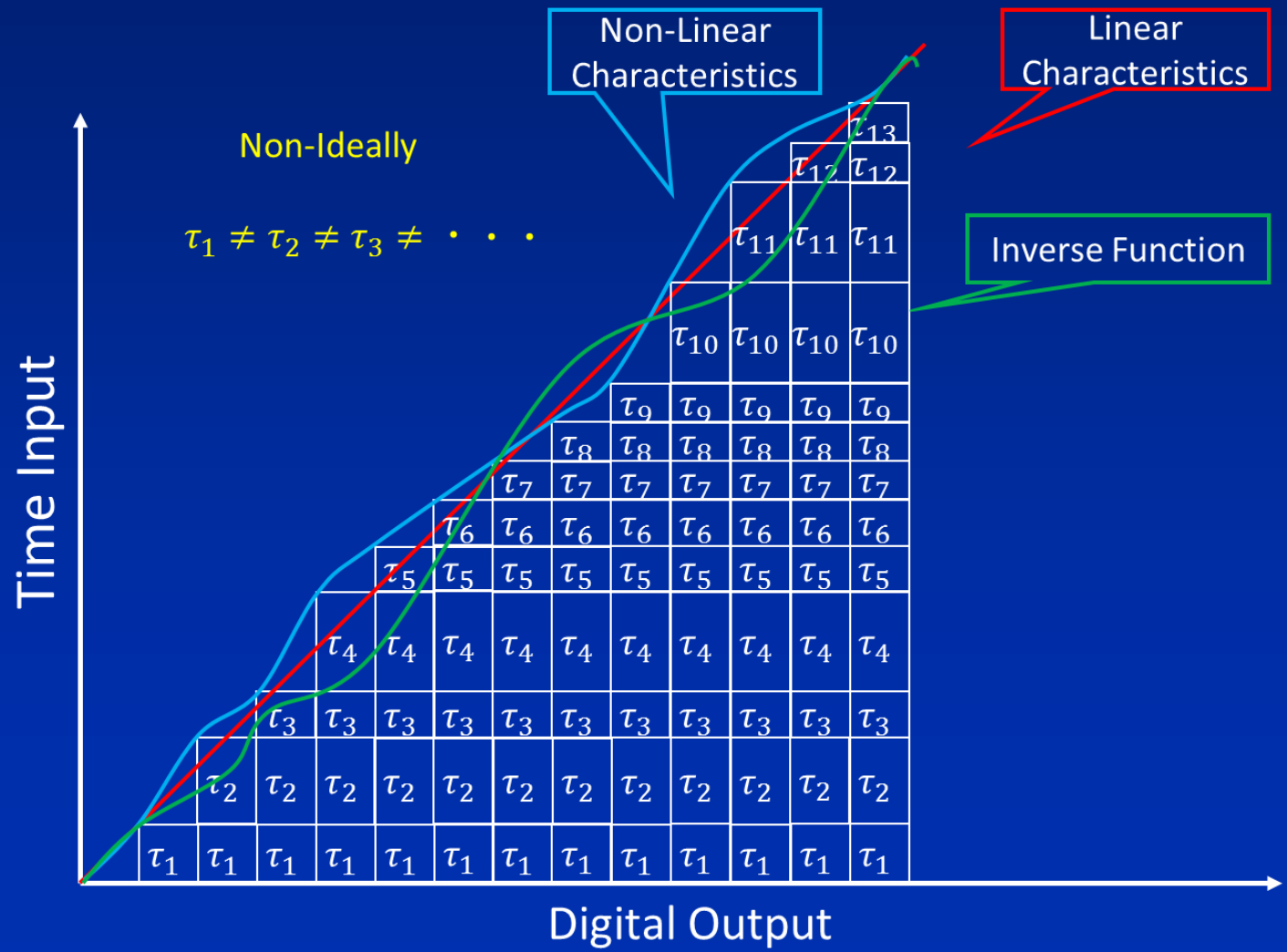




Digital Correction of TDC Nonlinearity

Relative variation

- Correction with inverse transfer function



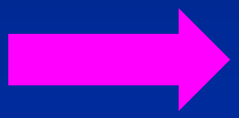
Digital Error Correction

Relative variation

- TDC linearity self-calibration with histogram

Dout(0)=1
Dout(1)=3
Dout(2)=5
Dout(3)=8
.
.

Calibration



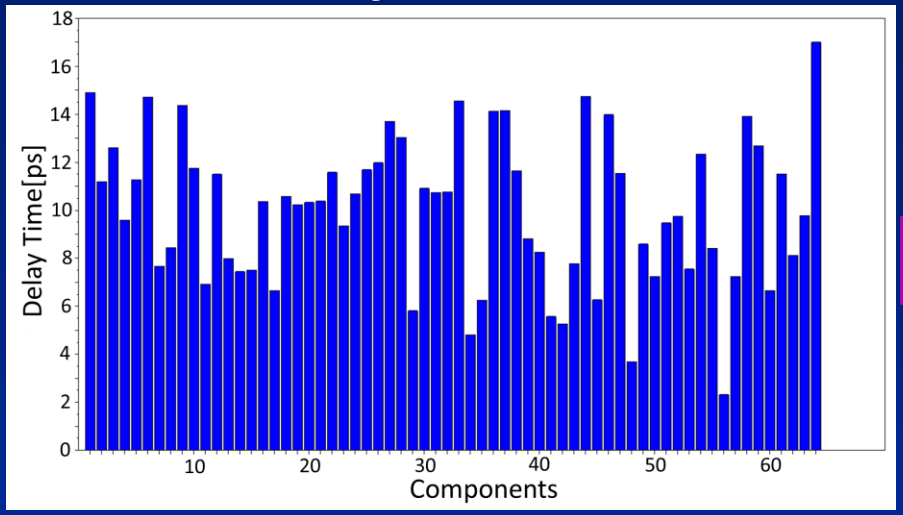
Dout(0)=0.3
Dout(1)=2.8
Dout(2)=4.5
Dout(3)=7.3
.
.

Corrected based on delay variation estimation

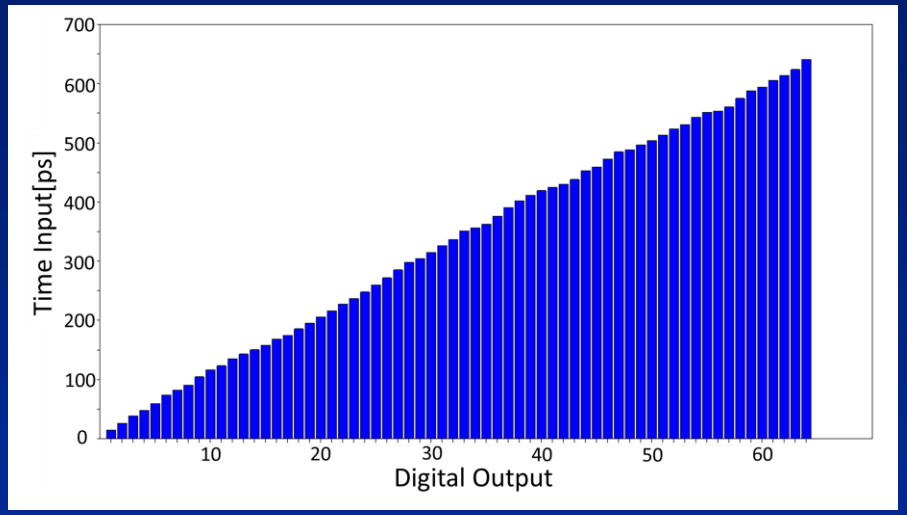
Simulation Verification

Relative variation

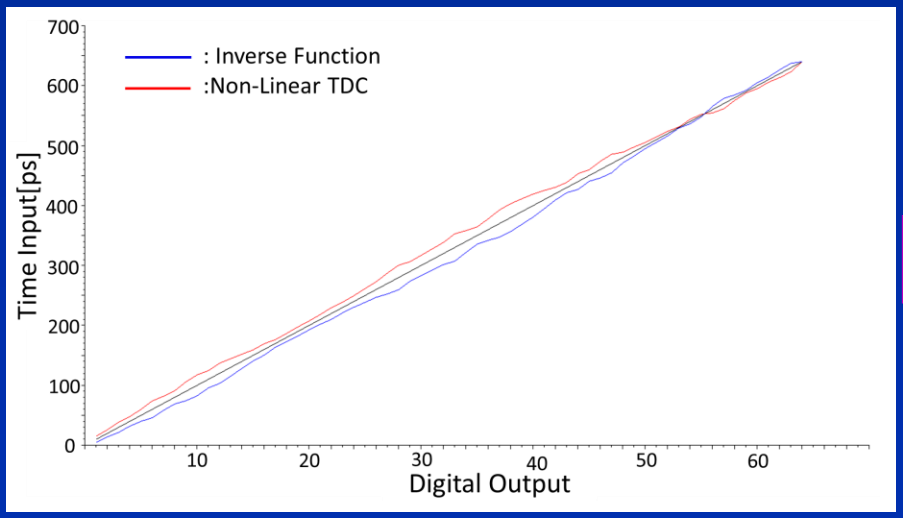
Delay variation

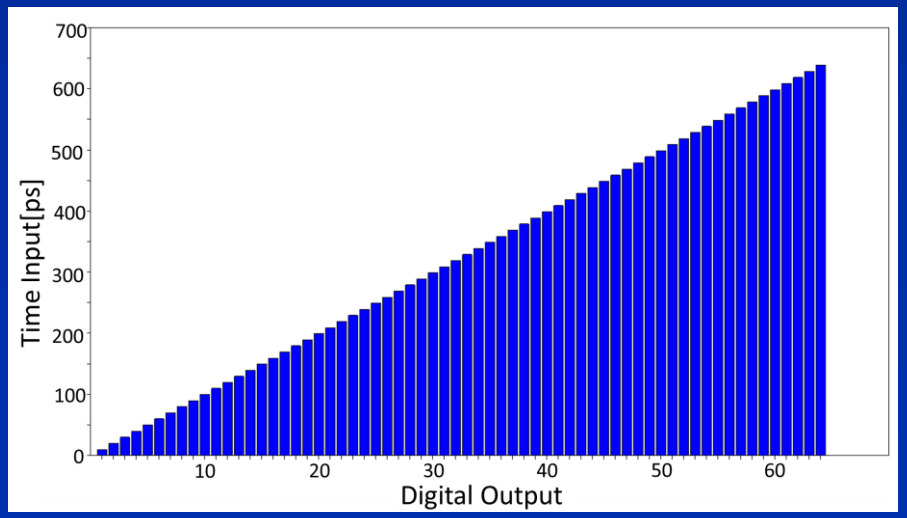


TDC characteristics before calibration



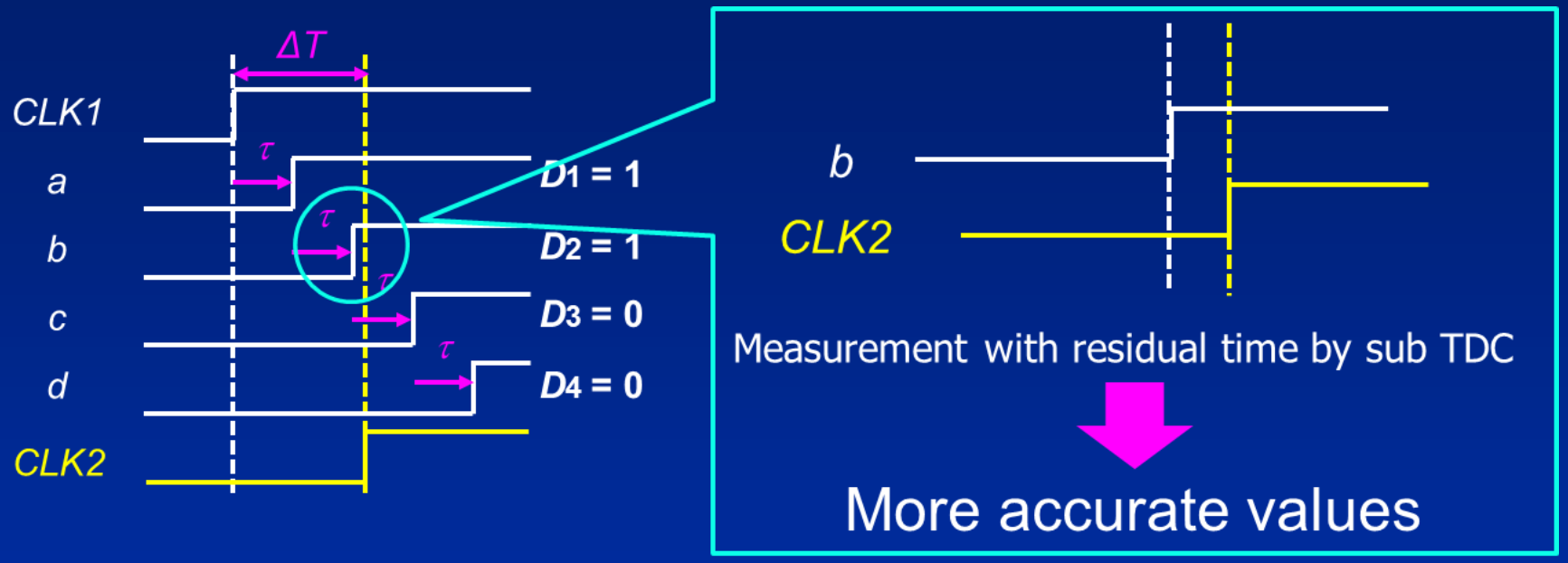
TDC characteristics after calibration





Fine Time Resolution with 2-Step Method

Absolute variation

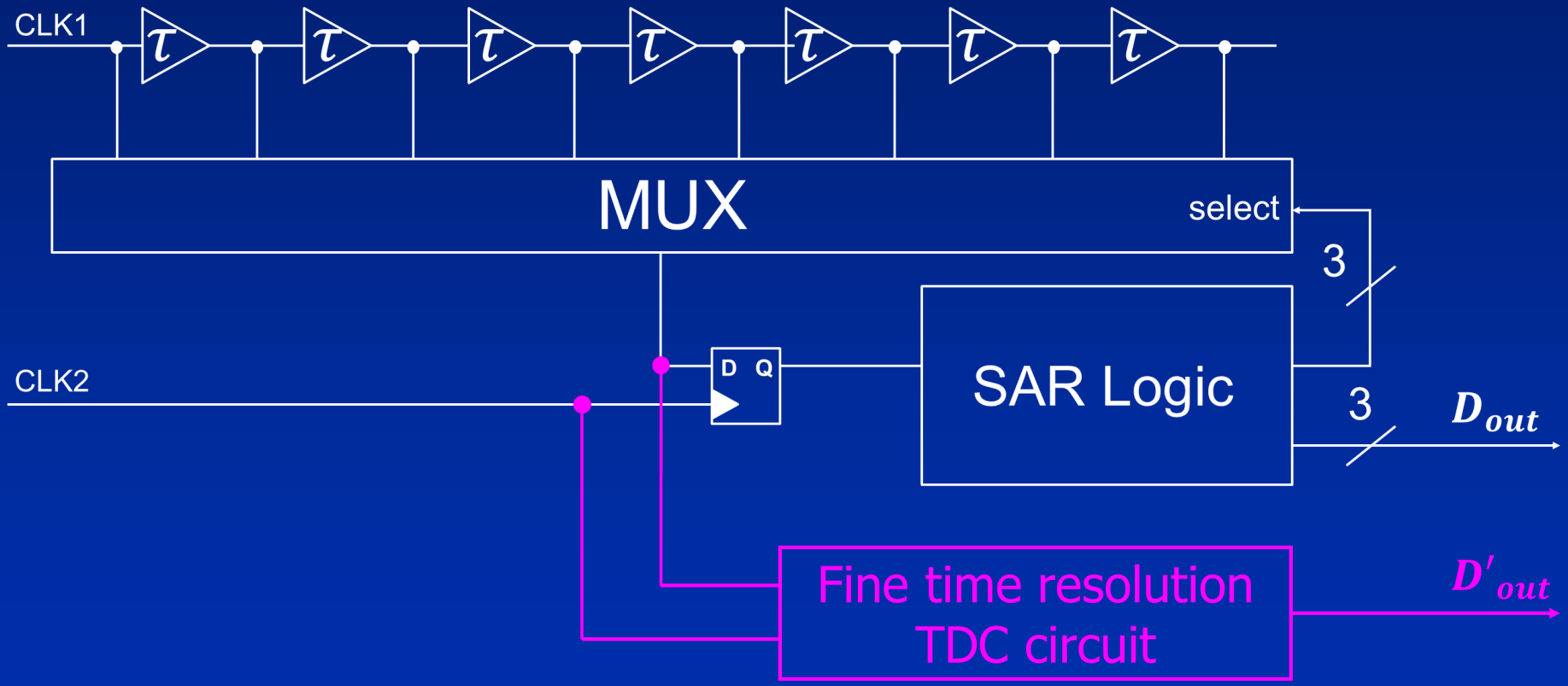


Step1 : SAR TDC → Integer time | **Residual time**

Step2 : SAR +Vernier TDC → Measurement of residual time

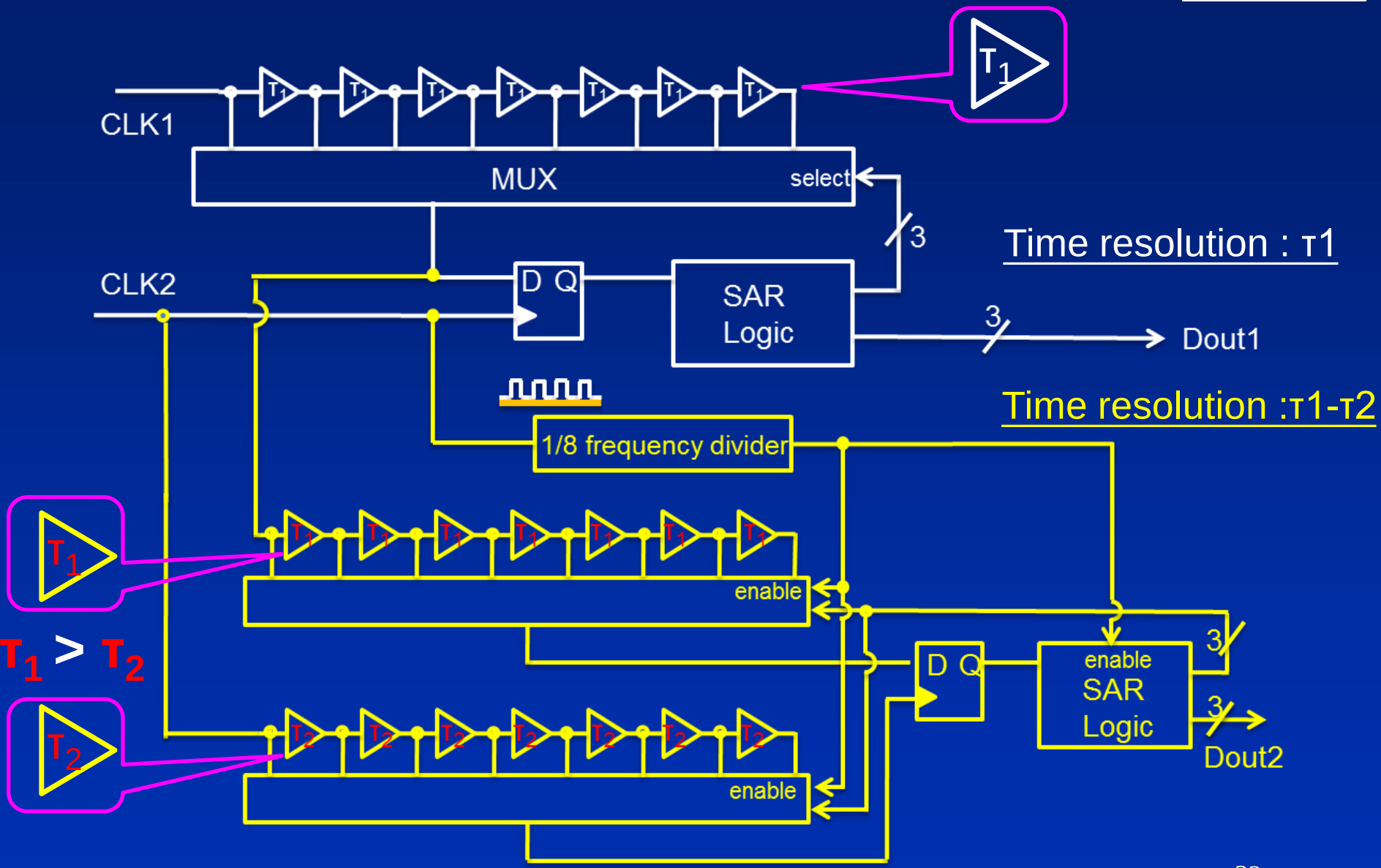
Block Diagram of SAR + Vernier TDC

Absolute variation



Configuration of SAR + Vernier TDC

Absolute variation

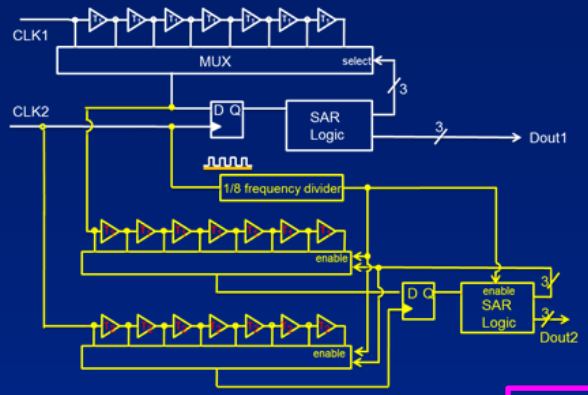


Calibration algorithm in 2-step SAR TDC

Absolute variation

# of samples: 3

$n_{\blacksquare}$, $m_{\blacksquare}$:outout data
$T_{\blacksquare}$:Known input data



D_{OUT1} → $n_{\blacksquare}$

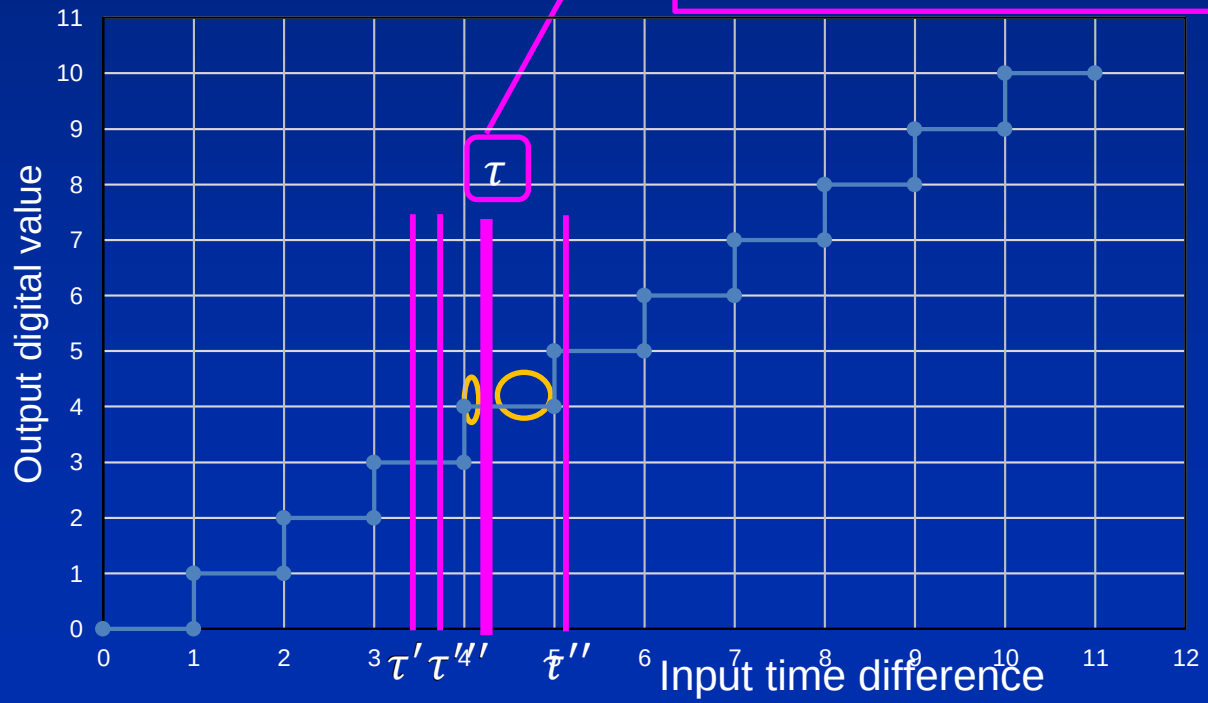
D_{OUT2} → $m_{\blacksquare}$

$$\begin{cases} n_A\tau_1 + m_A\tau_3 \cong T_1 \\ n_B\tau_1 + m_B\tau_3 \cong T_2 \\ n_C\tau_1 + m_C\tau_3 \cong T_3 \end{cases}$$

※ $\tau_3=\tau_1-\tau_2$

$$\begin{cases} \tau' = m_1\tau_1 + n_1\tau_3 \doteqdot T_1 \\ \tau'' = m_2\tau_1 + n_2\tau_3 \doteqdot T_2 \\ \tau''' = m_3\tau_1 + n_3\tau_3 \doteqdot T_3 \end{cases}$$

Find exact value of τ_1 or τ_2



Simulation Results

Absolute variation

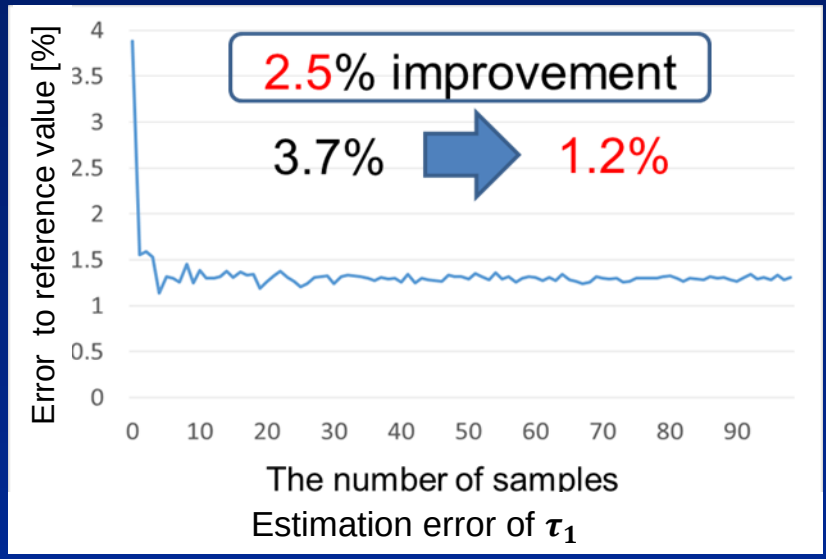
τ_1

# of samples : 2

About 3.7%

# of samples : 100

About 1.2%



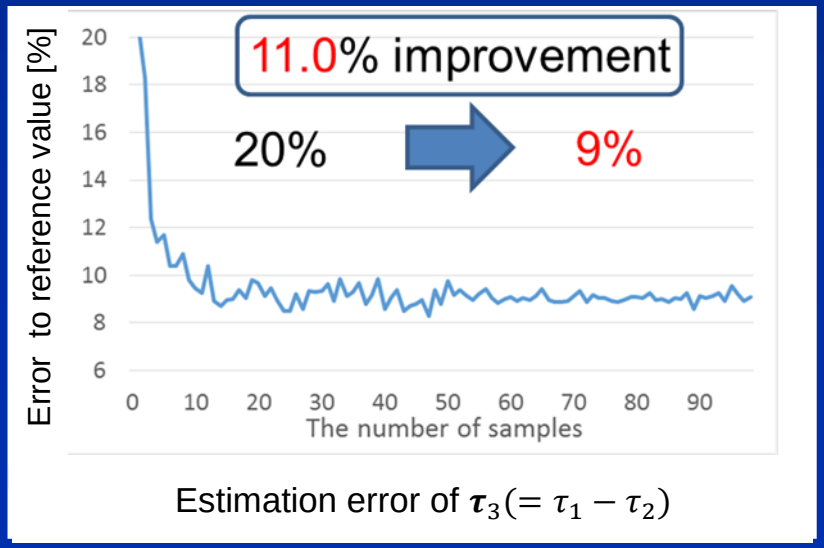
τ_3

# of samples : 2

About 20.0%

# of samples : 100

About 9.0%



※ $\tau_3 = \tau_1 - \tau_2$

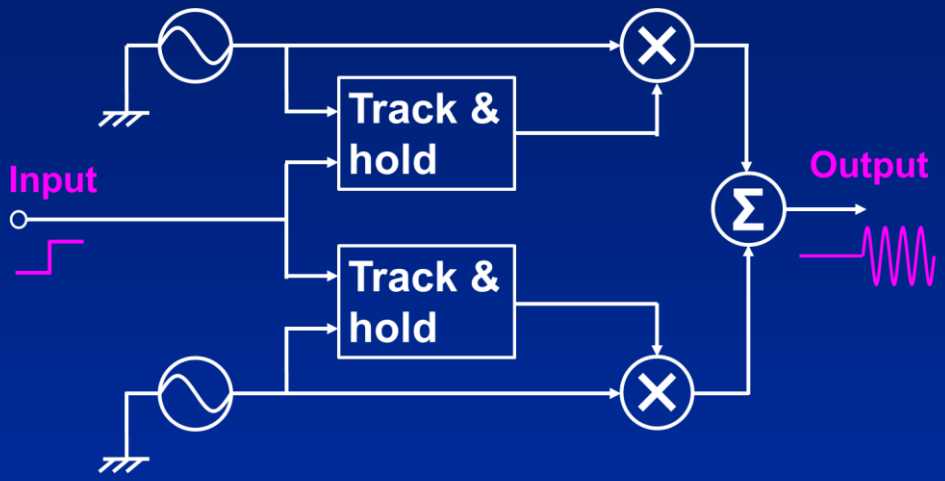
Outline

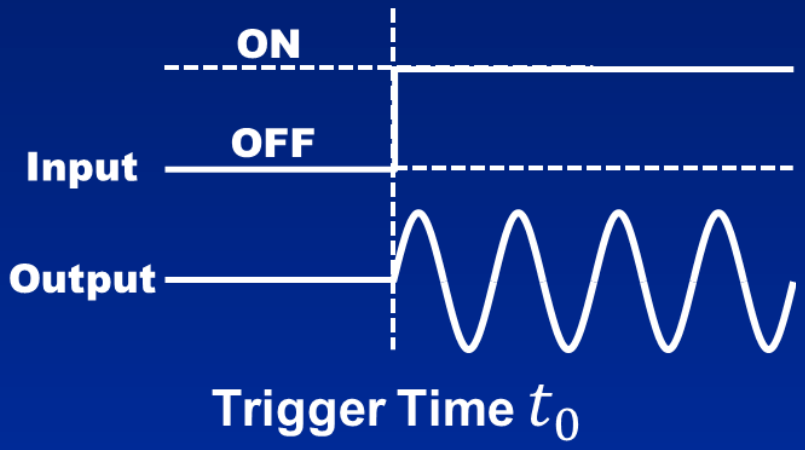
- Research Objective
- TDC Application to LSI Testing Technology
- SAR TDC Architecture & Operation
- SAR TDC with Self Calibration

  -Relative variation

  -Absolute variation
- SAR TDC Employing Trigger Circuit
- Summary

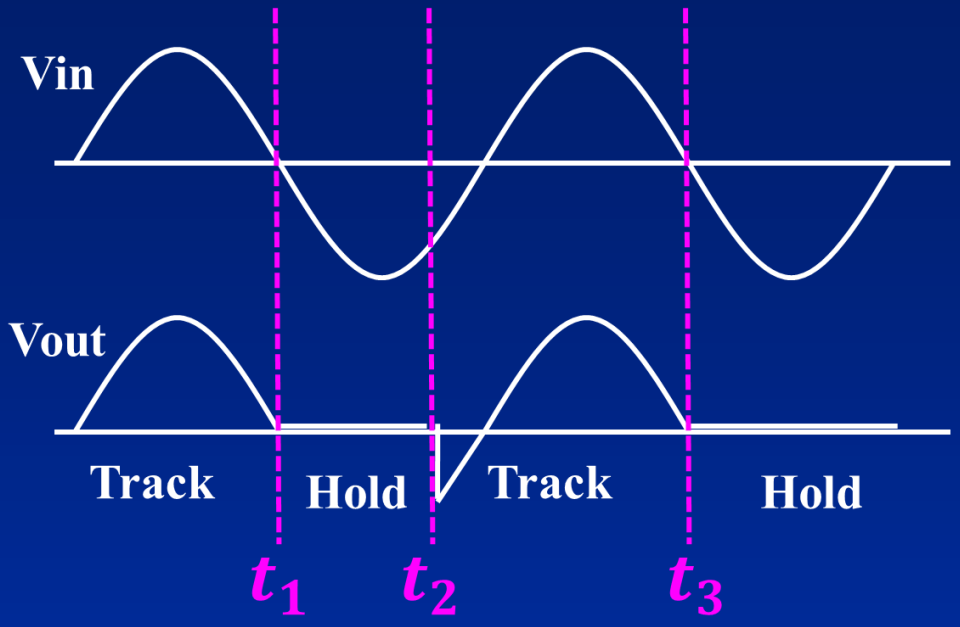
Trigger Circuit

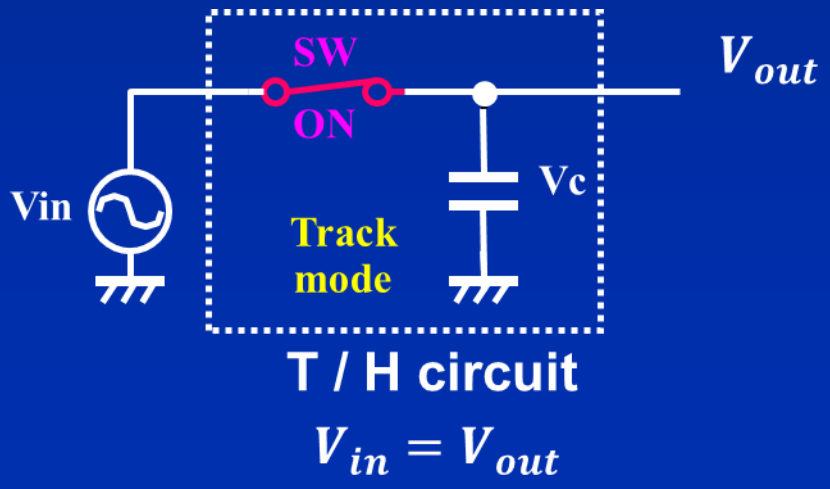


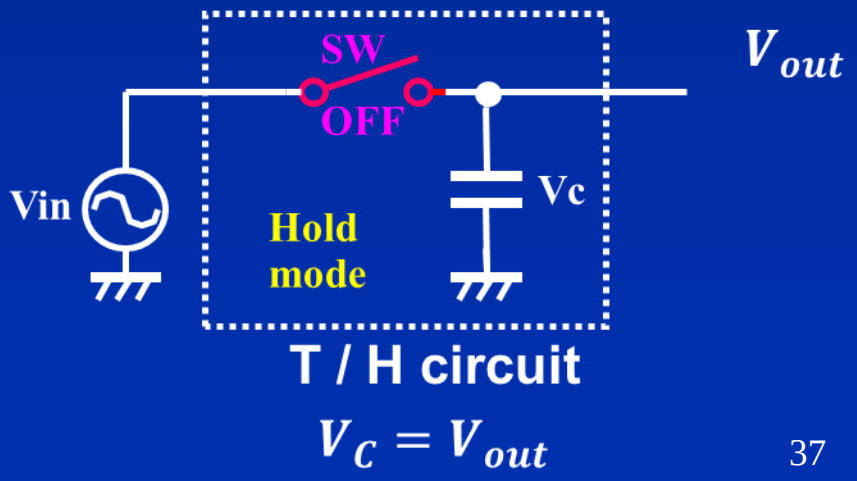


- Output starts to oscillate at rising timing edge of input

T/H Circuit


Vin
Vout
Track
Hold
Track
Hold
t_1
t_2
t_3


SW
ON
V_{out}
Vin
Vc
Track
mode
T / H circuit
$V_{in} = V_{out}$

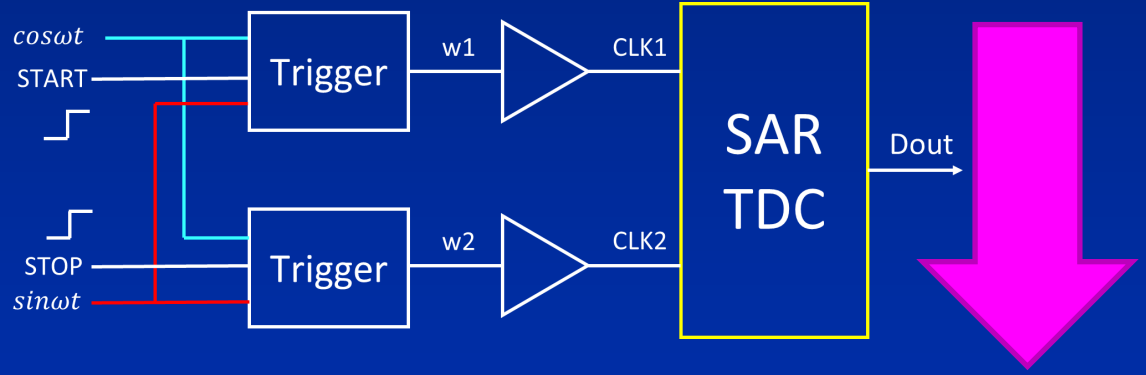

SW
OFF
V_{out}
Vin
Vc
Hold
mode
T / H circuit
$V_C = V_{out}$

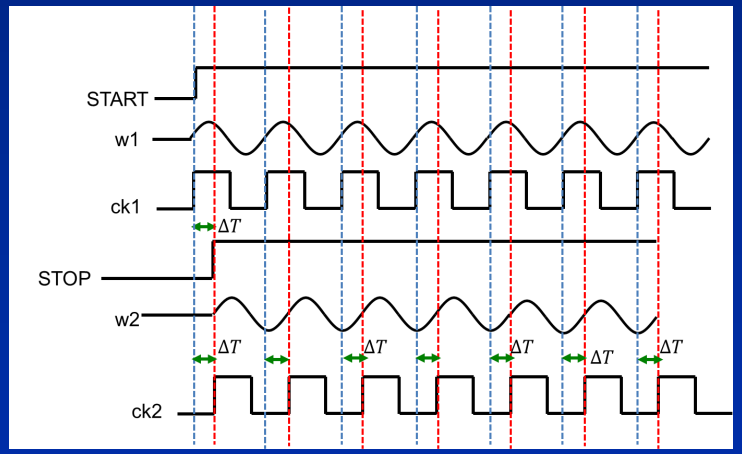
Problem of SAR-TDC & Remedy

Usual

Voltage can be held

Time difference cannot be held





Suggestion

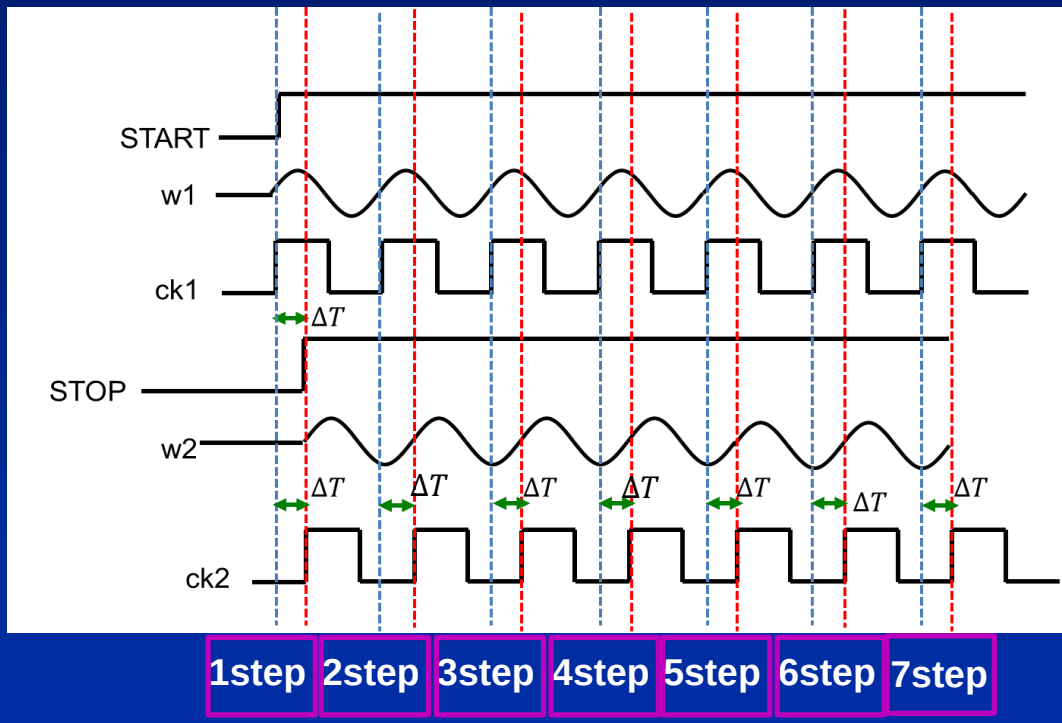
Time difference can be held !

One-shot Timing Measurement Using Trigger Circuit

Suggestion

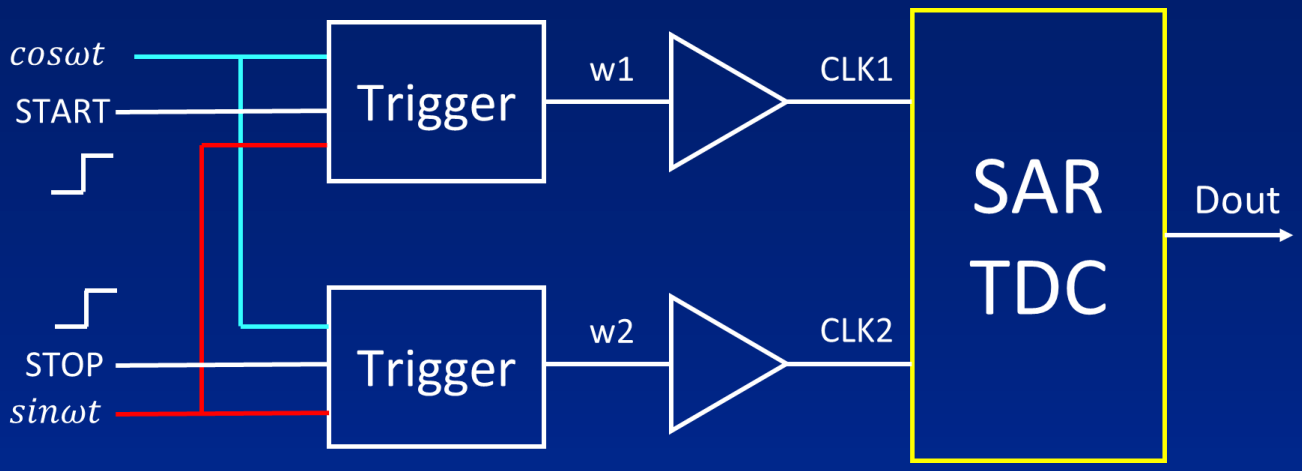
Input START, STOP signal

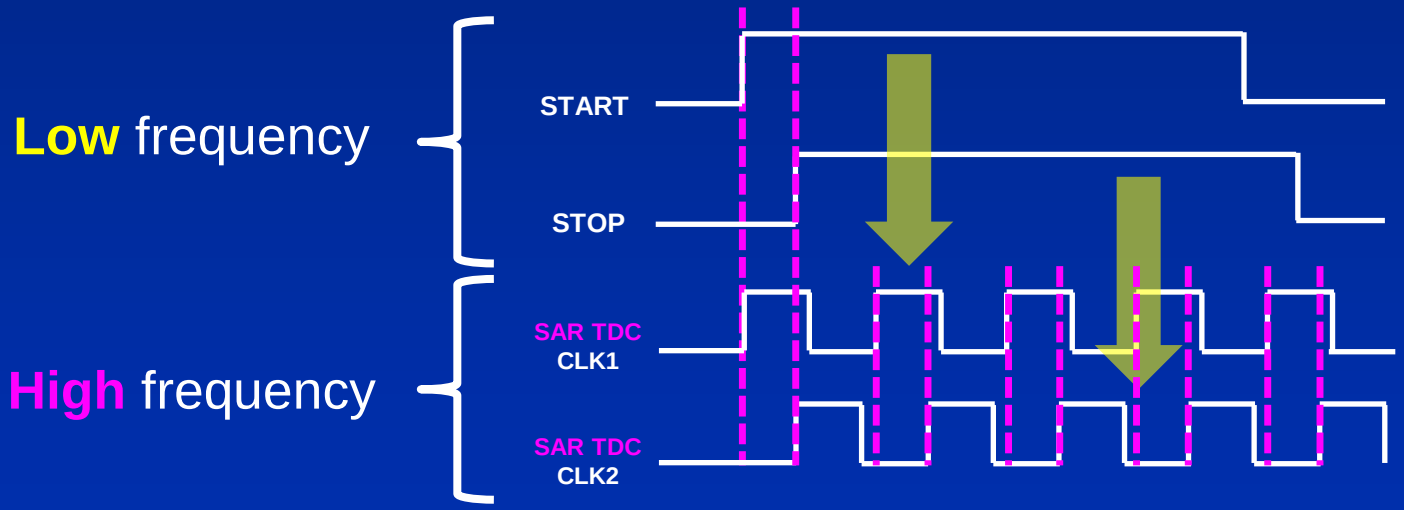
Oscillate with initial phase at input timing



It can hold the time difference using two trigger circuits

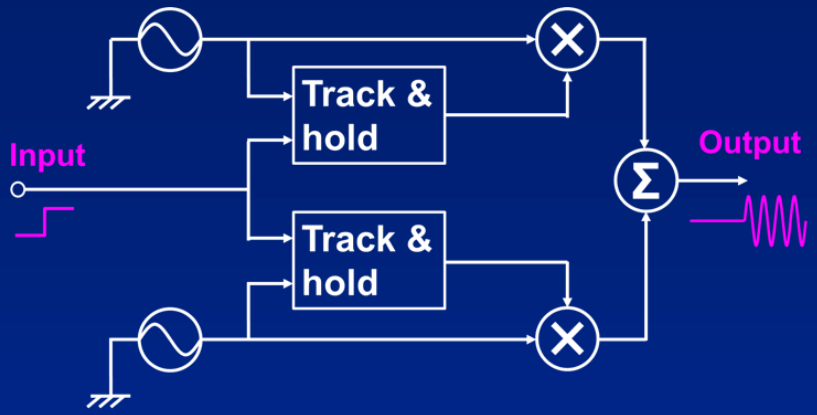
Low Frequency Clock Measurement

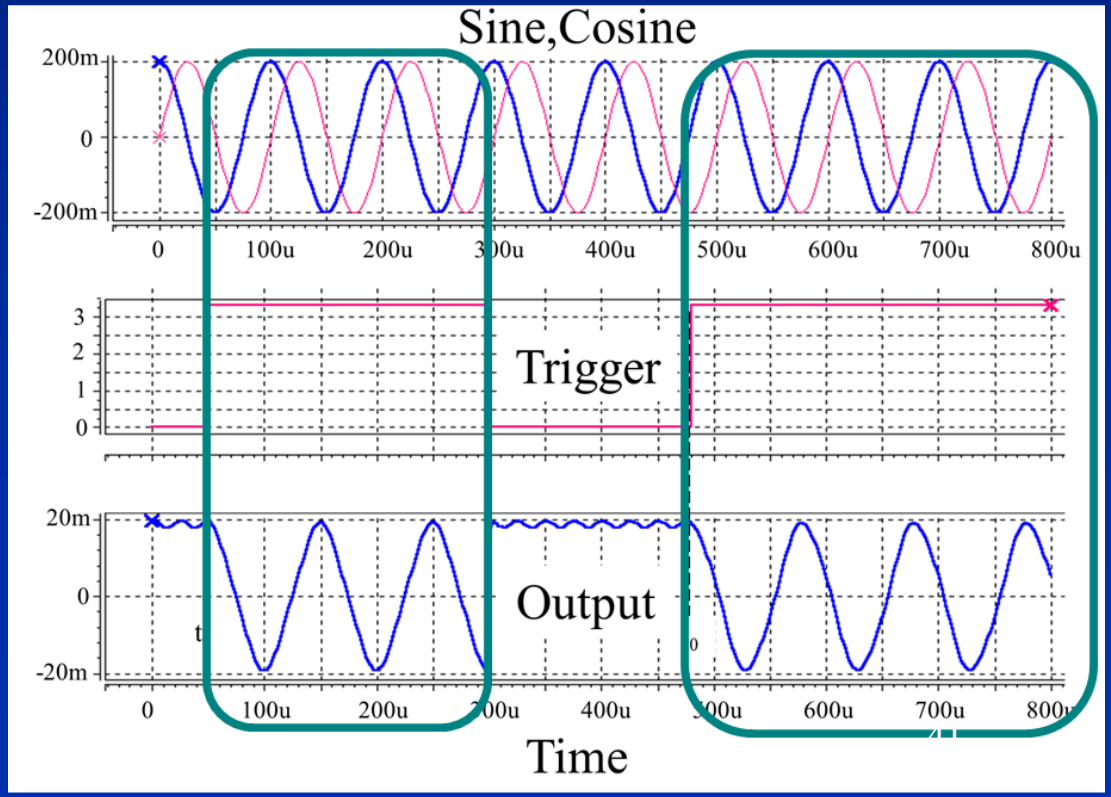




Short testing time for low frequency repetitive timing

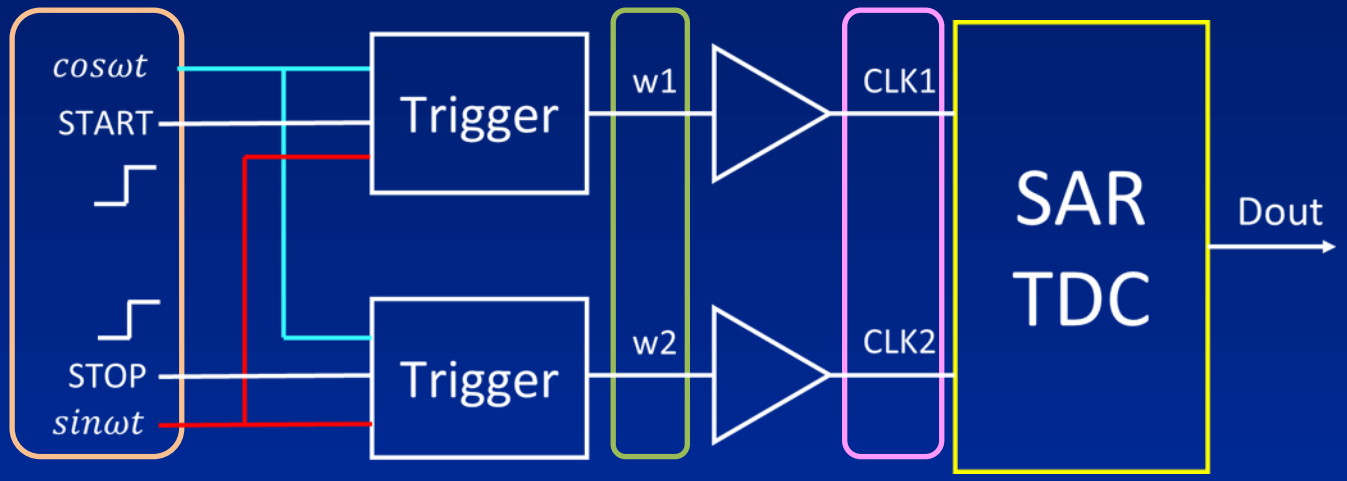
Trigger Circuit Waves

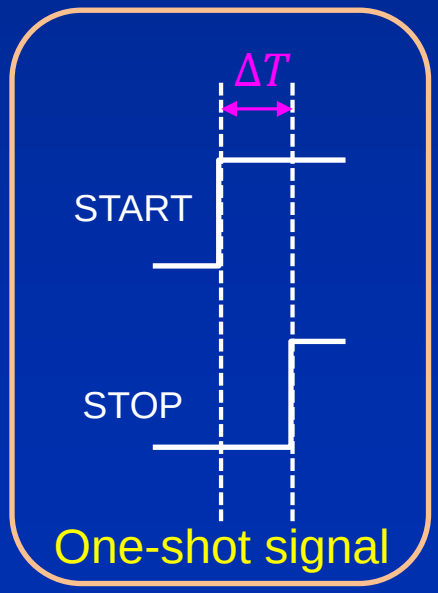


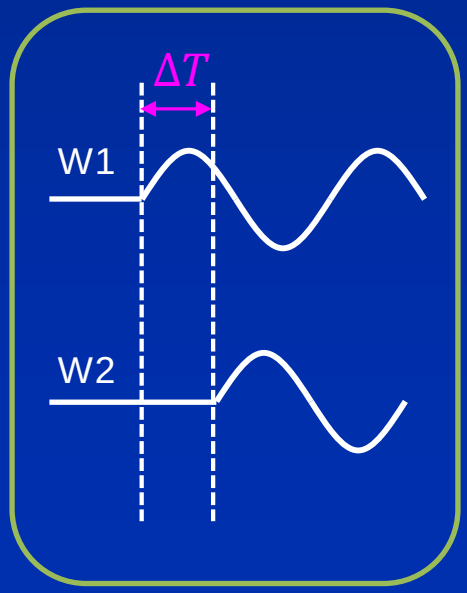


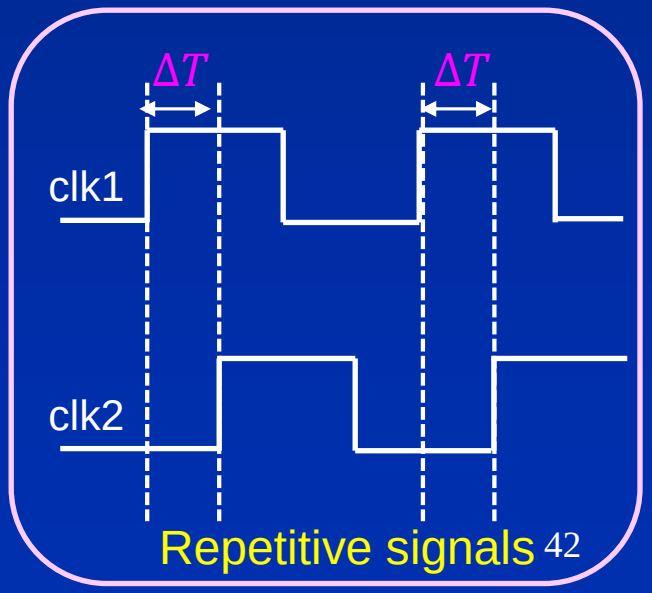
Combination of Trigger Circuit & SAR TDC

Proposed Circuit

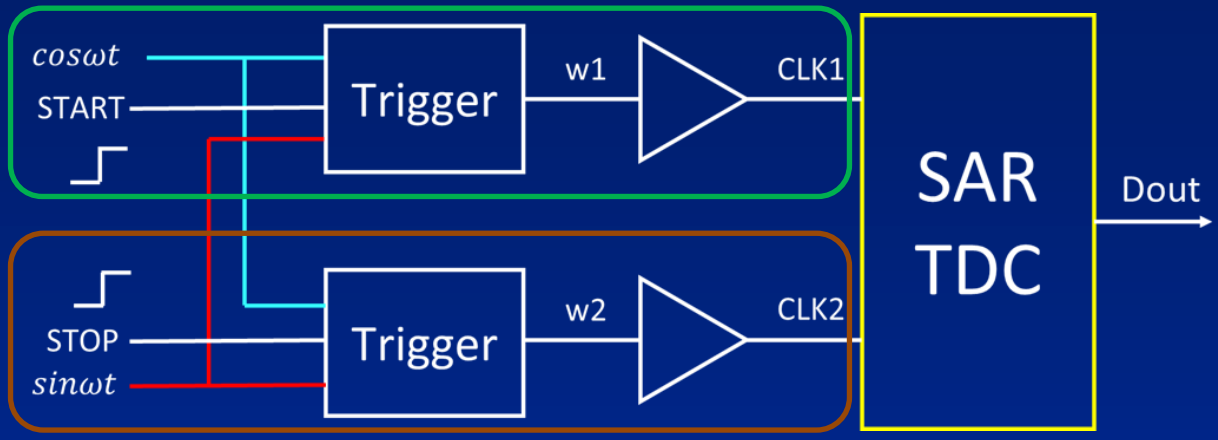


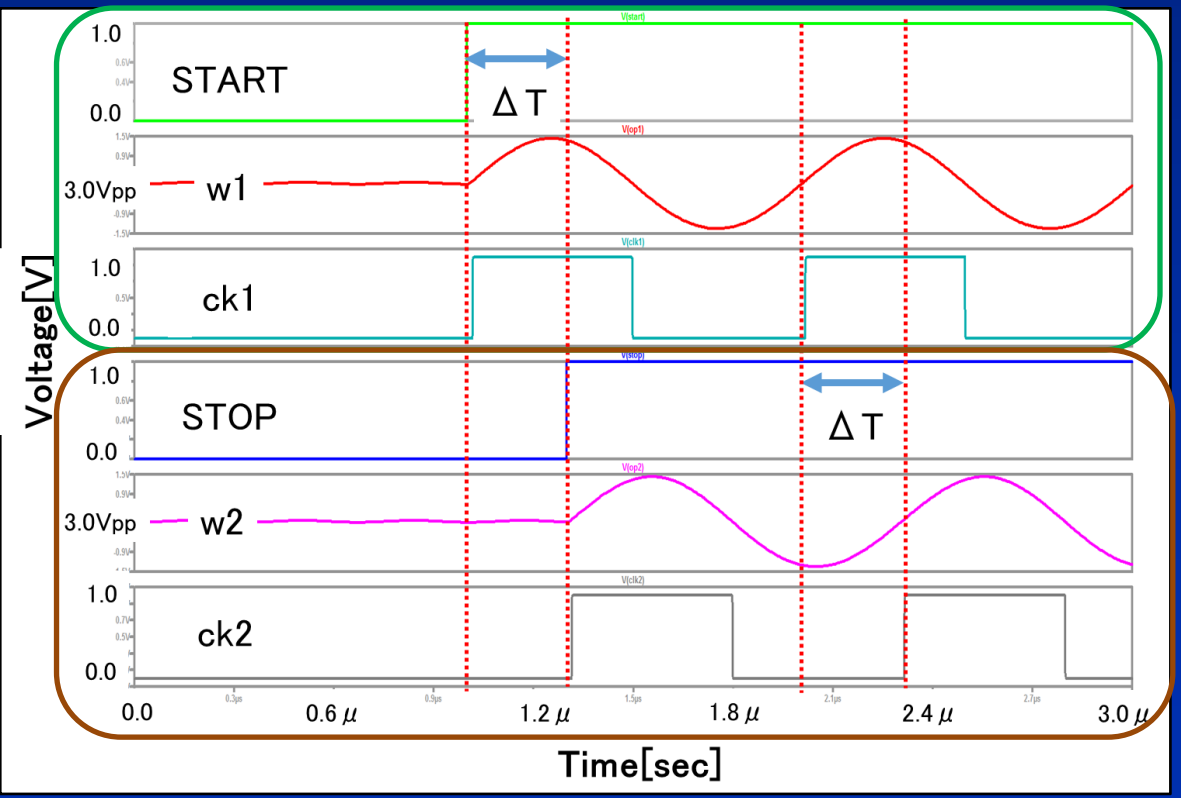






One-Shot Timing Measurement Simulation





2 trigger circuits can generate **repetitive signals**

One-shot timing can be measured with SAR TDC

Outline

- Research Objective
- TDC Application to LSI Testing Technology
- SAR TDC Architecture & Operation
- SAR TDC with Self Calibration

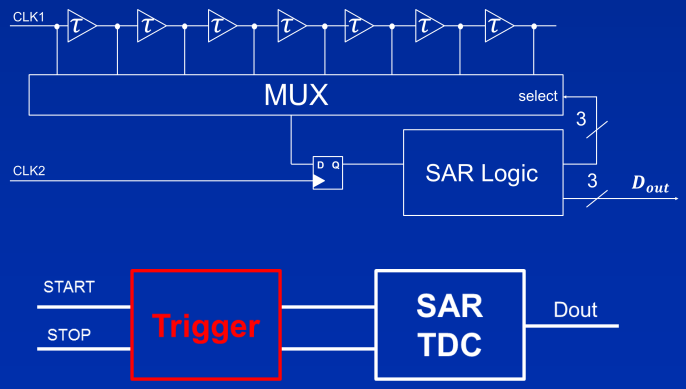
  -Relative variation

  -Absolute variation

- SAR TDC Employing Trigger Circuit
- Summary

Summary

- SAR TDC with self-calibration has been introduced
- Trigger circuit can generate repetitive signals
- One shot timing can be measured with SAR TDC



- ✓**Small circuit**
- ✓**Full digital**
- ✓**High linearity**
- ✓**High resolution**

Timing testing at low cost

Thank you for your attention

Q & A (1)

Q1 : You said the circuit scale of SAR TDC can be realized very small. Does it prove something? Are there any data? And how small is SAR TDC compared with Flash TDC?

A1: We confirmed it with FPGA, but I don’t have any data. But I have appendix slides. As you can see, In the flash TDC, at 10 bits, D-FFs are 1023. But, In the SAR TDC, at 10 bits, DFFs- are 23. And multiplexer can be realized small, simple switches. So circuit scare can be small.

Q & A (2)

Q2 : Interesting topic & study. How to configure delay elements? How to calibrate delay elements values?

A2 : Delay elements values cannot be calibrated directly.

But we can “digitally” calibrate by estimating original values of that TDC up to the decimal point. And this is appendix slides(P53,54). If the value of t1 is very large, there will be many occurrences of 100 at the stop A signal and 011 at the stop D signal.

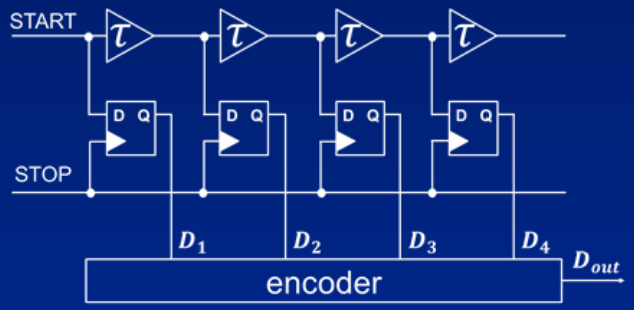
Q & A (3)

Q3 : How to input reset signal to proposed circuit's D-FF in calibration mode?

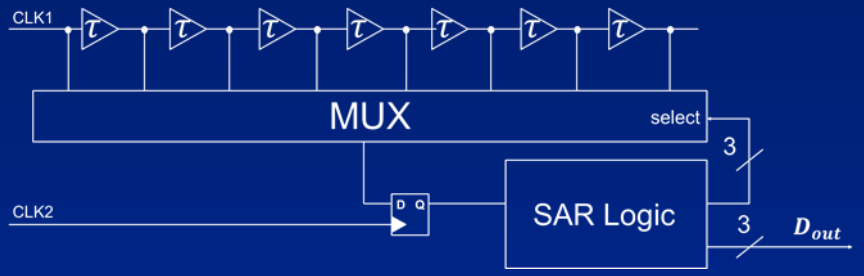
A3 : Sorry, I need to check. I'll send e-mail after.

Appendix

Flash TDC vs. SAR TDC



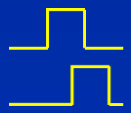
Flash TDC

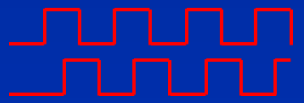


SAR TDC

10-bit :1023  # of D-FFs **10-bit : 23** 

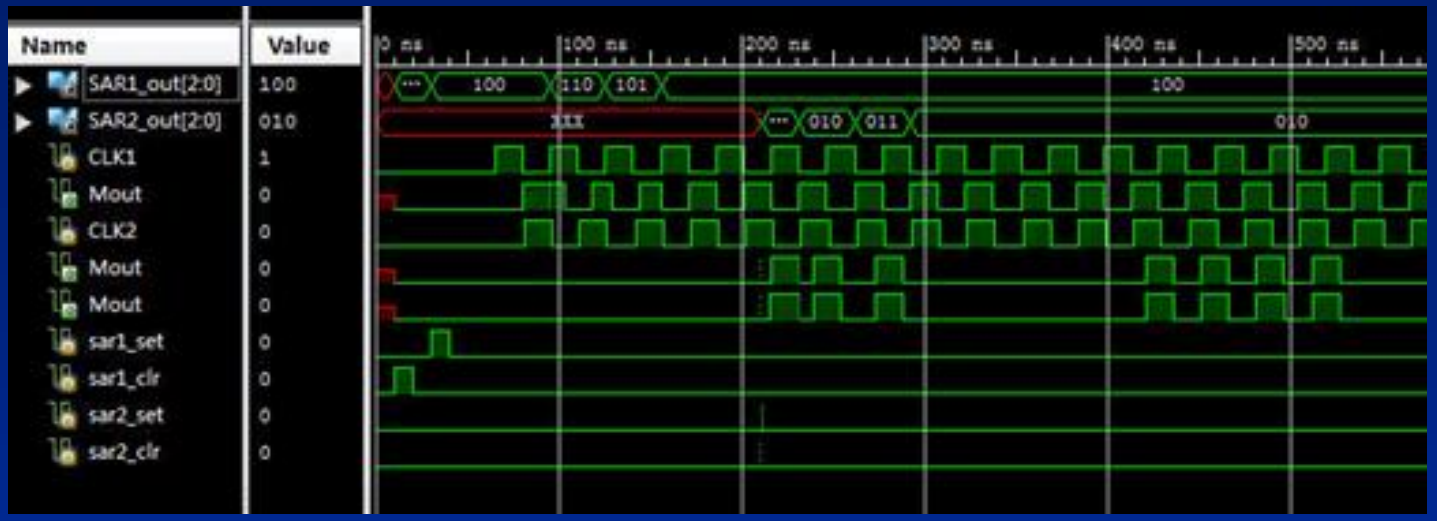
One Shot  Timing Signal Repetitive 



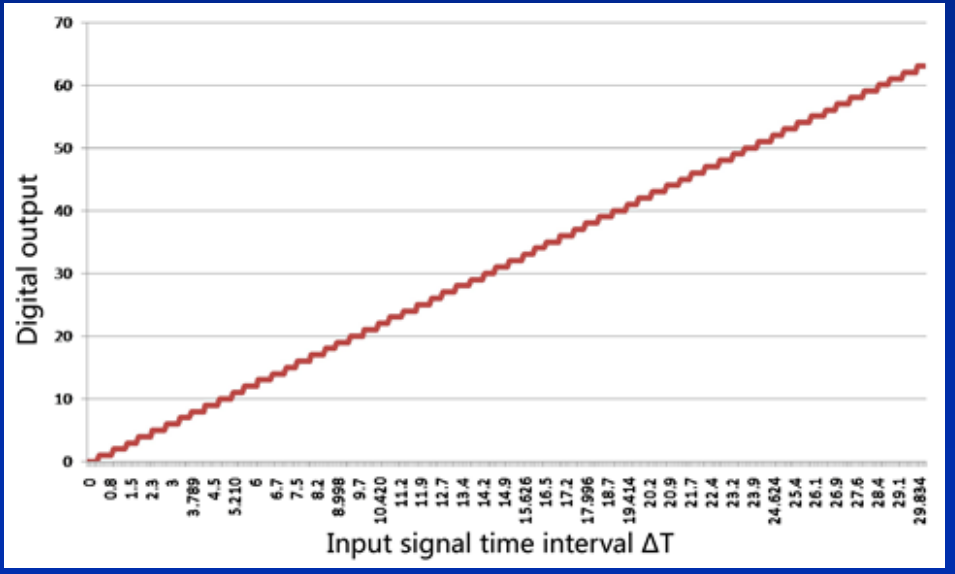


FPGA Implementation of 2 step SAR TDC

XILINX ISE

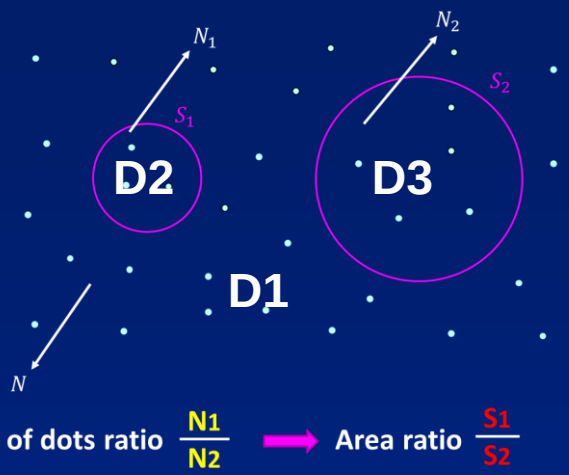


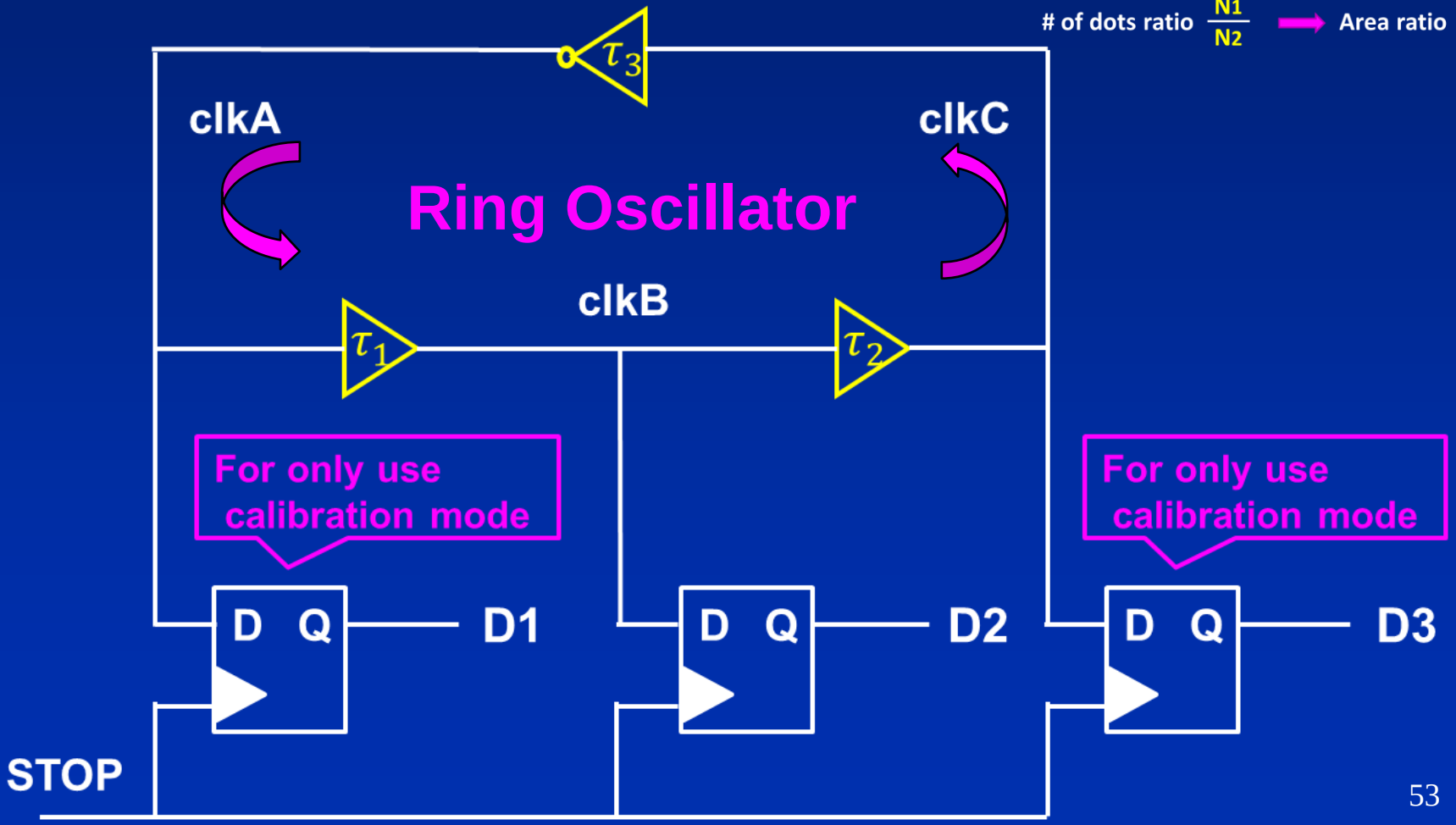
Frequency of CLK1 & CLK2: 33MHz
Time delay of buffers:
τ1 = 3.788ns, τ2 = 3.314ns
Minimum time resolution:
τ1-τ2 = 1/8τ1 = 0.474ns
△T to be measured:
4.3τ1 = 16.286ns



Simulation results :
{Dout1, Dout2}=4.250τ1=16.099ns
Error=0.050τ1=0.189ns

Simplified Model

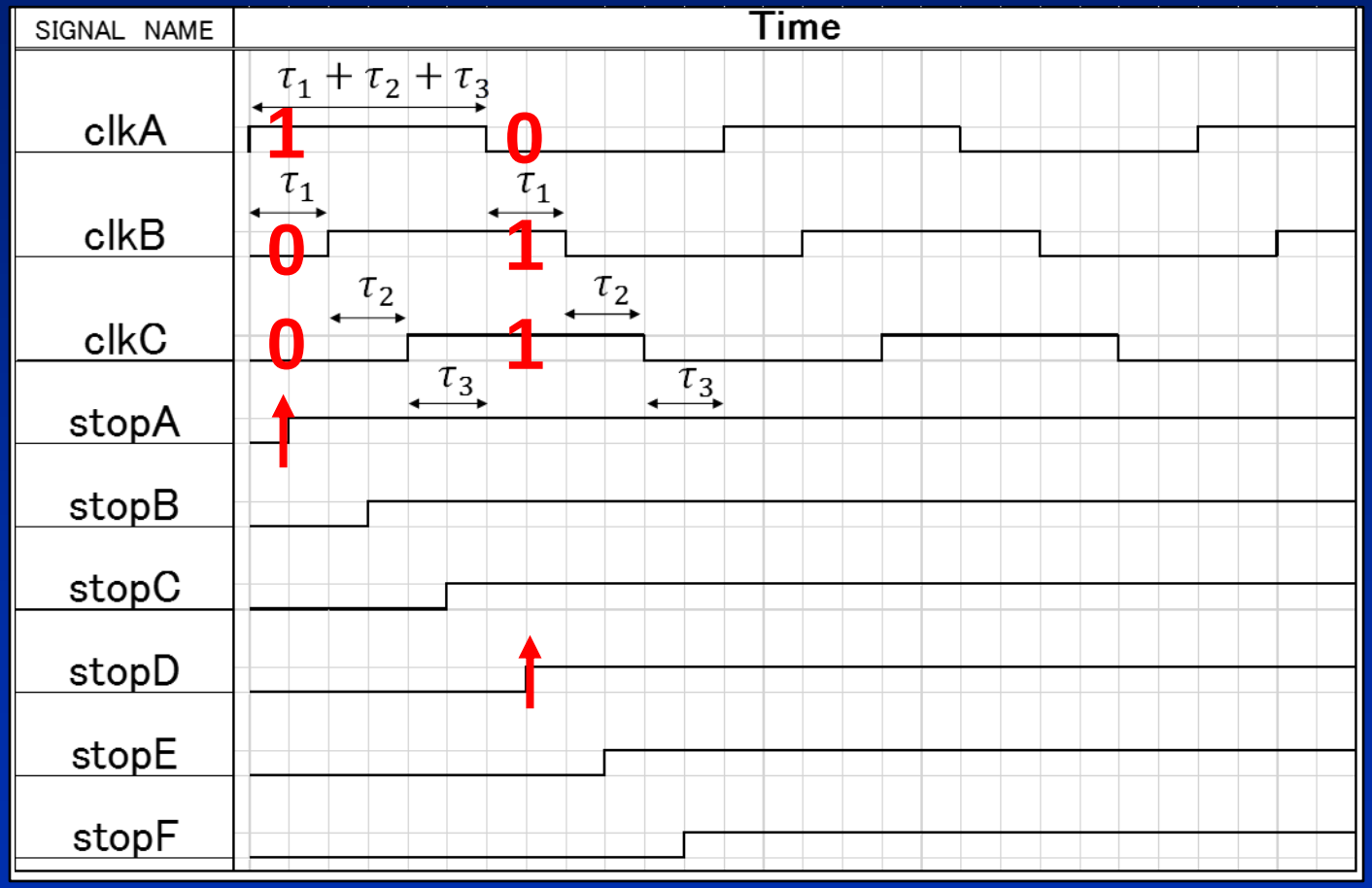




Operation of Histogram Method

Ring Oscillator

Asynchronous Clock



Two-stage CMOS Trigger Circuit