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Redundant SAR ADC Algorithm for Minute Current Measurement

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Abstract. This paper investigates a successive approximation register (SAR) AD conversion algorithm for measuring a minute current source. We consider the case that the input current is very small, and the sample & hold (SH) circuit in front on the SAR ADC takes relatively long time to settle completely. If a binary search SAR ADC is used, it has to wait until the SH circuit settle completely because the binary search has no redundancy. Then we propose to use a redundant search SAR ADC which can start to operate before its complete settling. Even if a decision error of successive comparison occurs in the previous stage because of the incomplete setting of the SH circuit, it can be corrected in the subsequent stage, thanks to the redundancy. Then the SAR AD conversion time can be shortened. We will present its operation principle and simulation results.

1. Introduction

We consider here to measure a minute current, such as for precise current source trimming. However, it takes relatively long time to measure it using a conventional binary SAR ADC. The SH circuit in front of the SAR ADC takes long time to settle completely for a minute current input. The binary search SAR ADC has no redundancy and it can start to operate only after the SH circuit settles completely; it takes a relatively long time. On the other hand, the redundant search SAR ADC can start to operate before incomplete settling of the SH circuit, because the wrong decisions in early SA stages can be corrected in latter SA stages thanks to the redundancy.

In this paper we thought that we can improve the settling time of the SH circuit by using the Fibonacci sequence and shorten the measurement of the small current source. And we have investigated its possibility and shown their simulation results.

2. Problems and Solutions to Minute Current Source Measurement

We consider a minute current source measurement using SAR ADC. In this case, the settling time of the SH circuit of the preceding stage becomes longer, which affects the measurement time (Fig. 1). Therefore, changing the later stage from the binary type to the redundant type is considered for the measurement time of each step to be shortened and for the measurement speed to be increased.

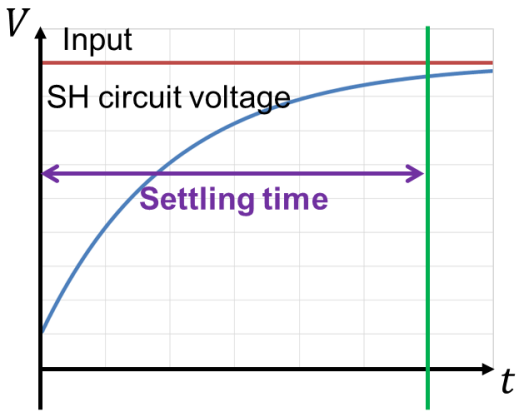

Fig. 1. Settling time of an SH circuit

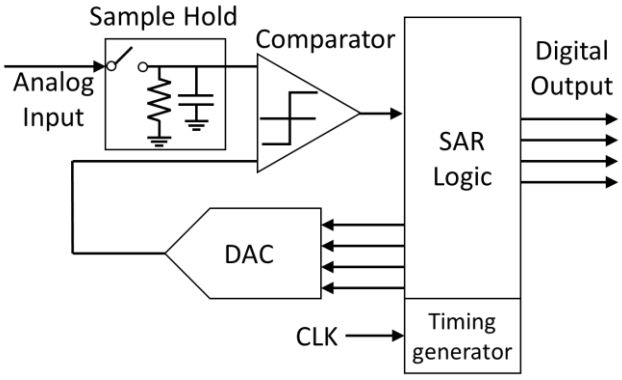

Fig. 2. Block diagram of an SAR ADC

3. SAR ADC and Redundancy Design

3.1 SAR ADC

SAR ADCs are used for medium sampling speed and high-resolution applications. Since they have features of low power and small chip area, they are widely applied to such as automotive, factory automation. Furthermore, it does not require operational amplifiers, which is suitable for nano-CMOS implementation.

The SAR ADC consists of an SH circuit, a comparator, a DAC, SAR logic and a timing generator (Fig. 2). For precise AD conversion, enough accuracy of the SH circuit and the DAC is required.

Conversion of the SAR ADC is based on principle of balance and generally it uses the binary search algorithm. Firstly, the SH circuit acquires an analog input voltage. Secondly, the comparator compares the input analog voltage and the reference voltage that is generated by the DAC and decides 1-bit digital output. Thirdly, SAR logic provides the DAC input based on the comparator output. The input voltage and the updated DAC output voltage are compared by the comparator. This operation is repeated and finally the SAR ADC can obtain the whole digital output. Fig. 3 shows the binary search algorithm of a 4-bit SAR ADC. The bold line in Fig. 3 indicates the reference voltage value to compare with the analog input at each step. Their values are calculated by either sum or difference between the last step reference voltage and the weighted voltage p(k) of each step as shown in Fig. 3.

3.2 SAR ADC Redundancy Design

Redundancy design is a popular technique to improve circuit and system performance. To apply the redundancy design to the SAR ADC means adding extra comparison [1-6]. This method changes binary weights to non-binary weights for the DAC and realizes digital error correction with redundancy property.

Fig. 4 shows an example of two redundant search operations of a 4-bit 5-step SAR ADC. There, the input voltage is 8.3LSB and the reference voltage weights p(k) are 1, 2, 3, 6 and 8. The one operation (solid arrows) assumes that the comparison is correct, whereas the other (dotted arrows) assumes that it is incorrect. However, both obtain the correct digital output of 8 by digital error correction. In the 4-bit 5-step SAR ADC as shown in Fig. 4, there are 25 comparison patterns and 24 output patterns. In other words, a given output level can be expressed by multiple comparison patterns. Thus, even if comparator decision is wrong at some steps, the correct ADC output may be obtained. Then we can make reliable SAR ADC.

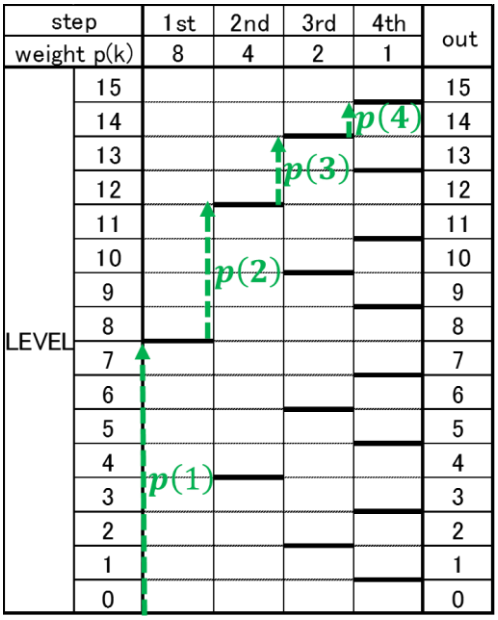

Fig. 3. Binary search algorithm of a 4-bit 4-step SAR ADC.

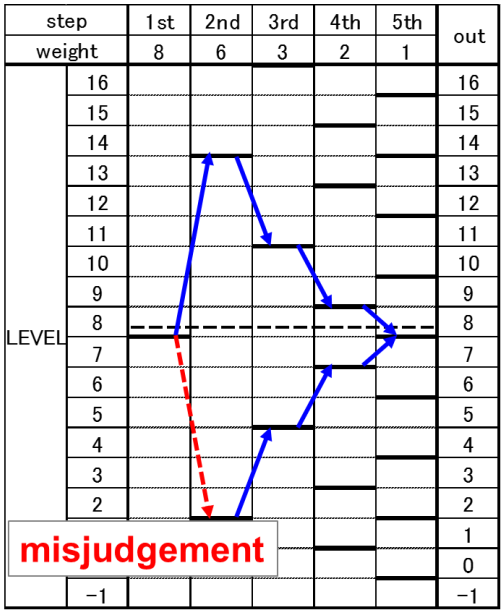

Fig. 4. Operation of a 4-bit 5-step SAR ADC in case of correct and incorrect judgments.

In addition, even if the number of the comparison steps is increased, the digital error correction enables high-speed AD conversion as a whole, because the digital error correction can take care of the DAC incomplete settling [1-6]; thus redundancy design has potential for reliable and/or high-speed SAR AD conversion.

3.3 Conventional Redundancy Design Issues

Reference voltage weight p(k) greatly affects redundant SAR ADC performance, and designers have selected p(k) by using Eq. (1). Here, M is the number of the whole steps and k is comparison step number.

$$p(k) = R^{M-k} \tag{1}$$

But conventional decision methods of reference voltage weights p(k) [1-5] have several issues as follows:

(1) First, the reference voltage weight p(k) in Eq.(1) is not an integer which is not suitable for the circuit design. We must round p(k) values to use integer for easy design and accurate conversion. However, the rounding operation causes variability of the correction capability at each step and they may disturb performance improvement.

(2) Second, there is difficulty of appropriate radix choice. ADC designers must choose a proper radix R ($1 \leq R < 2$) in Eq.(1). Fig. 4 shows an example in case of radix 1.80 and using rounding. However, in Fig.5, two-way arrows indicate that correctable input range cannot cover all input range, which means that there are some ranges that cannot be corrected. There is a trade-off between correction capability and conversion speed, and the SAR ADC designer is forced to search a radix that is the most suitable for SAR ADC.

(3) Third, there is an issue of internal DAC configuration. In the binary search SAR ADC, its internal DAC is realized easily by using binary network topology. But it is difficult to design the internal DAC of redundant SAR ADC. Conventional methods have realized internal DAC by complicated and large circuits.

We have shown the first and second issues are solved by Fibonacci sequence redundancy algorithm [6]. Further, this paper shows the Fibonacci sequence method also solve third issue.

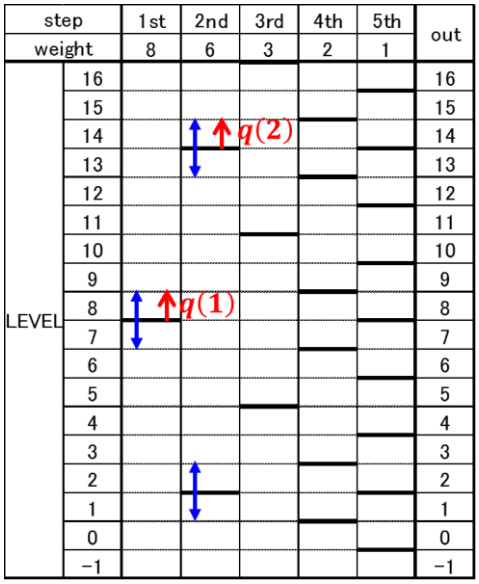

Fig. 5. 4-bit 5-step SAR ADC algorithm and definition of correctable difference q(k).

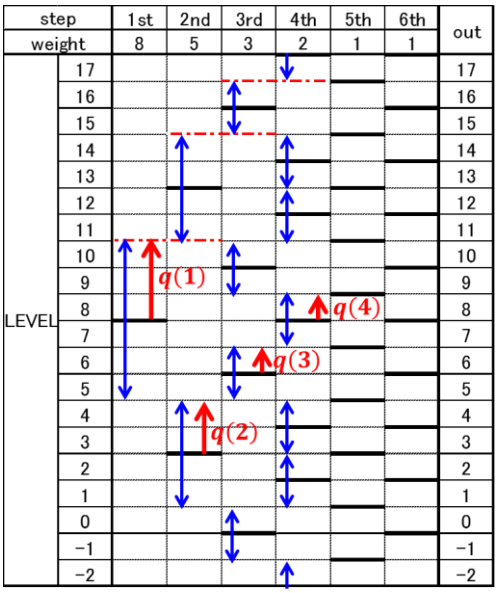

Fig.6. Redundant search algorithm of a 4-bit 6-step SAR ADC using Fibonacci sequence.

4. Redundancy design using Fibonacci Sequence

4.1 Fibonacci Sequence

Fibonacci sequence is defined by a recurrence relation as shown in Eq.(2), where n in Eq.(2) is an integer greater than or equal to 0. Fibonacci sequence is presented in 1202 by Leonardo Fibonacci, who was a mathematician in Italy and it is known as one of the most famous number theories [7].

$$F_{n+2} = F_n + F_{n+1} \quad \text{where } F_0 = 0, F_1 = 1 \tag{2}$$

Fibonacci numbers are expressed as the following by calculating Eq.(2).

0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, 233, 377, …

In short, the sum of neighboring two terms is next term.
In addition, the closest terms ratio of Fibonacci sequence converges at about 1.62 as shown Eq.(3).

$$\lim_{n\to\infty} \frac{F_{n+1}}{F_n} = 1.6180339887 = \varphi \tag{3}$$

This ratio is called “Golden ratio” and it is widely recognized as the most beautiful ratio.
Fibonacci sequence and Golden ratio are based on very simple rules like the above. However we can find them in various places of our surroundings such as nature and humanity, and they have many interesting and unique properties. Thus they have been studied by many researchers for more than 800 years.

4.2 Fibonacci Sequence Redundancy design

We have studied redundancy algorithm using Fibonacci sequence to solve issues shown in Section 3.3. This algorithm selects Fibonacci sequence for reference voltage weights and realizes approximate radix 1.62 with only integer terms. Then, we have shown several advantages as the follows: Since Fibonacci sequence consists of integer terms, we don’t require rounding operation. Fig. 6 using Fibonacci sequence weighted SAR ADC shows that all input range is covered by correctable range showed two-way arrows. It means that high reliability is achieved unlike conventional methods in Fig. 4.

Furthermore, we also showed Fibonacci method's advantage at speed as well as reliability. The Fibonacci method proved to be the fastest method at all resolutions.

This is the result of simulation taking account of incomplete settling of the output of the internal DAC. Normally, the settling time of the output of the internal DAC is longer than the settling time of the SH circuit. However, the settling time of the SH circuit may be longer than the settling time of the output of the internal DAC in some cases. Section 5 shows that Fibonacci sequence weighting SAR ADC is effective for such cases.

5. New Discovery of Fibonacci Sequence Weighted SAR ADC

Considering the settling time of the SH circuit, we consider that the Fibonacci type which is the redundant type has shorter measurement time than the binary type. By relaxing the comparative condition in the first half, the speed can be increased. The misjudgement can be corrected by strengthening the comparison condition in the latter half. As a result, the measurement time of each step decreases and the judgment speed rises. This is shown by simulation.

5.1 Simulation

Considering the settling time of the SH circuit, we show that the Fibonacci type has shorter measurement time than the binary type.

The simulation conditions are as follows.

- This simulation uses Scilab as a simulation tool.
- We replace the minute current source of the input signal with the voltage source and consider the settling time of the SH circuit.
- The SH circuit is an RC series circuit.
- The resolution is changed from 1 to 14 bits, and the accuracy is set to 1/2 LSB.
- The initial voltage of the capacitor is set to half of the full scale.

The simulation method is as follows.

(1) When $V_{in} = 2^n$ which is the worst case, the time to be taken so that the difference between the output of the SH circuit and the input becomes 1/2 LSB is divided according to number of steps, and based on this, a clock is generated (Fig. 7).
(2) V_{in} is changed from 0 to 2^n and a judgment is made using this clock.
(3) When the difference between the judgment result and the input is less than or equal to the LSB, the operation is terminated; otherwise, the clock is increased until it is within the range and the judgment is continued.

Fig. 8 shows a binary type determination example when $V_{in} = 25$. Fig. 9 shows a Fibonacci type determination example when $V_{in} = 25$. In Fig. 9, it can be seen that judgment errors occur in 1st step and 6th step

Simulation results are shown in the Fig. 10, where the Fibonacci type has a measurement time faster than that of the binary type, and as the number of bits increases, the difference in measurement time increases.

6. Conclusion

We consider the settling time of the SH circuit when measuring a minute current source using SAR ADC. We have shown that the SH circuit output for a binary type SAR ADC without redundancy has to be completely settled. Fibonacci type with redundancy can shorten the measurement time of each step due to incomplete settling. As a result, the measurement time of the Fibonacci type is shorter than that of the binary type.

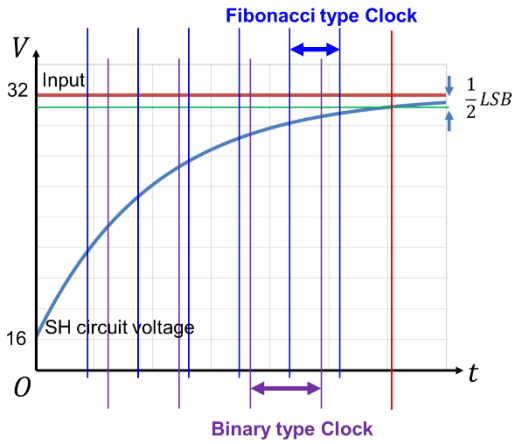

Fig. 7. Clock generation operation (5bit SAR ADC)

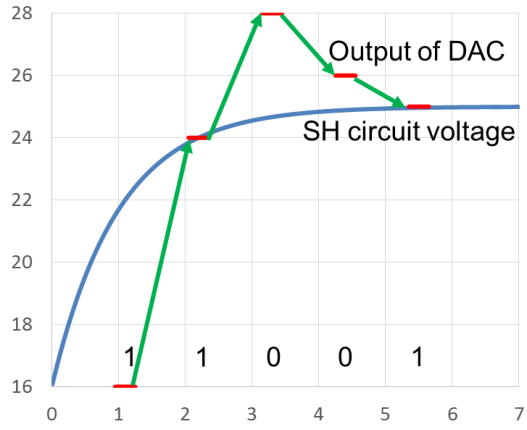

Fig. 8. Binary type determination example ($V_{in} = 25$)

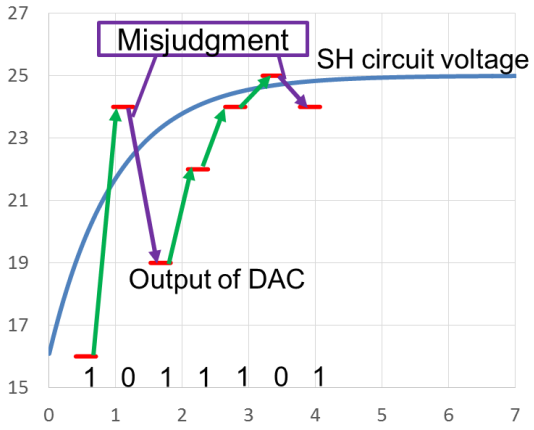

Fig. 9. Fibonacci type determination example ($V_{in} = 25$)

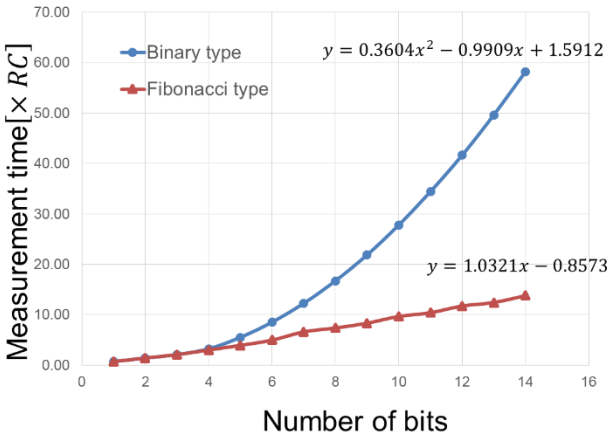

Fig. 10. Relationship between number of bits and measurement time

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