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Invited Paper

Noise Spread Spectrum with Notch Characteristics using Pulse Coding Technology for DC-DC Converter

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Abstract. This document explains a novel EMI spread spectrum technology with the adjustable notch frequencies using the automatic setting the notch frequency with the pulse coding method of the DC-DC switching converter for the communication equipment. In this paper, the notch frequency is automatically set to that of the received signal by adjusting the clock frequency using the equation Fn=(N+0.5)Fck. We have examined the theoretical notch frequency which is adjustable in the PWC controlled converter using the equation Fn=N/(W1-W2).

1. Introduction

In recent years, the circuit of the communication devices has been accelerated to be higher density packaging. The power of the switching converter has become large and large and the fluctuation of the switching noise has strongly spread in the wide frequency range. So it is very important to reduce an Electro Magnetic Interference (EMI) noise by suppressing the peak levels at the fundamental frequency and its harmonic frequencies.

On the other hand, for the communication equipment including the radio receiver, it is very important to reduce the radiation noise at the specific frequencies, such as the receiving frequency, by suppressing diffusion of power supply noise. We have proposed the pulse coding technique to have the notch characteristics at the desired frequency in the noise spectrum of the switching converter [3]~[6].

In this paper, we show the EMI reduction and the notch frequency in the noise spectrum of the switching converter, and show the experiment of the notch characteristics using the PWC method.

2. Switching Converters with Spread Spectrum

2.1 Basic DC-DC Switching Converters

Fig. 1 shows the basic block diagram of the buck type DC-DC converter[1],[2] with the PWM (Pulse Width Modulation) signal control and Fig.2 shows its main signals. This converter consists of the power stage and the control block. The power stage contains a main power switch, a free-wheel diode, an inductor and an output capacitor. The main switch is controlled by the PWM signal from the control block, which consists of an operational amplifier, a comparator and a reference voltage source. The comparator generates the PWM signal compared the saw-tooth signal with the amplified error voltage.

When the switch is ON, the inductor current flows from the input voltage source E and charges the output capacitance shown as the red solid line in Fig. 1. When the switch is OFF, the inductor current flows through the diode shown as the blue dashed line in Fig.1

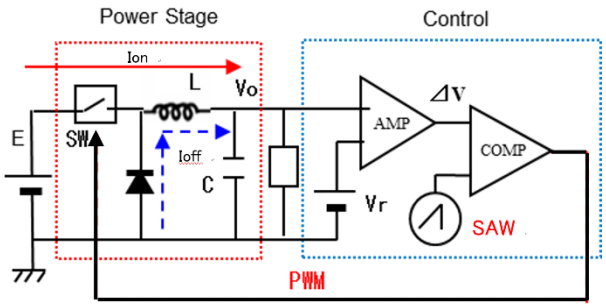

Fig. 1 Buck Converter with PWM Signal

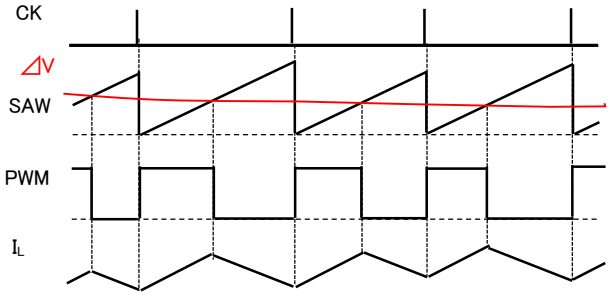

Fig. 2 Waveform of Buck Converter

2.2 EMI Reduction with Clock Modulation

In order to reduce the EMI noise, modulation of the clock pulse is usually used by shaking the phase or frequency of the clock in Fig. 1. The power spectrum of the PWM signal without the clock modulation is shown in Fig. 3. There is the line spectrum at the clock frequency (0.2MHz) and many harmonic spectra appear. The level of clock spectrum is 3.5V which is the largest in this figure.

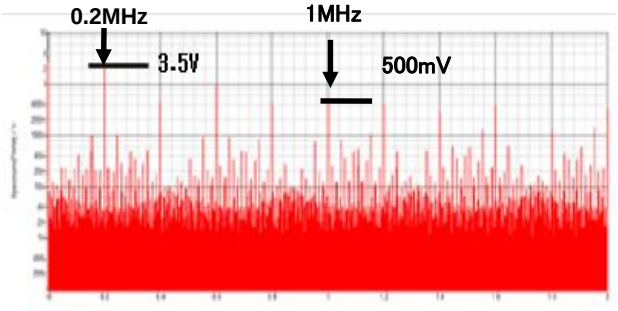

Fig. 3 Spectrum without EMI Reduction

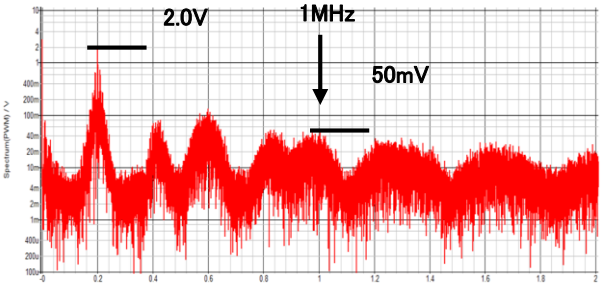

Fig. 4 Spectrum with EMI Reduction

3. Notch Frequency with Pulse Coding Control

3.1 Circuit of the Pulse Coding Control

Fig.5 shows the control circuit for the pulse coding. The amplified error voltage of the output voltage is compared with the reference voltage Vr and its output logic level is kept in the D-FF (flip-flop) by the clock for synchronizing with the clock. The output of this FF is called select signal SEL which chooses one of the two pulses input to the selector. These two pulses are the coding pulses generated using the modulated clock. We call the selected signal PCD (pulse coded driving) signal.

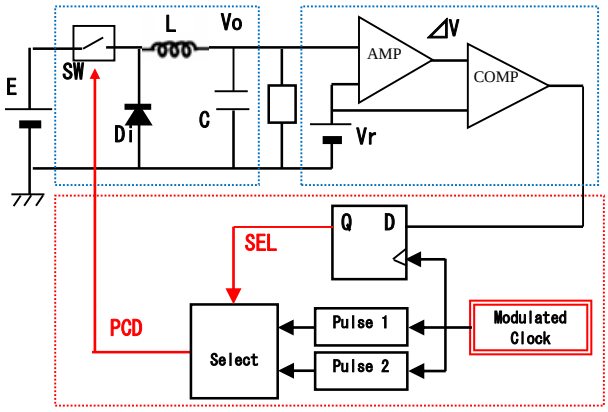

Fig. 5 Converter with Pulse Coding Control

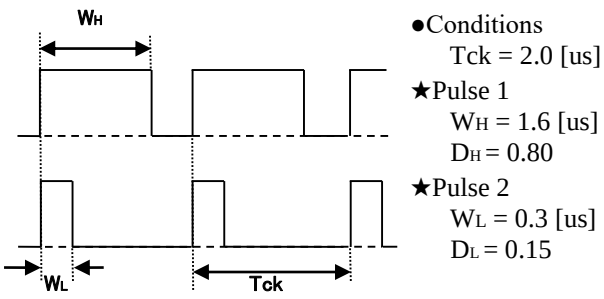

Fig. 6 Coded Pulses of PWC Control

In this simulation, the width of PWC pulses are used to generate the notch frequency in the power spectrum of the modulated clock. The conditions of the PWC control and the other conditions are Vi=10V, Vo=5.0V, Io=0.2A and Fck=500kHz as shown in Fig. 6.

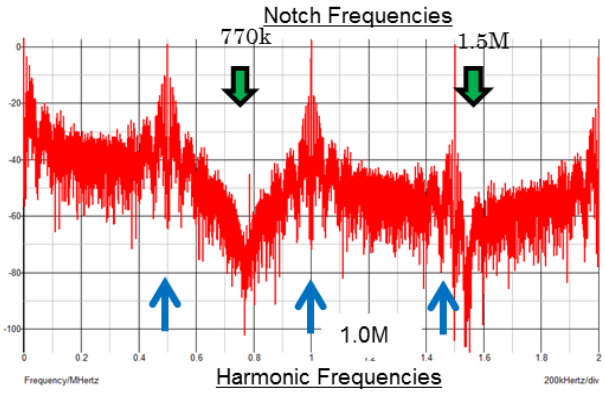

Fig. 7 Simulated Spectrum with PWC Control

3.2 Simulation Results with the PWC Control

Fig. 7 shows the spectrum of the coded pulses of the PCD signal. There appears the notch characteristics at the frequency of 770 kHz and 1.5MHz, which are the theoretical frequencies.

3.3 Derivation of Theoretical Notch Frequency

The PWM pulse of the PWC converter is the random series of the two pulses. The theoretical frequency of the PWC control is derived as bellow by performing Fast Fourier Transform to the pair of the coding pulses. The absolute value of Eq. (1) is derived to the next sinc Eq. (2).

$$F(\omega) = \int_{-\infty}^{\infty} f(t)\mathrm{e}^{-j\omega t}dt = \int_{0}^{t_1} \mathrm{e}^{-jwt}dt + \int_{\frac{T}{2}}^{\frac{T}{2}+t_2} \mathrm{e}^{-jwt}dt$$

$$= \frac{1}{\omega}\Big(\sin(\omega t_1) - \sin(\omega t_2) \ +j\cos(\omega t_1) - j\cos(\omega t_2)\Big) \quad (1)$$

$$|F(\omega)| = \frac{1}{\omega}\sqrt{4\sin^2\left(\frac{\omega t_2 - \omega t_1}{2}\right)} = (t_2 - t_1)\mathrm{sinc}\left(\frac{t_2 - t_1}{2}\omega\right) \quad (2)$$

Where ω=2πf, so the notch frequencies fn are derived in Eq. (3), where N is the natural number. Here, it depends on only the difference of the pulse width ($t_2 - t_1$).

$$(t_2 - t_1)\,\omega/2 = N\pi \quad \therefore \quad fn = N / (t_2 - t_1) \quad (3)$$

4. Automatic Generation of the Notch Frequency

4.1 Analysis of Relationship with the Clock Frequency and the Notch Frequency

Generally speaking, it is good for the notch frequency Fn to appear at the middle between the clock frequency Fck and its twice frequency 2Fck as shown in Fig. 7, or between its twice frequency and the three times frequency. Of course, Fn should be the frequency of the receiving signal Fin. These relationships are shown as the next Eq. (4), which are easy to be set using the PLL (Phase Locked Loop) circuit. Here, N is the natural number.

Fin = (N+0.5)·Fck : When N=1, Fin/3 = Fck/2, When N=2, Fin/5 = Fck/2 (4)

On the other hand, the operating duty Do of the PWM signal in the switching converter is usually represented like Do=Vo/Vin, here Vin and Vo are input/output DC voltages, respectively. Hence the pulse width To of the PWM signal is represented as shown in Eq. (5). According to Eq. (3), the period of the notch frequency Tn is derived from the difference between the pulse width of t_2 and t_1 as shown in Eq. (5). Here, Tp is the half of Tin and Tn equals to Tin.

To=Do*Tck=(Vo/Vin)*Tck , t_2 =To+Tp, t_1=To－Tp ∴ Tn = $t_2 - t_1$ = 2*Tp (5)

4.2 Simulation Result using the PLL Circuit

Fig. 8 shows the block diagram of the control circuit of the proposed converter. The received signal Fin and the generated clock signal Fck are synchronized by the PLL (Phase Locked Loop) circuit according to Eq. (4). In order to generate the coding pulses P_H and P_L, two periods of Tin and Tck are measured by the sawtooth signal and the peak voltage hold circuit. Tp and To are generated to be half of Tin and Tck by comparing these sawtooth signals and the half of the peak-held voltages Vin/2 and Vck/2 shown in Fig.9. Then P_H and P_L are derived by adding or subtracting as To$\pm$Tp.

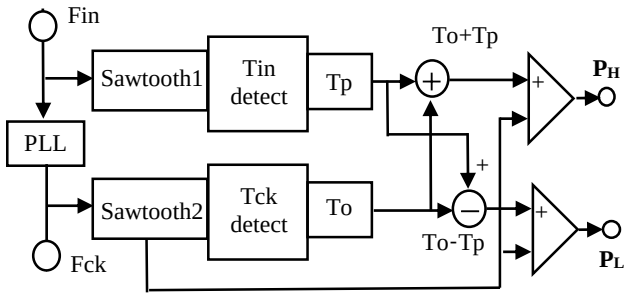

Fig. 8 Block diagram of proposed circuit

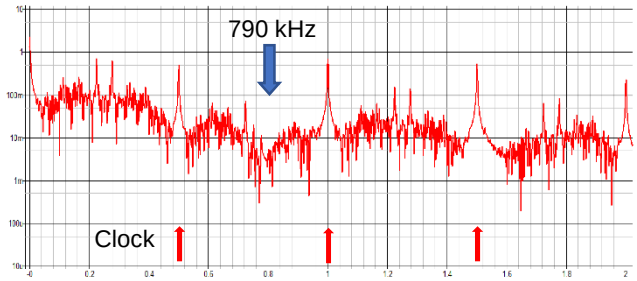

Fig. 10 Noise Spectrum with Pulse Coding 1

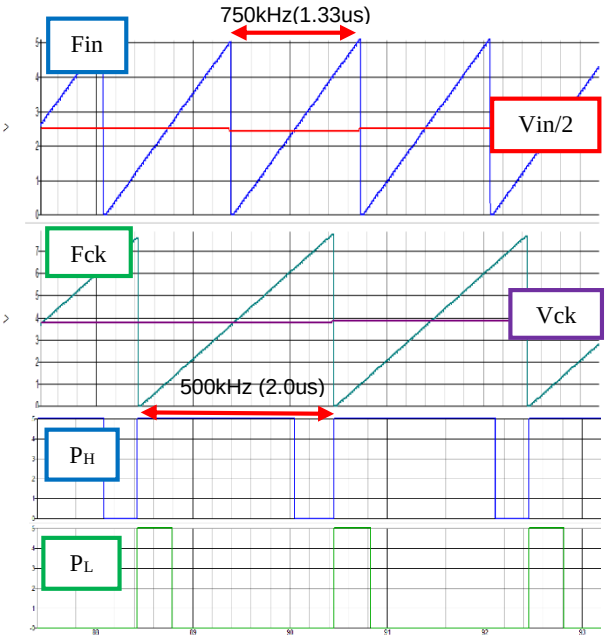

Fig. 9 Waveform of Fig.8 (Fin=750kHz)

In the proposed system, the input/output voltage are Vin=10V and Vo=5.0V, so the theoretical duty ratio of the PWM signal is Do=0.5 from Eq. (5). When the frequency of the input signal is set at Fin=750kHz, the frequency of the clock is guided at Fck=500kHz. In order to set the notch frequency at Fin=750 kHz, the calculated pulse width is W_{Ho} =1.67us and W_{Lo} =0.33us.

Seeing the simulation results, the simulated clock frequency Fcks is set to about 500kHz and the simulated widths of the coded pulses are set to about W_{HS} =1.64us and W_{LS} =0.36us as shown in Fig. 9. In this case, the theoretical simulation notch frequency is calculated at Fnso=780kHz and the simulated notch frequency is appeared at Fns=790kHz shown in Fig. 10, which is almost equal to the theoretical notch frequency Fin=750kHz.

4.3 Another Simulation Results

When the input frequency is higher than the twice frequency of the clock, it's suitable to set N=2 in Eq. (4). In this case, Fck/2 is phase-locked with Fin/5, here the input frequency is set Fin=1.0MHz and the phase-looked clock frequency is Fck=400kHz. Then the theoretical notch frequency will be Fno=1.0MHz. In this case, W_{HS} =1.74us and W_{LS} =0.80us and the simulated notch frequency is appeared at Fns =1.08MHz, which is between 2*Fck and 3*Fck. The second order notch frequency also appears at 2.15MHz as shown in Fig. 11.

4.4 Step response for input frequency change

In the communication devices, there are many changes of the receiving signal and the input frequency. It is important for these devices to response quickly for the frequency changes. Fig. 12 shows the responses of our proposed converter when N=1, here Fck=750kHz when Fin=1.0MHz. There are the output voltage ripple and the response of the PLL circuit when Fin changes 0.5M/ 1.0MHz. Here the waveform of Tck shows the response of the PLL circuit. The static voltage ripple is 15mVpp at Fin=0.5MHz and 8mVpp at Fin=1.0MHz. The undershoot is about 15mV and the settling time is about 150us.

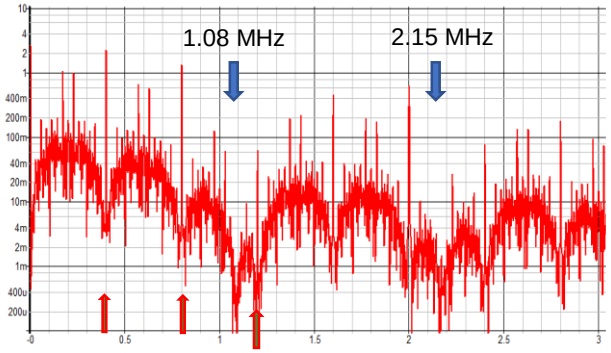

Fig.11 Noise Spectrum with Pulse coding 2

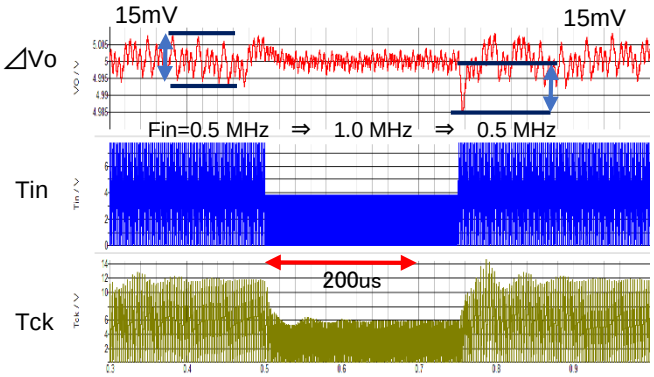

Fig. 12 Transient Response for Fin Change

5. Direct Generating the Clock Pulse

5.1 Proposed Circuit of the Direct Method

We have investigated the direct generating method of the clock pulse and calculated the coded pulses. The relationship between the input signal and the clock pulse is shown in Eq. (4). According to this equation, the period of the clock Tck is able to be generated by adding Tin and half of Tin shown in Fig. 15. Tin is measured using the digital counter. In a digital circuit, it is easy to make a half value with a shifter. After getting the data of Tck, the decoded pulses are made in the same way shown in Fig. 10.

$$Fin=(N+0.5)\cdot Fck \Rightarrow Tck=(N+0.5)\cdot Tin \quad (6)$$

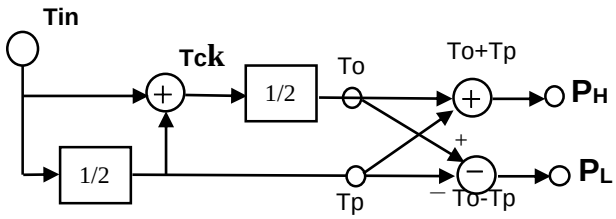

Fig. 13 Block Diagram of the New Circuit

5.2 Simulated results of the direct method

Fig. 14 shows the simulated pulses directly generated from the input signal. Here, 3・Fck equals to 2・Fin, it means 2・Tck=3・Tin. The conditions of this simulation are Fin= 750kHz (Tin= 1.33us) and N=1. Then Fck is set to be 500kHz (Tck=2.0us).

In the simulated spectrum of the direct method shown in Fig. 15, the generated clock is modulated with EMI reduction like Fig. 4. The notch characteristics clearly appears and its frequency is just 750 kHz which is equal to Fin. The bottom level of the notch frequency is about 1mV. There appears another big notch at F=3.0MHz, which is the 4th harmonic of the fundamental notch frequency Fn.

Fig. 16 shows another spectrum when the case of N=2 in the equation 4. In this case, the input frequency is Fin=1.27MHz then the clock frequency is set to be Fck=500kHz. There also appears another big notch at the 4th harmonic frequency F=5.06MHz whose bottom level is 0.3mV which is deeper than that of Fig. 15.

Fig. 17 shows the transient response when the input frequency is changed from 1.25M to 1.0MHz and to 0.75MHz. The clock frequency is changed according to the change of Fin. Fig. 17 also shows the change of the peak of the sawtooth signal of Fck. The settling time is only 2 clocks which is much faster than that of the case with the PLL circuit.

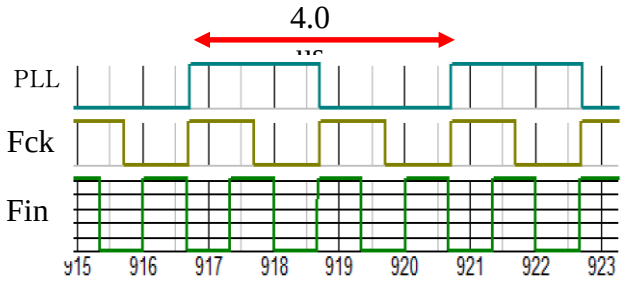

Fig. 14 Waveform of Direct Generate Method

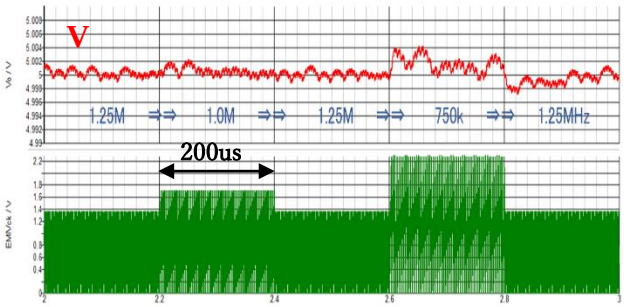

Fig. 17 Transient Response for Fin Change

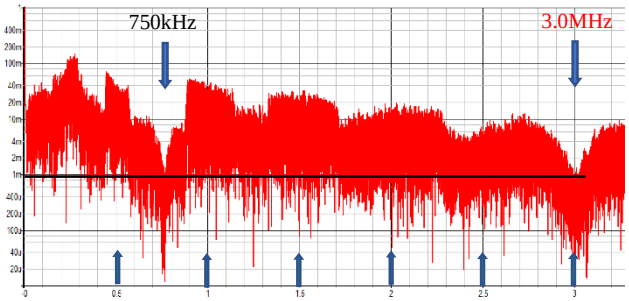

Fig. 15 Simulated spectrum (N=1)

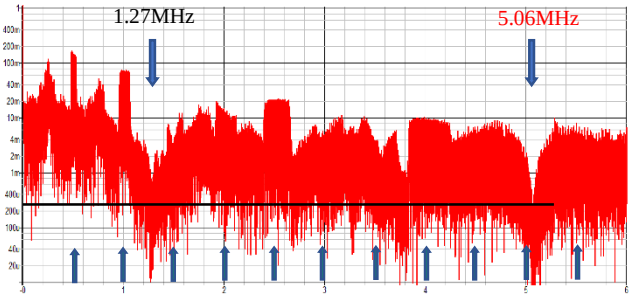

Fig. 16 Another simulated spectrum (N=2)

6. Conclusion

This paper has proposed a new technique to generate the notch characteristics at the desired frequency in the noise spectrum of the switching converter. The notch and the clock are automatically generated at the frequencies where the notch frequency Fn appears between the clock frequency Fck and its 2nd harmonic or the 2nd and the 3rd harmonics. In the direct generating method, the settling time of transient response for Fin change is only two clocks.

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